

ExpressCard™ POWER INTERFACE SWITCH

FEATURES

- Meets the ExpressCard™ Standard (ExpressCard|34 or ExpressCard|54)
- Compliant with the ExpressCard™ Compliance Checklists
- Fully Satisfies the ExpressCard™ Implementation Guidelines
- Supports Systems with WAKE Function
- TTL-Logic Compatible Inputs
- Short Circuit and Thermal Protection
- –40°C to 85°C Ambient Operating Temperature Range

- Available in a 20-pin TSSOP or 24-pin PowerPAD™ HTSSOP (Single)
- Available in a 32-pin PowerPAD™ HTSSOP (Dual)

APPLICATIONS

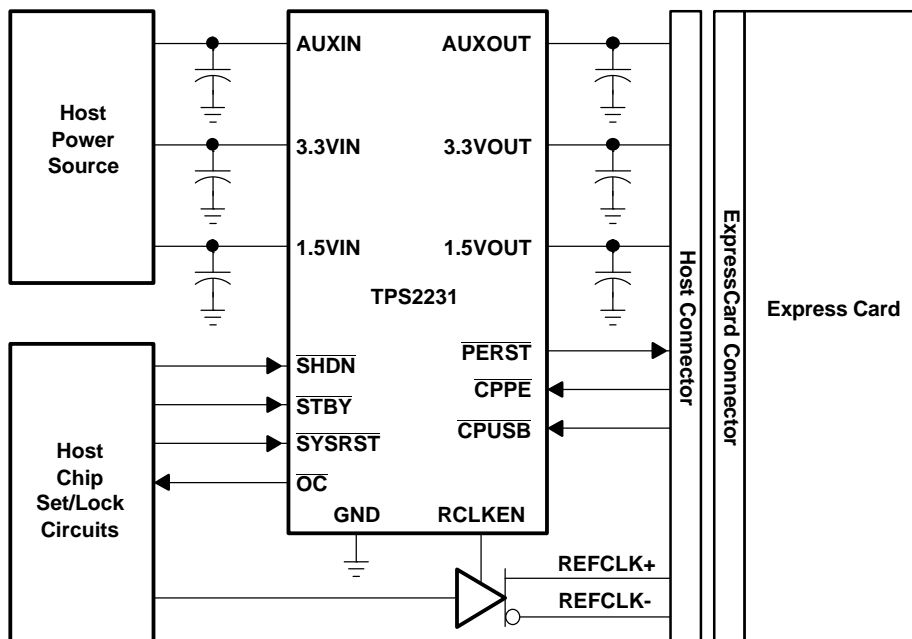
- Notebook Computers
- Desktop Computers
- Personal Digital Assistants (PDAs)
- Digital Cameras
- TV and Set Top Boxes

DESCRIPTION

The TPS2231 and TPS2236 ExpressCard power interface switches provide the total power management solution required by the ExpressCard specification. The TPS2231 and TPS2236 ExpressCard power interface switches distribute 3.3 V, AUX, and 1.5 V to the ExpressCard socket. Each voltage rail is protected with integrated current-limiting circuitry.

The TPS2231 supports systems with single-slot ExpressCard|34 or ExpressCard|54 sockets. The TPS2236 supports systems with dual-slot ExpressCard sockets.

End equipment for the TPS2231 and TPS2236 include notebook computers, desktop computers, personal digital assistants (PDAs), and digital cameras.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ExpressCard is a trademark of Personal Computer Memory Card International Association.
PowerPAD is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES ⁽¹⁾	
		TSSOP	PowerPAD HTSSOP
–40°C to 85°C	Single	TPS2231PW ⁽²⁾	TPS2231PWP
	Dual		TPS2236DAP ⁽²⁾

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., TPS2231PWPR).

(2) Product preview stage of development

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			UNIT
V _I	Input voltage range for card power	V _{I(3.3VIN)}	–0.3 V to 6 V
		V _{I(1.5VIN)}	–0.3 V to 6 V
		V _{I(AUXIN)}	–0.3 V to 6 V
Logic input/output voltage			–0.3 V to 6 V
V _O	Output voltage range	V _{O(3.3VOUT)}	–0.3 V to 6 V
		V _{O(1.5VOUT)}	–0.3 V to 6 V
		V _{O(AUXOUT)}	–0.3 V to 6 V
Continuous total power dissipation			See Dissipation Rating Table
I _O	Output current	I _{O(3.3VOUT)}	Internally limited
		I _{O(AUXOUT)}	Internally limited
		I _{O(1.5VOUT)}	Internally limited
T _J	Operating virtual junction temperature range		–40°C to 120°C
T _{stg}	Storage temperature range		–55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C
\overline{OC} sink current			10 mA
\overline{PERST} sink/source current			10 mA

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS (THERMAL RESISTANCE = °C/W)

PACKAGE ⁽¹⁾	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PW(20)	704.2 mW	7.41 mW/°C	370.6 mW	259.5 mW
PWP (24)	3153 mW	33.19 mW/°C	1659.5 mW	1161.6 mW
DAP (32) PowerPAD not soldered down	993.4 mW	10.46 mW/°C	522.8 mW	366 mW
DAP (32)	4040.8 mW	42.55 mW/°C	2126.8 mW	1488.7 mW

(1) These devices are mounted on an JEDEC low-k board (2-oz. traces on surface), (The table is assuming that the maximum junction temperature is 120°C). The power pad on the device must be soldered down to the power pad on the board if best thermal performance is needed.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V _{I(3.3VIN)}	Input voltage	3.3VIN is only required for its respective functions	3	3.6	V
V _{I(1.5VIN)}		1.5VIN is only required for its respective functions	1.35	1.65	
V _{I(AUXIN)}		AUXIN is required for all circuit operations	3	3.6	
I _{O(3.3VOUT)}	Continuous output current	T _J = 120°C	0	1.3	A
I _{O(1.5VOUT)}			0	650	mA
I _{O(AUXOUT)}			0	275	mA
T _J	Operating virtual junction temperature		−40	120	°C

ELECTRICAL CHARACTERISTICS

$T_J = 25^\circ\text{C}$, $V_{I(3.3VIN)} = V_{I(AUXIN)} = 3.3\text{ V}$, $V_{I(1.5VIN)} = 1.5\text{ V}$, $V_{I(SHDNx)} = V_{I(STBYx)} = 3.3\text{ V}$, $V_{I(CPPEX)} = V_{I(CPUSBx)} = 0\text{ V}$, $V_{I(SYSRST)} = 3.3\text{ V}$, OCx and RCLKENx and PERSTx are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER SWITCH								
Power switch resistance	3.3VIN to 3.3VOUT with two switches on for dual		T _J = 25°C, I = 1300 mA each		45		mΩ	
			T _J = 100°C, I = 1300 mA each		68			
	1.5VIN to 1.5VOUT With two switches on for dual		T _J = 25°C, I = 650 mA each		46		mΩ	
			T _J = 100°C, I = 650 mA each		70			
	AUXIN to AUXOUT with two switches on for dual		T _J = 25°C, I = 275 mA each		120		mΩ	
			T _J = 100°C, I = 275 mA each		200			
R _(DIS_FET)	Discharge resistance on 3.3V/1.5V/AUX outputs		V _{I(/SHDNx)} = 0 V, I _(discharge) = 1 mA		100	500	Ω	
I _{OS}	Short-circuit output current ⁽¹⁾	I _{OS(3.3VOUT)} (steady-state value)		T _J [−40, 120°C]. Output powered into a short	1.35	2	2.5	A
		I _{OS(1.5VOUT)} (steady-state value)			0.67	1	1.3	A
		I _{OS(AUXOUT)} (steady-state value)			275	450	600	mA
Thermal shutdown	Trip point, T _J	Rising temperature, not in overcurrent condition		155	165		°C	
		Overcurrent condition		120	130			
	Hysteresis				10			
Current-limit response time	From short to the 1 st threshold within 1.1 times of final current limit, T _J = 25°C		V _{O(3.3VOUT)} with 100-mΩ short		43	100	μs	
			V _{O(1.5VOUT)} with 100-mΩ short		100	140		
			V _{O(AUXOUT)} with 100-mΩ short		38	100		
I _I	Normal operation of TPS2236	I _{I(AUXIN)}	Outputs are unloaded, T _J [−40, 120°C] (does not include CPPEX and CPUSBx logic pullup currents)		200	μA		
		I _{I(3.3VIN)}			25			
		I _{I(1.5VIN)}			15			
	Normal operation of TPS2231	I _{I(AUXIN)}			85	150	μA	
		I _{I(3.3VIN)}			10	15		
		I _{I(1.5VIN)}			2.5	10		

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

ELECTRICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$, $V_{I(3.3\text{VIN})} = V_{I(\text{AUXIN})} = 3.3\text{ V}$, $V_{I(1.5\text{VIN})} = 1.5\text{ V}$, $V_{I(\text{SHDNx})}$, $V_{I(\text{STBYx})} = 3.3\text{ V}$, $V_{I(\text{CPPEx})} = V_{I(\text{CPUSBx})} = 0\text{ V}$,
 $V_{I(\text{SYSRST})} = 3.3\text{ V}$, OCx and RCLKENx and PERSTx are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I _I	Total input quiescent current	Normal operation of TPS2236	I _{I(AUXIN)}	Outputs are unloaded, T _J [−40, 120°C] (include $\overline{\text{CPPE}}_{\text{x}}$ and $\overline{\text{CPUSB}}_{\text{x}}$ logic pullup currents)		320	μA	
			I _{I(3.3VIN)}			25		
			I _{I(1.5VIN)}			15		
		Normal operation of TPS2231	I _{I(AUXIN)}			120	210	μA
			I _{I(3.3VIN)}			10	15	
			I _{I(1.5VIN)}			2.5	10	
		Shutdown mode of TPS2236	I _{I(AUXIN)}	$\overline{\text{CPUSB}} = \overline{\text{CPPE}} = 0\text{ V}$ $\overline{\text{SHDN}} = 0\text{ V}$ (discharge FETs are on) (include $\overline{\text{CPPE}}_{\text{x}}$ and $\overline{\text{CPUSB}}_{\text{x}}$ logic pullup currents and $\overline{\text{SHDN}}$ pullup current) T _J [−40, 120°C]		440	μA	
			I _{I(3.3VIN)}			20		
			I _{I(1.5VIN)}			20		
		Shutdown mode of TPS2231	I _{I(AUXIN)}			144	270	μA
			I _{I(3.3VIN)}			3.5	10	
			I _{I(1.5VIN)}			0.5	10	
I _{Ikg(FWD)}	TPS2236	I _{I(AUXIN)}	$\overline{\text{SHDN}} = 3.3\text{ V}$, $\overline{\text{CPUSB}} = \overline{\text{CPPE}} = 3.3\text{ V}$ (no card present, discharge FETs are on); current measured at input pins T _J = 120°C, includes RCLKEN pullup current		100	μA		
		I _{I(3.3VIN)}			100			
		I _{I(1.5VIN)}			100			
	TPS2231	I _{I(AUXIN)}			20	50	μA	
		I _{I(3.3VIN)}			0.1	50		
		I _{I(1.5VIN)}			0.1	50		
I _{Ikg(RVS)}	I _{I(AUXOUT)}	T _J = 25°C	V _{O(AUXOUT)} = V _{O(3.3VOUT)} = 3.3 V; V _{O(1.5VOUT)} = 1.5 V; All voltage inputs are grounded (current measured from output pins going in)		0.1	10	μA	
		T _J = 120°C			50			
	I _{I(3.3VOUT)}	T _J = 25°C			0.1	10	μA	
		T _J = 120°C			50			
	I _{I(1.5VOUT)}	T _J = 25°C			0.1	10	μA	
		T _J = 120°C			50			
LOGIC SECTION ($\overline{\text{SYSRST}}$, $\overline{\text{SHDN}}_{\text{x}}$, STBY_{x} , $\overline{\text{PERST}}_{\text{x}}$, RCLKEN _x , $\overline{\text{OC}}_{\text{x}}$, $\overline{\text{CPUSB}}_{\text{x}}$, $\overline{\text{CPPE}}_{\text{x}}$)								
	Logic input supply current	I _{I(SYSRST)}	Input	$\overline{\text{SYSRST}} = 3.6\text{ V}$, sinking		0	1	μA
				$\overline{\text{SYSRST}} = 0\text{ V}$, sourcing	10		30	
		I _{I(SHDNx)}	Input	$\overline{\text{SHDN}}_{\text{x}} = 3.6\text{ V}$, sinking		0	1	μA
				$\overline{\text{SHDN}}_{\text{x}} = 0\text{ V}$, sourcing	10		30	
		I _{I(STBYx)}	Input	$\text{STBY}_{\text{x}} = 3.6\text{ V}$, sinking		0	1	μA
				$\text{STBY}_{\text{x}} = 0\text{ V}$, sourcing	10		30	
	I _{I(RCLKENx)}	Input	RCLKEN _x = 0 V, sourcing	10		30	μA	
	I _{I(CPUSBx)} or I _{I(CPPEx)}	Inputs	$\overline{\text{CPUSB}}$ or $\overline{\text{CPPE}} = 0\text{ V}$, sinking		0	1	μA	
			$\overline{\text{CPUSB}}$ or $\overline{\text{CPPE}} = 3.6\text{ V}$, sourcing	10		30		
	Logic input voltage	High level			2		V	
		Low level				0.8		
RCLEN output low voltage		Output	I _{O(RCLKEN)} = 60 μA			0.4	V	
$\overline{\text{PERST}}$ assertion threshold of output voltage ($\overline{\text{PERST}}$ asserted when any output voltage falls below the threshold)			3.3VOUT falling	2.7		3	V	
			AUXOUT falling	2.7		3		
			1.5VOUT falling	1.2		1.35		
$\overline{\text{PERST}}$ assertion delay from output voltage			3.3VOUT, AUXOUT, or 1.5VOUT falling			500	ns	
$\overline{\text{PERST}}$ de-assertion delay from output voltage			3.3VOUT, AUXOUT, and 1.5VOUT rising within tolerance	4	10	20	ms	
$\overline{\text{PERST}}$ assertion delay from $\overline{\text{SYSRST}}$			Max time from $\overline{\text{SYSRST}}$ asserted or de-asserted			500	ns	

ELECTRICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$, $V_{I(3.3\text{VIN})} = V_{I(\text{AUXIN})} = 3.3\text{ V}$, $V_{I(1.5\text{VIN})} = 1.5\text{ V}$, $V_{I(\text{SHDNx})}$, $V_{I(\text{STBYx})} = 3.3\text{ V}$, $V_{I(\text{CPPEx})} = V_{I(\text{CPUSBx})} = 0\text{ V}$,
 $V_{I(\text{SYSRST})} = 3.3\text{ V}$, $\overline{\text{OCx}}$ and RCLKENx and PERSTx are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{W(\text{PERST})}$	$\overline{\text{PERST}}$ minimum pulse width	3.3VOUT, AUXOUT, or 1.5VOUT falling out of tolerance or triggered by $\overline{\text{SYSRST}}$	100	250		μs
	$\overline{\text{PERST}}$ output low voltage	$I_{O(\text{PERST})} = 500\text{ }\mu\text{A}$			0.4	V
	$\overline{\text{PERST}}$ output high voltage		2.4			V
	$\overline{\text{OC}}$ output low voltage	$I_{O(\text{OC})} = 2\text{ mA}$			0.4	V
	$\overline{\text{OC}}$ leakage current	$V_{O(\text{OC})} = 3.6\text{ V}$			1	μA
	$\overline{\text{OC}}$ deglitch	Falling into or out of an overcurrent condition	6		20	mS
UNDERVOLTAGE LOCKOUT (UVLO)						
	3.3VIN UVLO	3.3VIN level, below which 3.3VIN and 1.5VIN switches are off	2.6		2.9	V
	1.5VIN UVLO	1.5VIN level, below which 3.3VIN and 1.5VIN switches are off	1		1.25	
	AUXIN UVLO	AUXIN level, below which all switches are off	2.6		2.9	
	UVLO hysteresis			100		mV

SWITCHING CHARACTERISTICS

$T_J = 25^\circ\text{C}$, $V_{I(3.3\text{VIN})} = V_{I(\text{AUXIN})} = 3.3\text{ V}$, $V_{I(1.5\text{VIN})} = 1.5\text{ V}$, $V_{I(\text{SHDNx})}$, $V_{I(\text{STBYx})} = 3.3\text{ V}$, $V_{I(\text{CPPEx})} = V_{I(\text{CPUSBx})} = 0\text{ V}$,
 $V_{I(\text{SYSRST})} = 3.3\text{ V}$, $\overline{\text{OCx}}$ and RCLKENx and PERSTx are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise times	3.3VIN to 3.3VOUT $C_L(3.3\text{VOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(3.3\text{VOUT})} = 0\text{ A}$	0.1		3	ms
		AUXIN to AUXOUT $C_L(\text{AUXOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(\text{AUXOUT})} = 0\text{ A}$	0.1		3	
		1.5VIN to 1.5VOUT $C_L(1.5\text{VOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(1.5\text{VOUT})} = 0\text{ A}$	0.1		3	
		3.3VIN to 3.3VOUT $C_L(3.3\text{VOUT}) = 100\text{ }\mu\text{F}$, $R_L = V_{I(3.3\text{VIN})}/1\text{ A}$	0.1		6	
		AUXIN to AUXOUT $C_L(\text{AUXOUT}) = 100\text{ }\mu\text{F}$, $R_L = V_{I(\text{AUXIN})}/0.250\text{ A}$	0.1		6	
		1.5VIN to 1.5VOUT $C_L(1.5\text{VOUT}) = 100\text{ }\mu\text{F}$, $R_L = V_{I(1.5\text{VIN})}/0.500\text{ A}$	0.1		6	
t_f	Output fall times when card removed (both CPUSB and CPPE de-asserted)	3.3VIN to 3.3VOUT $C_L(3.3\text{VOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(3.3\text{VOUT})} = 0\text{ A}$	10		150	μs
		AUXIN to VAUXOUT $C_L(\text{AUXOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(\text{AUXOUT})} = 0\text{ A}$	10		150	
		1.5VIN to 1.5VOUT $C_L(1.5\text{VOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(1.5\text{VOUT})} = 0\text{ A}$	10		150	
		3.3VIN to 3.3VOUT $C_L(3.3\text{VOUT}) = 20\text{ }\mu\text{F}$, $I_{O(3.3\text{VOUT})} = 0\text{ A}$	2		30	ms
		AUXIN to VAUXOUT $C_L(\text{AUXOUT}) = 20\text{ }\mu\text{F}$, $I_{O(\text{AUXOUT})} = 0\text{ A}$	2		30	
		1.5VIN to 1.5VOUT $C_L(1.5\text{VOUT}) = 20\text{ }\mu\text{F}$, $I_{O(1.5\text{VOUT})} = 0\text{ A}$	2		30	
t_f	Output fall times when SHDN asserted (card is present)	3.3VIN to 3.3VOUT $C_L(3.3\text{VOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(3.3\text{VOUT})} = 0\text{ A}$	10		150	μs
		AUXIN to VAUXOUT $C_L(\text{AUXOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(\text{AUXOUT})} = 0\text{ A}$	10		150	
		1.5VIN to 1.5VOUT $C_L(1.5\text{VOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(1.5\text{VOUT})} = 0\text{ A}$	10		150	
		3.3VIN to 3.3VOUT $C_L(3.3\text{VOUT}) = 100\text{ }\mu\text{F}$, $R_L = V_{I(3.3\text{VIN})}/1\text{ A}$	0.1		5	ms
		AUXIN to VAUXOUT $C_L(\text{AUXOUT}) = 100\text{ }\mu\text{F}$, $R_L = V_{I(\text{AUXIN})}/0.250\text{ A}$	0.1		5	
		1.5VIN to 1.5VOUT $C_L(1.5\text{VOUT}) = 100\text{ }\mu\text{F}$, $R_L = V_{I(1.5\text{VIN})}/0.500\text{ A}$	0.1		5	
$t_{pd(\text{on})}$	Turn-on propagation delay	3.3VIN to 3.3VOUT $C_L(3.3\text{VOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(3.3\text{VOUT})} = 0\text{ A}$	0.1		1	ms
		AUXIN to VAUXOUT $C_L(\text{AUXOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(\text{AUXOUT})} = 0\text{ A}$	0.05		0.5	
		1.5VIN to 1.5VOUT $C_L(1.5\text{VOUT}) = 0.1\text{ }\mu\text{F}$, $I_{O(1.5\text{VOUT})} = 0\text{ A}$	0.1		1	
		3.3VIN to 3.3VOUT $C_L(3.3\text{VOUT}) = 100\text{ }\mu\text{F}$, $R_L = V_{I(3.3\text{VIN})}/1\text{ A}$	0.1		1.5	
		AUXIN to VAUXOUT $C_L(\text{AUXOUT}) = 100\text{ }\mu\text{F}$, $R_L = V_{I(\text{AUXIN})}/0.250\text{ A}$	0.05		1	
		1.5VIN to 1.5VOUT $C_L(1.5\text{VOUT}) = 100\text{ }\mu\text{F}$, $R_L = V_{I(1.5\text{VIN})}/0.500\text{ A}$	0.1		1.5	

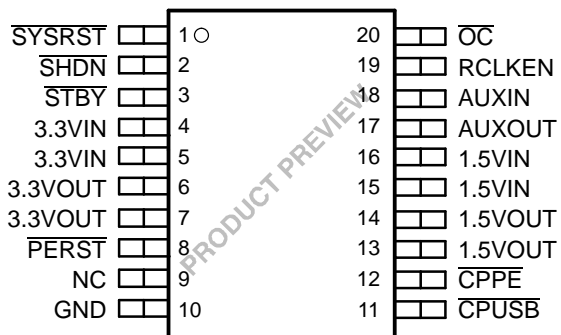
SWITCHING CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$, $V_{I(3.3\text{VIN})} = V_{I(\text{AUXIN})} = 3.3\text{ V}$, $V_{I(1.5\text{VIN})} = 1.5\text{ V}$, $V_{I(\text{SHDNx})}$, $V_{I(\text{STBYx})} = 3.3\text{ V}$, $V_{I(\text{CPPEx})} = V_{I(\text{CPUSBx})} = 0\text{ V}$, $V_{I(\text{SYSRST})} = 3.3\text{ V}$, OCx and RCLKENx and PERSTx are open, all voltage outputs unloaded (unless otherwise noted)

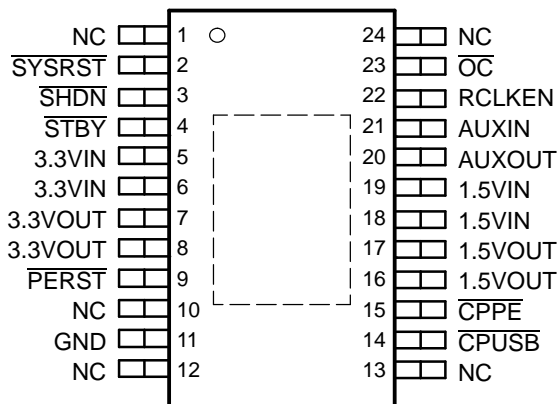
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{pd(off)}}$ Turn-off propagation delay	3.3VIN to 3.3VOUT	$C_{L(3.3\text{VOUT})} = 0.1\text{ }\mu\text{F}$, $I_{O(3.3\text{VOUT})} = 0\text{ A}$		0.1	1.5
	AUXIN to VAUXOUT	$C_{L(\text{AUXOUT})} = 0.1\text{ }\mu\text{F}$, $I_{O(\text{AUXOUT})} = 0\text{ A}$		0.05	0.5
	1.5VIN to 1.5VOUT	$C_{L(1.5\text{VOUT})} = 0.1\text{ }\mu\text{F}$, $I_{O(1.5\text{VOUT})} = 0\text{ A}$		0.1	1.5
	3.3VIN to 3.3VOUT	$C_{L(3.3\text{VOUT})} = 100\text{ }\mu\text{F}$, $R_L = V_{I(3.3\text{VIN})}/1\text{ A}$		0.1	1.5
	AUXIN to VAUXOUT	$C_{L(\text{AUXOUT})} = 100\text{ }\mu\text{F}$, $R_L = V_{I(\text{AUXIN})}/0.250\text{ A}$		0.05	0.5
	1.5VIN to 1.5VOUT	$C_{L(1.5\text{VOUT})} = 100\text{ }\mu\text{F}$, $R_L = V_{I(1.5\text{VIN})}/0.500\text{ A}$		0.1	1

PIN ASSIGNMENTS

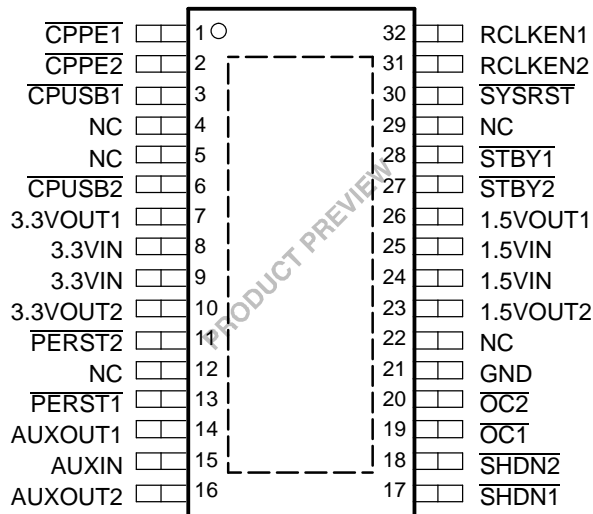
TPS2231
PW PACKAGE
(TOP VIEW)



TPS2231
PWP PACKAGE
(TOP VIEW)



TPS2236
DAP PACKAGE
(TOP VIEW)



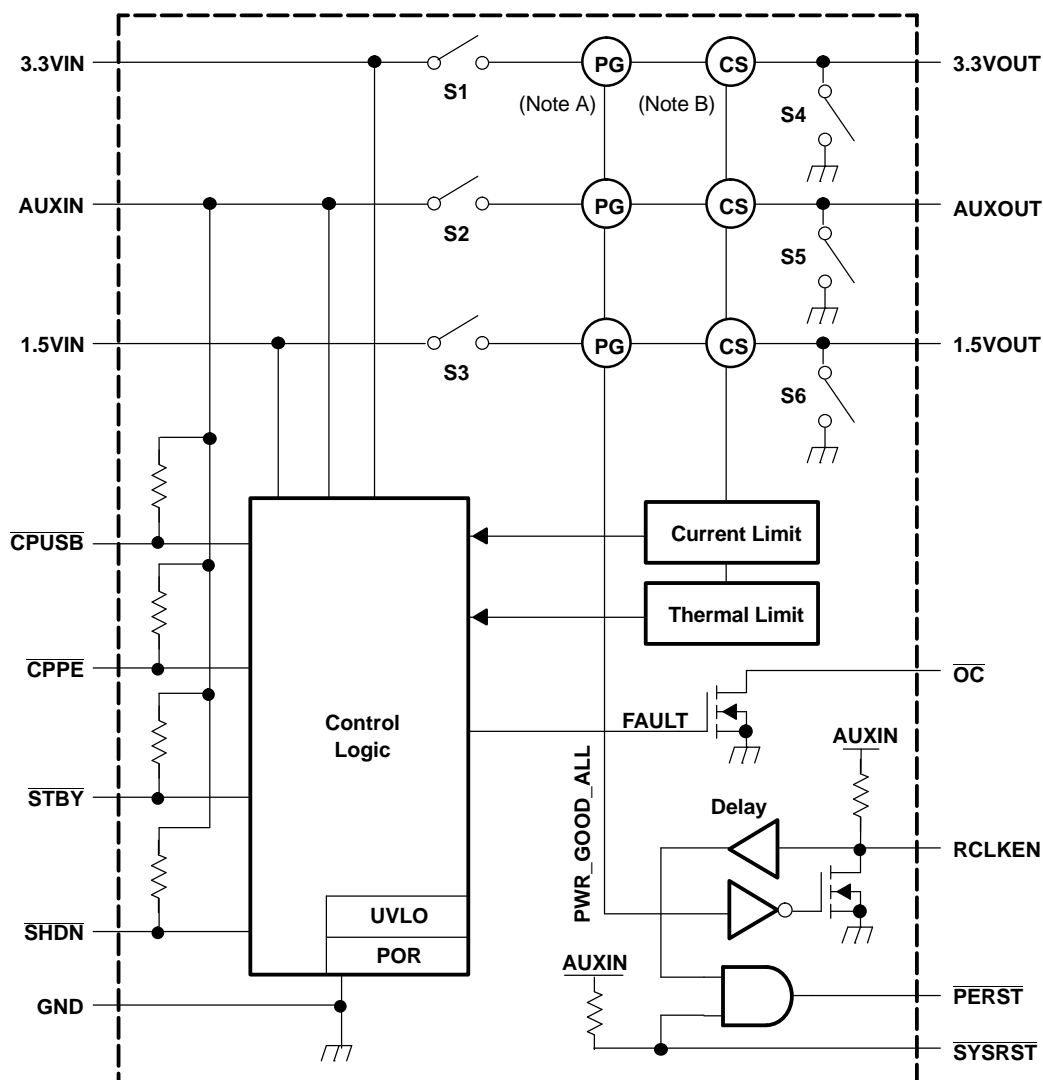
NC – No internal connection

TERMINAL FUNCTIONS

TERMINAL					I/O	DESCRIPTION
TPS2231			TPS2236			
NAME	NO.		NAME	NO.		
	PW	PWP		DAP		
3.3VIN	4, 5	5, 6	3.3VIN	8, 9	I	3.3-V input for 3.3VOUT
1.5VIN	15, 16	18, 19	1.5VIN	24, 25	I	1.5-V input for 1.5VOUT
AUXIN	18	21	AUXIN	15	I	AUX input for AUXOUT and chip power
GND	10	11	GND	21		Ground
3.3VOUT	6, 7	7, 8	3.3VOUT1	7	O	Switched output that delivers 0 V, 3.3 V or high impedance to card
1.5VOUT	13, 14	16, 17	1.5VOUT1	26	O	Switched output that delivers 0 V, 1.5 V or high impedance to card
AUXOUT	17	20	AUXOUT1	14	O	Switched output that delivers 0 V, AUX or high impedance to card
			3.3VOUT2	10	O	Switched output that delivers 0 V, 3.3 V or high impedance to card
			1.5VOUT2	23	O	Switched output that delivers 0 V, 1.5 V or high impedance to card
			AUXOUT2	16	O	Switched output that delivers 0 V, AUX or high impedance to card
$\overline{\text{SYSRST}}$	1	2	$\overline{\text{SYSRST}}$	30	I	System Reset input – active low, logic level signal. Internally pulled up to AUXIN.
$\overline{\text{CPPE}}$	12	15	$\overline{\text{CPPE1}}$	1	I	Card Present input for PCI Express cards. Internally pulled up to AUXIN.
$\overline{\text{CPUSB}}$	11	14	$\overline{\text{CPUSB1}}$	3	I	Card Present input for USB cards. Internally pulled up to AUXIN.
			$\overline{\text{CPPE2}}$	2	I	Card Present input for PCI Express cards. Internally pulled up to AUXIN.
			$\overline{\text{CPUSB2}}$	6	I	Card Present input for USB cards. Internally pulled up to AUXIN.
$\overline{\text{PERST}}$	8	9	$\overline{\text{PERST1}}$	13	O	A logic level power good to slot 0 (with delay)
			$\overline{\text{PERST2}}$	11	O	A logic level power good to slot 1 (with delay)
$\overline{\text{SHDN}}$	2	3	$\overline{\text{SHDN1}}$	17	I	Shutdown input – active low, logic level signal. Internally pulled up to AUXIN.
			$\overline{\text{SHDN2}}$	18	I	Shutdown input – active low, logic level signal. Internally pulled up to AUXIN.
$\overline{\text{STBY}}$	3	4	$\overline{\text{STBY1}}$	28	I	Standby input – active low, logic level signal. Internally pulled up to AUXIN.
			$\overline{\text{STBY2}}$	27	I	Standby input – active low, logic level signal. Internally pulled up to AUXIN.
RCLKEN	19	22	RCLKEN1	32	I/O	Reference Clock Enable signal. As an output, a logic level power good to host for slot 0 (no delay – open drain). As an input, if kept inactive (low) by the host, prevents $\overline{\text{PERST}}$ from being de-asserted. Internally pulled up to AUXIN.
			RCLKEN2	31	I/O	Reference Clock Enable signal. As an output, a logic level power good to host for slot 1 (no delay – open drain). As an input, if kept inactive (low) by the host, prevents $\overline{\text{PERST}}$ from being de-asserted. Internally pulled up to AUXIN.
$\overline{\text{OC}}$	20	23	$\overline{\text{OC1}}$	19	O	Overcurrent status output for slot 0 (open drain)
			$\overline{\text{OC2}}$	20	O	Overcurrent status output for slot 1 (open drain)
NC	9	1, 10, 12, 13, 24	NC	4, 5, 12, 22, 29		No connection

FUNCTIONAL BLOCK DIAGRAM

Single ExpressCard Power Switch

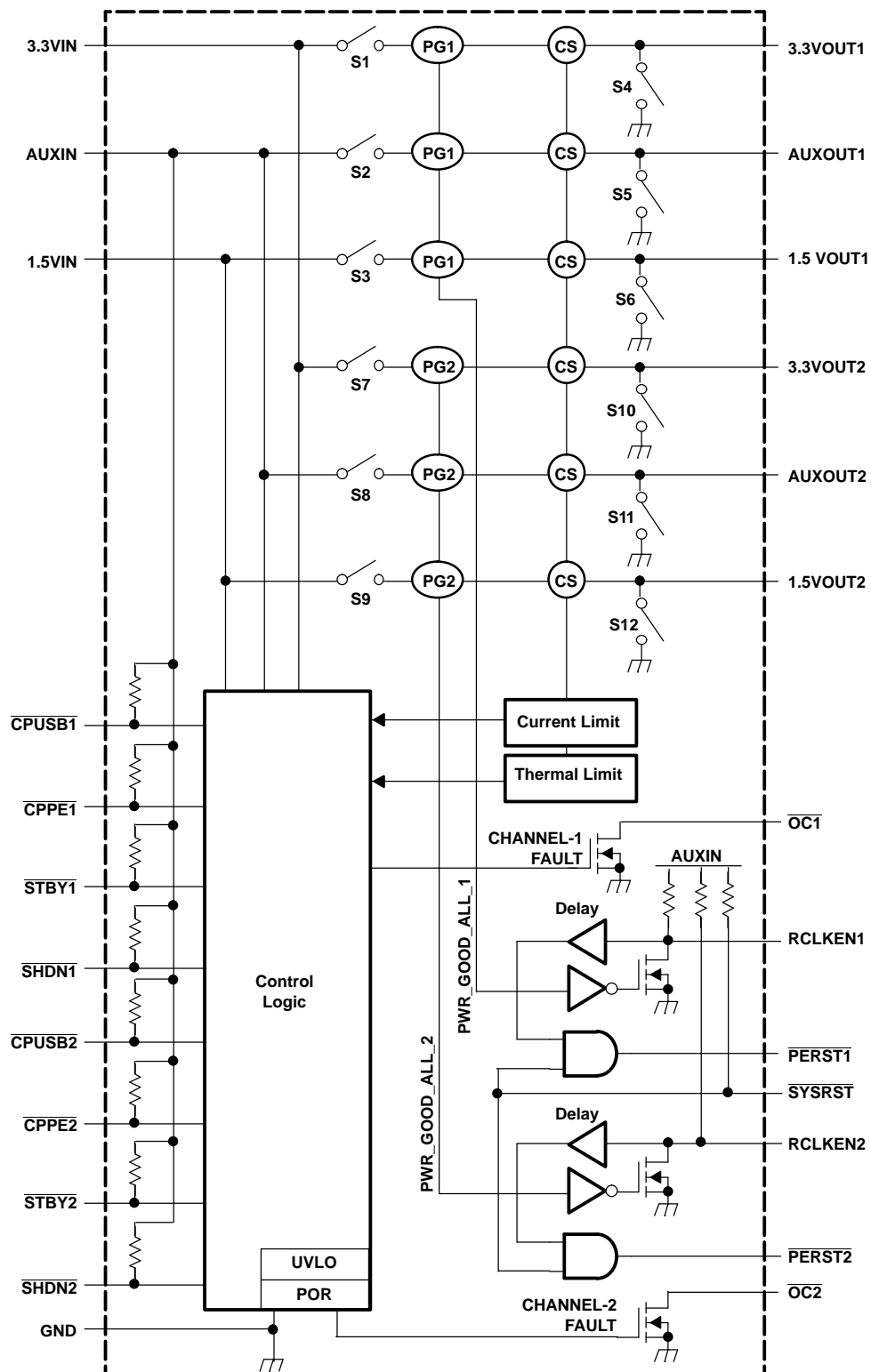


Note A: PG = power good

Note B: CS = current sense

FUNCTIONAL BLOCK DIAGRAM (continued)

Dual ExpressCard Power Switch



DETAILED PIN DESCRIPTIONS

CPPE

A logic low level on this input indicates that the card present supports PCI Express functions. CPPE connects to the AUXIN input through an internal pullup. When a card is inserted, CPPE is physically connected to ground if the card supports PCI Express functions.

CPUSB

A logic low level on this input indicates that the card present supports USB functions. CPUSB connects to the AUXIN input through an internal pullup. When a card is inserted, CPUSB is physically connected to ground if the card supports USB functions.

SHDN

When asserted (logic low), this input instructs the power switch to turn off all voltage outputs and the discharge FETs are activated. SHDN has an internal pullup connected to AUXIN.

STBY

When asserted (logic low) after the card is inserted, this input places the power switch in standby mode by turning off the 3.3-V and 1.5-V power switches and keeping the AUX switch on. If asserted prior to the card being present, STBY places the power switch in OFF Mode by turning off the AUX, 3.3-V, and 1.5-V power switches. STBY has an internal pullup connected to AUXIN.

RCLKEN

This pin serves as both an input and an output. On power up, a discharge FET keeps this signal at a low state as long as any of the output power rails are out of their tolerance range. Once all output power rails are within tolerance, the switch releases RCLKEN allowing it to transition to a high state (internally pulled up to AUXIN). The transition of RCLKEN from a low to a high state starts an internal timer for the purpose of deasserting PERST. As an input, RCLKEN can be kept low to delay the start of the PERST internal timer.

Because RCLKEN is internally connected to a discharge FET, this pin can only be driven low and should never be driven high as a logic input. When an external circuit drives this pin low, RCLKEN becomes an input; otherwise, this pin is an output.

RCLKEN can be used by the host system to enable a clock driver.

PERST

On power up, this output remains asserted (logic level low) until all power rails are within tolerance. Once all power rails are within tolerance and RCLKEN has been released (logic high), PERST is deasserted (logic high) after a time delay as shown in the parametric table. On power down, this output is asserted whenever any of the power rails drop below their voltage tolerance.

The PERST signal is an output from the host system and an input to the ExpressCard module. This signal is only used by PCI Express-based modules and its function is to place the ExpressCard module in a reset state.

During power up, power down, or whenever power to the ExpressCard module is not stable or not within voltage tolerance limits, the ExpressCard standard requires that PERST be asserted. As a result, this signal also serves as a power-good indicator to the ExpressCard module, and the relationship between the power rails and PERST are explicitly defined in the ExpressCard standard.

The host can also place the ExpressCard module in a reset state by asserting a system reset SYSRST. This system reset generates a PERST to the ExpressCard module without disrupting the voltage rails. This is what is normally called a *warm* reset. However, in a *cold* start situation, the system reset can also be used to extend the length of time that PERST is asserted.

Detailed Pin Descriptions (continued)

SYSRST

This input is driven by the host system and directly affects PERST. Asserting SYSRST (logic low) forces PERST to assert. RCLKEN is not affected by the assertion of SYSRST. SYSRST has an internal pullup connected to AUXIN.

OC

This pin is an open-drain output. When any of the three power switches (AUX, 3.3V, and 1.5V) is in an overcurrent condition, OC is asserted (logic low) by an internal discharge FET with a deglitch delay. Otherwise, the discharge FET is open, and the pin can be pulled up to a power supply through an external resistor.

FUNCTIONAL TRUTH TABLES

TRUTH TABLE FOR VOLTAGE OUTPUTS

VOLTAGE INPUTS ⁽¹⁾			LOGIC INPUTS			VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	<u>SHDN</u>	<u>STBY</u>	<u>CP</u> ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

- (1) For input voltages, *On* means the respective input voltage is higher than its turnon threshold voltage; otherwise, the voltage is *Off* (for AUX input, *Off* means the voltage is close to zero volt).
- (2) For output voltages, *On* means the respective power switch is turned on so the input voltage is connected to the output; *Off* means the power switch and its output discharge FET are both off; *GND* means the power switch is off but the output discharge FET is on so the voltage on the output is pulled down to 0 V.
- (3) *Mode* assigns each set of input conditions and respective output voltage results to a different name. These modes are referred to as input conditions in the following *Truth Table for Logic Outputs*.
- (4) CP = CPUSB and CPPE– equal to 1 when both CPUSB and CPPE signals are logic high, or equal to 0 when either CPUSB or CPPE is low.

TRUTH TABLE FOR LOGIC OUTPUTS

INPUT CONDITIONS			LOGIC OUTPUTS	
MODE	<u>SYSRST</u>	RCLKEN ⁽¹⁾	<u>PERST</u>	RCLKEN ⁽²⁾
OFF	X	X	0	0
Shutdown				
No Card				
Standby				
Card Inserted	0	Hi-Z	0	1
	0	0	0	0
	1	Hi-Z	1	1
	1	0	0	0

- (1) RCLKEN as a logic input in this column. RCLKEN is an I/O pin and it can be driven low externally, left open, or connected to high-impedance terminals, such as the gate of a MOSFET. It must not be driven high externally.
- (2) RCLKEN as a logic output in this column.

POWER STATES

If AUXIN is not present, then all input-to-output power switches are kept off (*OFF* mode).

If AUXIN is present and $\overline{\text{SHDN}}$ is asserted (logic low), then all input-to-output power switches are kept off and the output discharge FETs are turned on (*Shutdown* mode). If $\overline{\text{SHDN}}$ is asserted and then de-asserted, the state on the outputs is restored to the state prior to $\overline{\text{SHDN}}$ assertion.

If 3.3VIN, AUXIN and 1.5VIN are present at the input of the power switch and no card is inserted, then all input-to-output power switches are kept off and the output discharge FETs are turned on (*No Card* mode).

If 3.3VIN, AUXIN and 1.5VIN are present at the input of the power switch prior to a card being inserted, then all input-to-output power switches are turned on once a card-present signal ($\overline{\text{CPUSB}}$ and/or $\overline{\text{CPPE}}$) is detected (*Card Inserted* mode).

If a card is present and all output voltages are being applied, then the $\overline{\text{STBY}}$ is asserted (logic low); the AUXOUT voltage is provided to the card, and the 3.3VOUT and 1.5VOUT switches are turned off (*Standby* mode).

If a card is present and all output voltages are being applied, then the 1.5VIN, or 3.3VIN is removed from the input of the power switch; the AUXOUT voltage is provided to the card and the 3.3VOUT and 1.5VOUT switches are turned off (*Standby* mode).

If prior to the insertion of a card, the AUXIN is available at the input of the power switch and 3.3VIN and/or 1.5VIN are not, or if $\overline{\text{STBY}}$ is asserted (logic low), then no power is made available to the card (*OFF* mode). If 1.5VIN and 3.3VIN are made available at the input of the power switch after the card is inserted and $\overline{\text{STBY}}$ is not asserted, all the output voltages are made available to the card (*Card Inserted* mode).

DISCHARGE FETs

The discharge FETs on the outputs are activated whenever the device detects that a card is not present (*No Card* mode). Activation occurs after the input-to-output power switches are turned off (*break before make*). The discharge FETs de-activate if either of the card-present lines go active low, unless the $\overline{\text{SHDN}}$ pin is asserted.

The discharge FETs are also activated whenever the $\overline{\text{SHDN}}$ input is asserted and stay asserted until $\overline{\text{SHDN}}$ is de-asserted.

PARAMETER MEASUREMENT INFORMATION

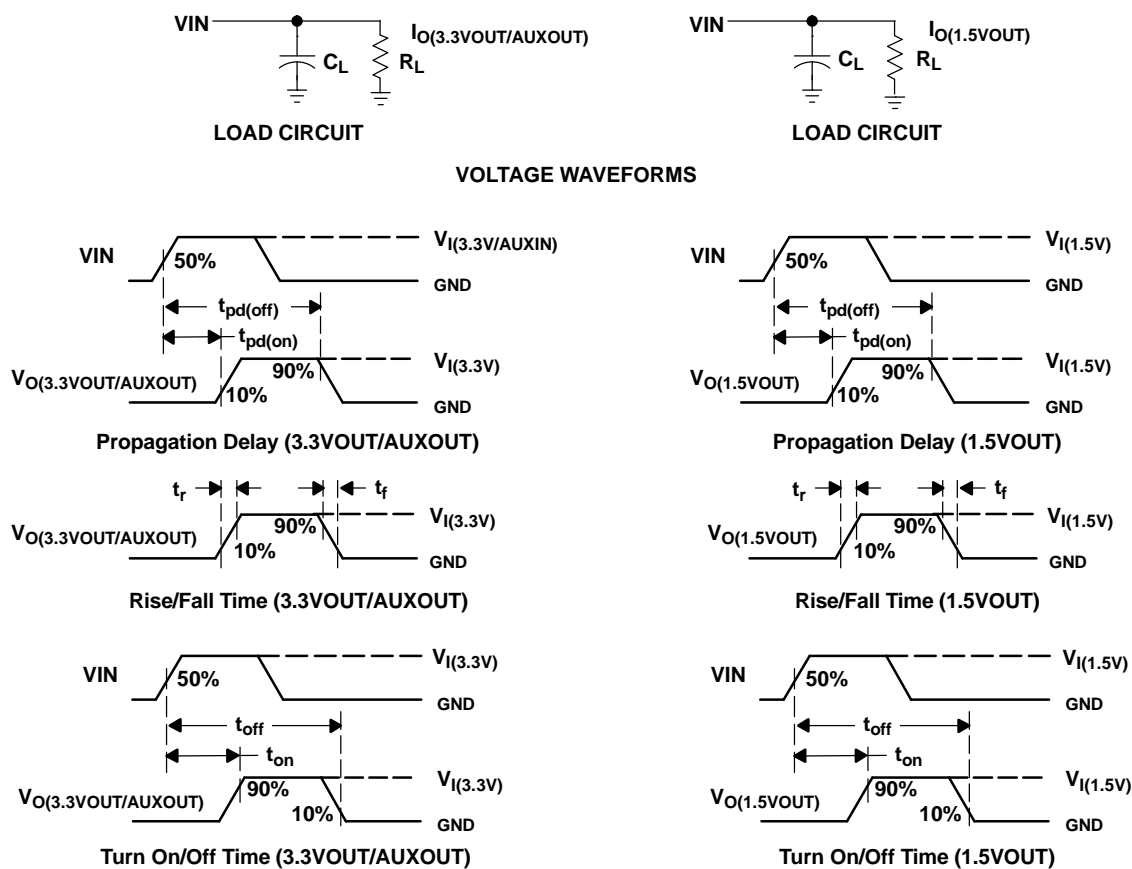


Figure 1. Test Circuits and Voltage Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage when card is inserted	vs Time	2
RCLKEN and $\overline{\text{PERST}}$ voltage during power up	vs Time	3
RCLKEN and $\overline{\text{PERST}}$ voltage during power down	vs Time	4
$\overline{\text{PERST}}$ asserted by $\overline{\text{SYSRST}}$ when power is on	vs Time	5
$\overline{\text{PERST}}$ de-asserted by $\overline{\text{SYSRST}}$ when power is on	vs Time	6
Output voltage when 3.3VIN is removed	vs Time	7
Output voltage when 1.5VIN is removed	vs Time	8
$\overline{\text{OC}}$ response when powered into a short (3.3VOUT)	vs Time	9
Supply current of AUXIN	vs Junction temperature	10
Static drain-source on-state resistance	vs Junction temperature	11
3.3-V power switch current limit	vs Junction temperature	12
1.5-V power switch current limit	vs Junction temperature	13
AUX power switch current limit	vs Junction temperature	14
3.3-V power switch current limit trip	vs Junction temperature	15
1.5-V power switch current limit trip	vs Junction temperature	16
AUX power switch current limit trip	vs Junction temperature	17

OUTPUT VOLTAGE WHEN CARD IS INSERTED
vs
TIME

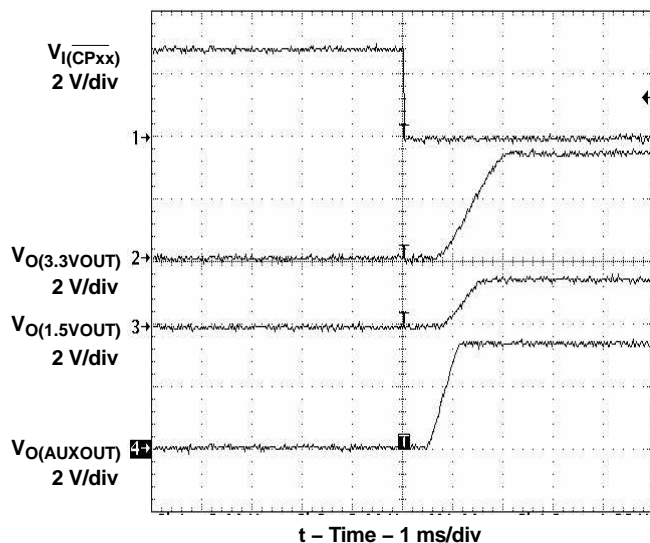


Figure 2.

RCLKEN and $\overline{\text{PERST}}$ VOLTAGE DURING POWER UP
vs
TIME

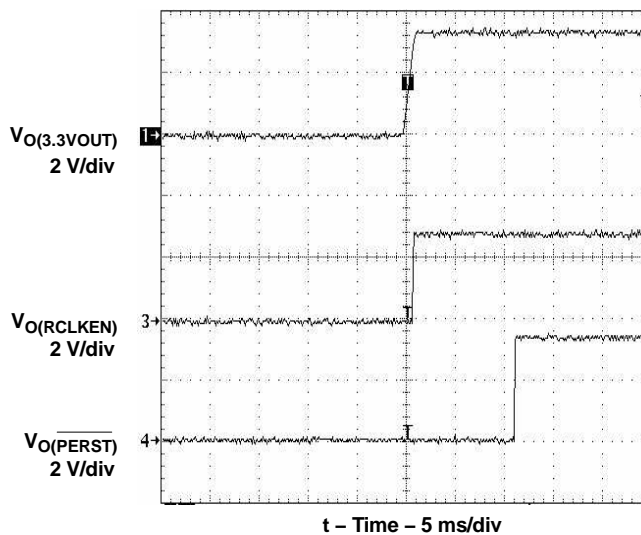


Figure 3.

RCLKEN AND $\overline{\text{PERST}}$ VOLTAGE DURING POWER DOWN

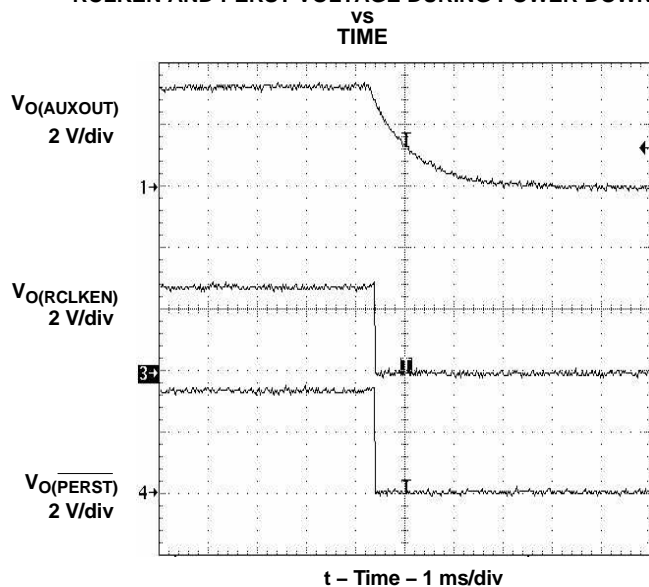


Figure 4.

$\overline{\text{PERST}}$ ASSERTED BY $\overline{\text{SYSRST}}$ WHEN POWER IS ON

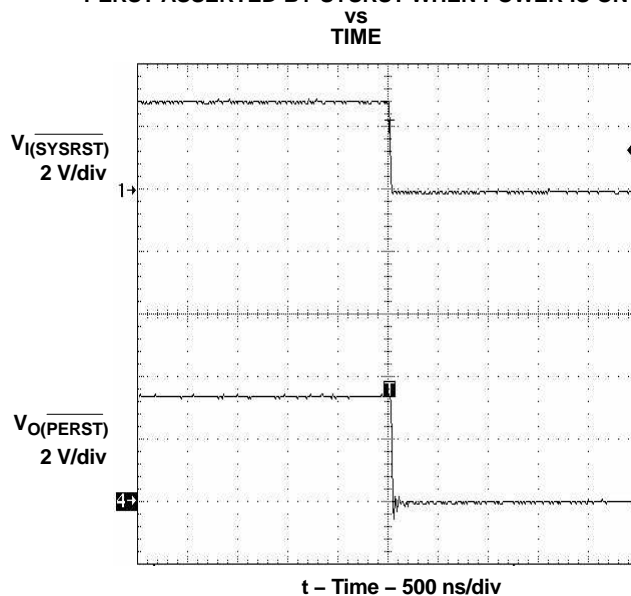


Figure 5.

$\overline{\text{PERST}}$ DE-ASSERTED BY $\overline{\text{SYSRST}}$ WHEN POWER IS ON

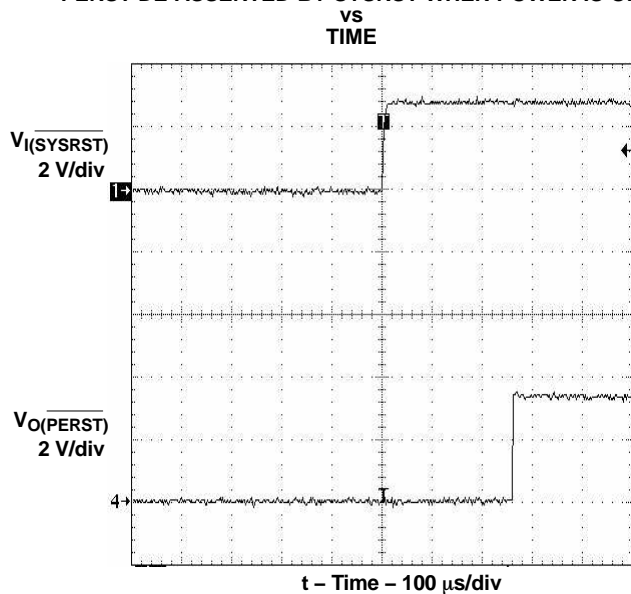


Figure 6.

OUTPUT VOLTAGE WHEN 3.3VIN IS REMOVED

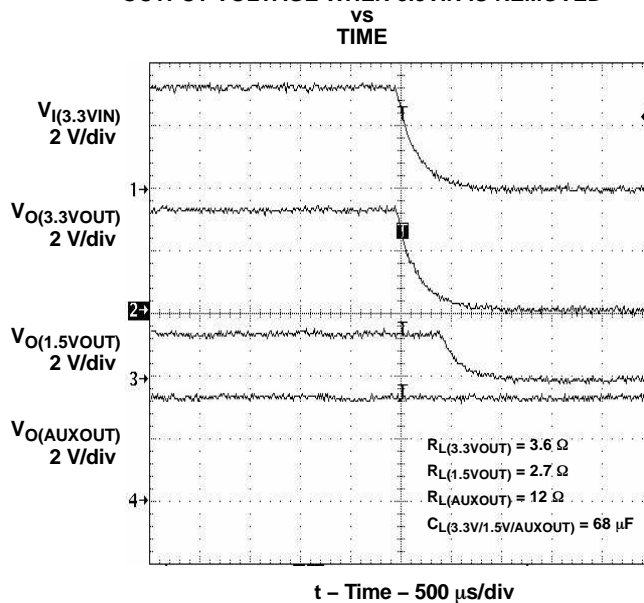


Figure 7.

OUTPUT VOLTAGE WHEN 1.5VIN IS REMOVED
vs
TIME

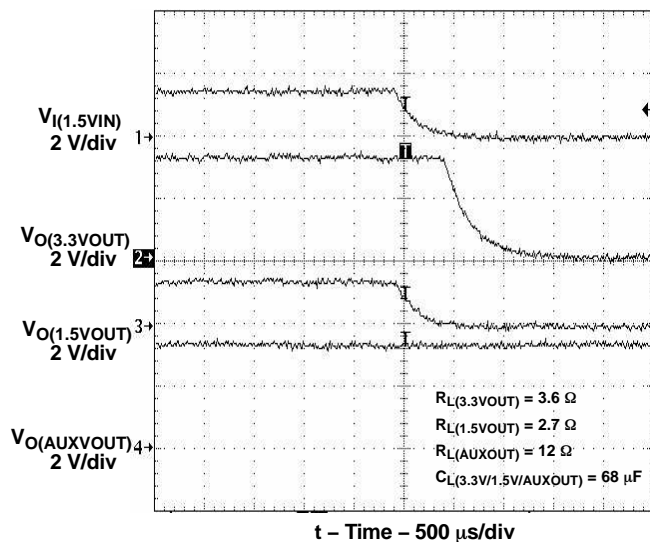


Figure 8.

\overline{OC} RESPONSE WHEN POWERED INTO A SHORT
(3.3VOUT)
vs
TIME

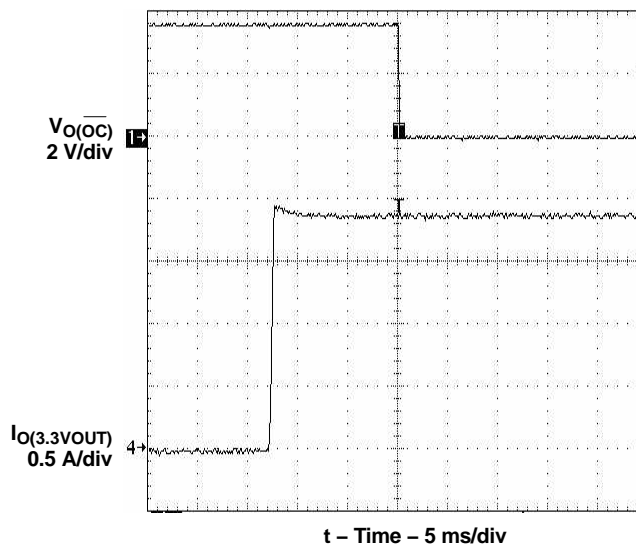


Figure 9.

SUPPLY CURRENT OF AUXIN
vs
JUNCTION TEMPERATURE

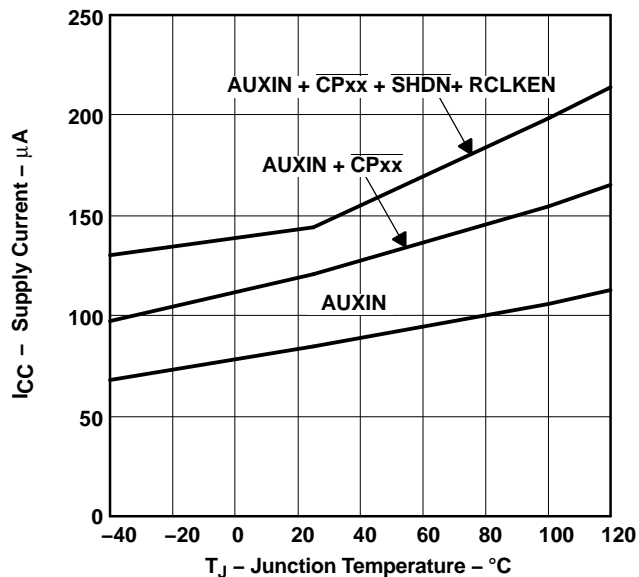


Figure 10.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

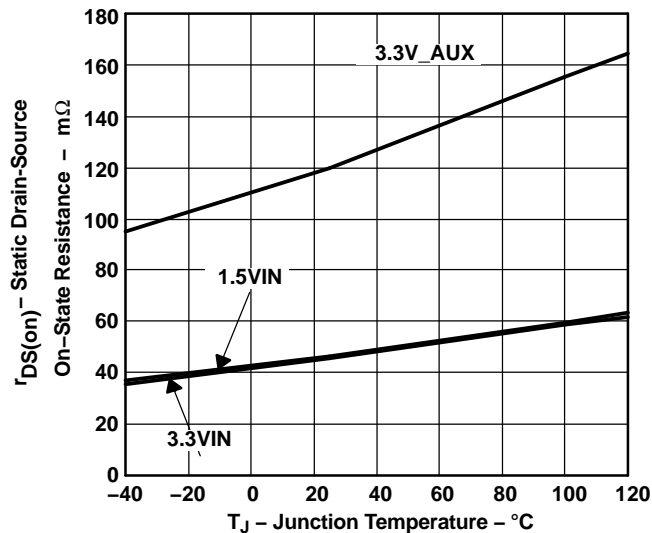


Figure 11.

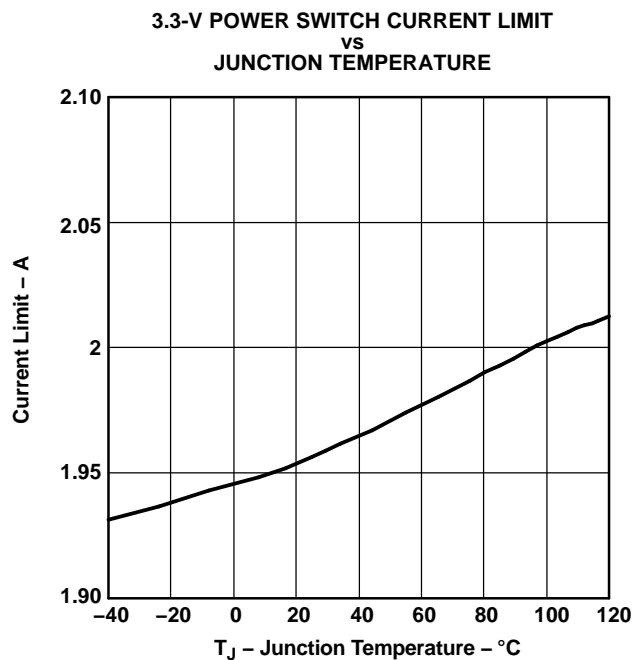


Figure 12.

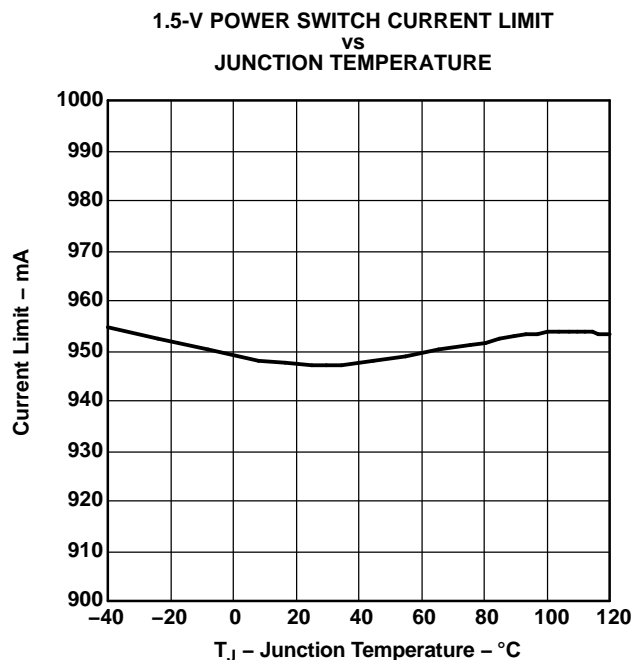


Figure 13.

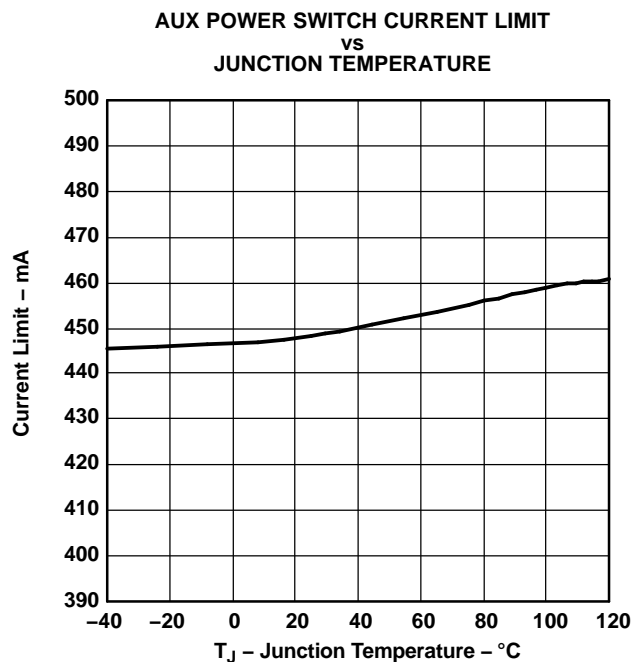


Figure 14.

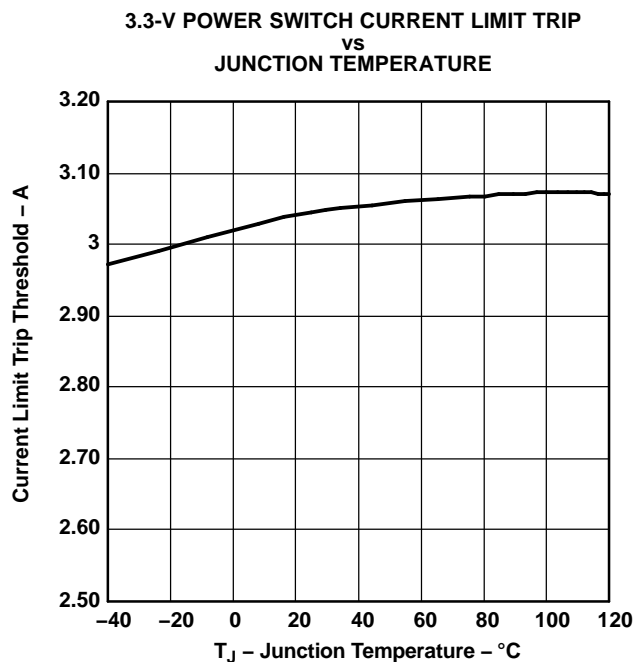


Figure 15.

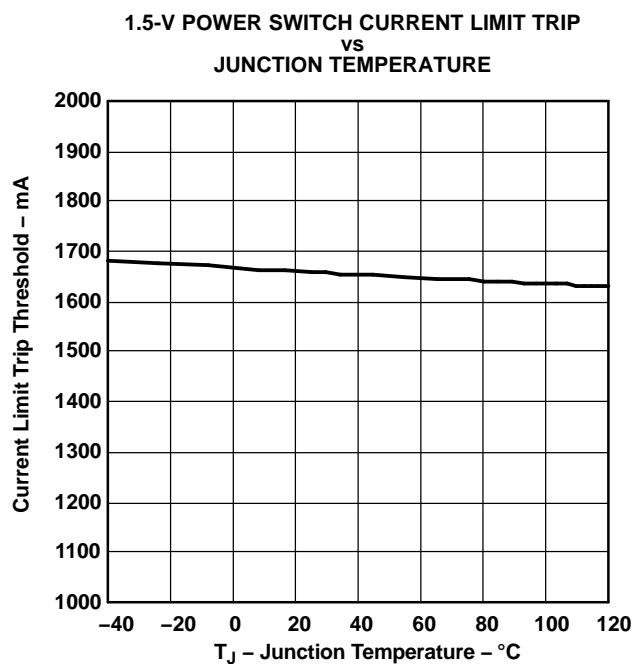


Figure 16.

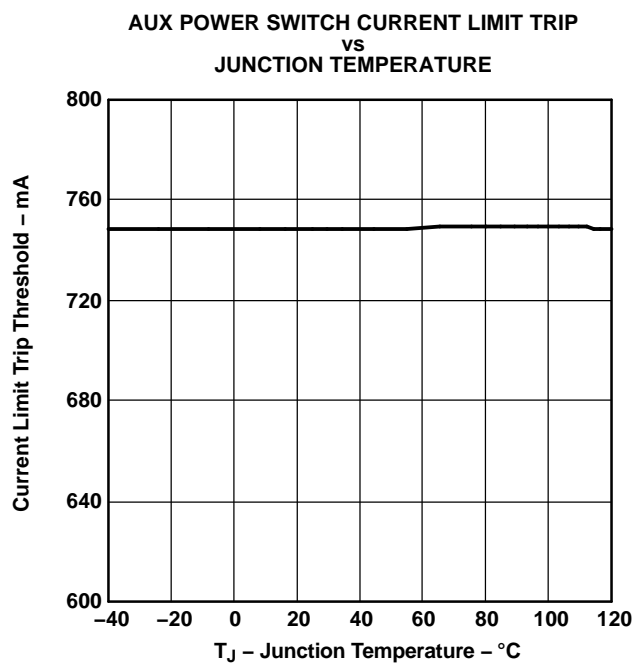


Figure 17.

APPLICATION INFORMATION

INTRODUCTION TO ExpressCard

An ExpressCard module is an add-in card with a serial interface based on PCI Express and/or Universal Serial Bus (USB) technologies. An ExpressCard comes in two form factors defined as ExpressCard|34 or ExpressCard|54. The difference, as defined by the name, is the width of the module, 34 mm or 54 mm, respectively. Host systems supporting the ExpressCard module can support either the ExpressCard|34 or ExpressCard|54 or both.

ExpressCard POWER REQUIREMENTS

Regardless of which ExpressCard module is used, the power requirements as defined in the ExpressCard Standard apply to both on an individual slot basis. The host system is required to supply 3.3 V, 1.5 V, and AUX to each of the ExpressCard slots. However, the voltage is only applied after an ExpressCard is inserted into the slot.

The ExpressCard connector has two pins, $\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$, that are used to signal the host when a card is inserted. If the ExpressCard module itself connects the $\overline{\text{CPPE}}$ to ground, the logic low level on that signal indicates to the host that a card supporting PCI Express has been inserted. If $\overline{\text{CPUSB}}$ is connected to ground, then the ExpressCard module supports the USB interface. If both PCI Express and USB are supported by the ExpressCard module, then both signals, $\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$, must be connected to ground.

In addition to the Card Present signals ($\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$), the host system determines when to apply power to the ExpressCard module based on the state of the system. The state of the system is defined by the state of the 3.3 V, 1.5 V, and AUX input voltage rails. For the sake of simplicity, the 3.3-V and 1.5-V rails are defined as the primary voltage rails as oppose to the auxiliary voltage rail, AUX.

ExpressCard POWER SWITCH OPERATION

The ExpressCard power switch resides on the host, and its main function is to control when to send power to the ExpressCard slot. The ExpressCard power switch makes decisions based on the Card Present inputs and on the state of the host system as defined by the primary and auxiliary voltage rails.

The following conditions define the operation of the host power controller:

1. When both primary power and auxiliary power at the input of the ExpressCard power switch are off, then all power to the ExpressCard connector is off regardless of whether a card is present.
2. When both primary power and auxiliary power at the input of the ExpressCard power switch are on, then power is only applied to the ExpressCard after the ExpressCard power switch detects that a card is present.
3. When primary power (either +3.3 V or +1.5 V) at the input of the ExpressCard power switch is off and auxiliary power at the input of the ExpressCard power switch is on, then the ExpressCard power switch behaves in the following manner:
 - a. If neither of the Card Present inputs is detected (no card inserted), then no power is applied to the ExpressCard slot.
 - b. If the card is inserted after the system has entered this power state, then no power is applied to the ExpressCard slot.
 - c. If the card is inserted prior to the removal of the primary power (either +3.3 V or +1.5 V or both) at the input of the ExpressCard power switch, then only the primary power (both +3.3 V and +1.5 V) is removed and the auxiliary power is sent to the ExpressCard slot.

Figure 18 through Figure 23 illustrate the timing relationships between power/logic inputs and outputs of ExpressCard.

APPLICATION INFORMATION (continued)

EXPRESS CARD TIMING DIAGRAMS

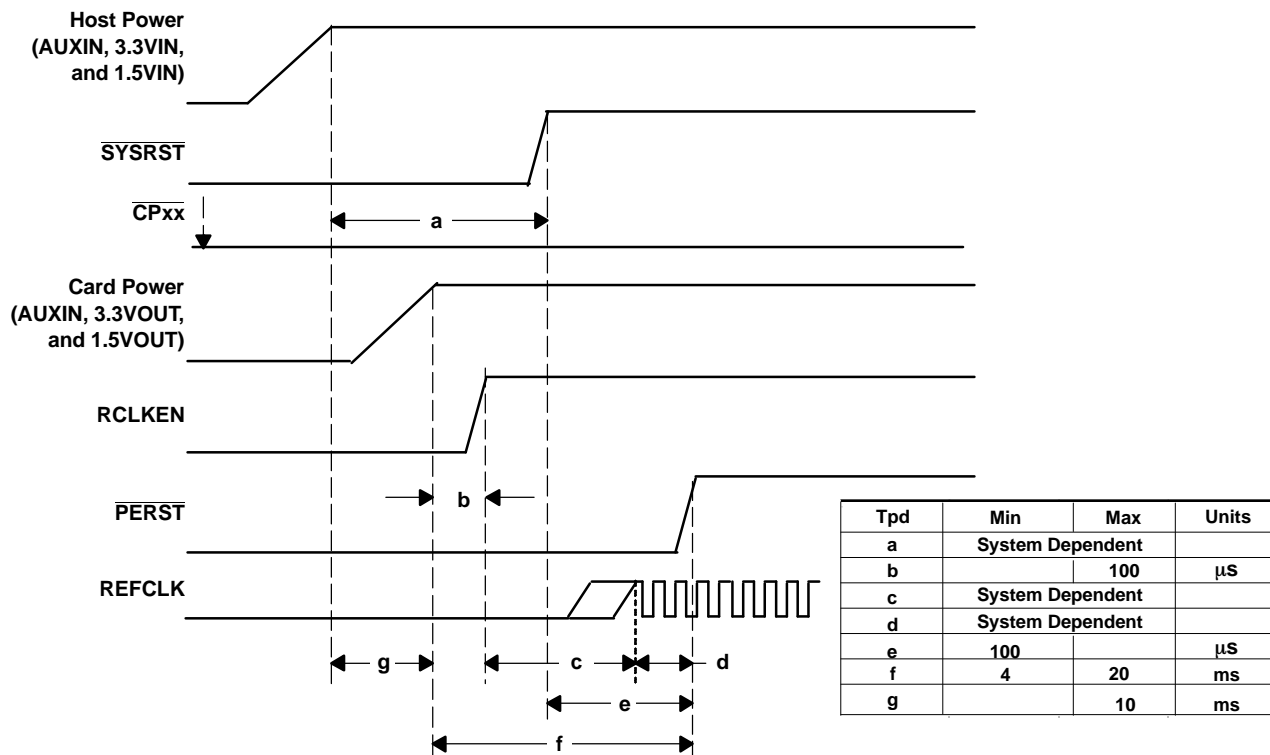


Figure 18. Timing Signals - Card Present Before Host Power Is On

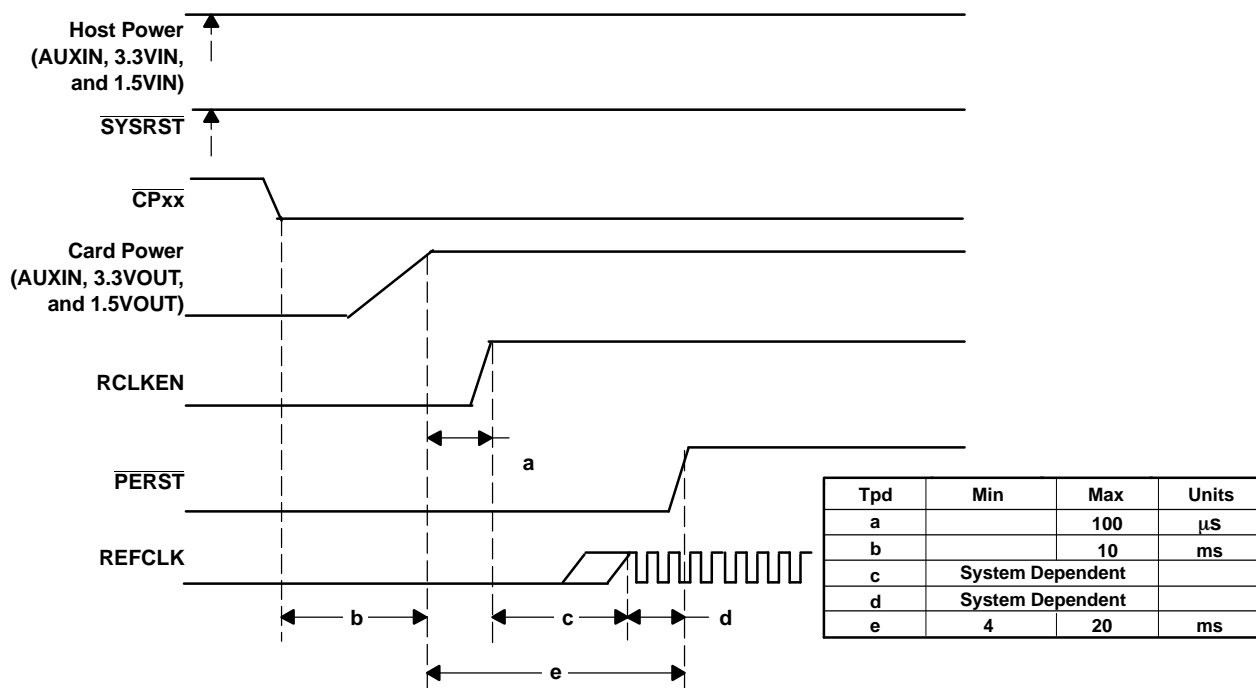
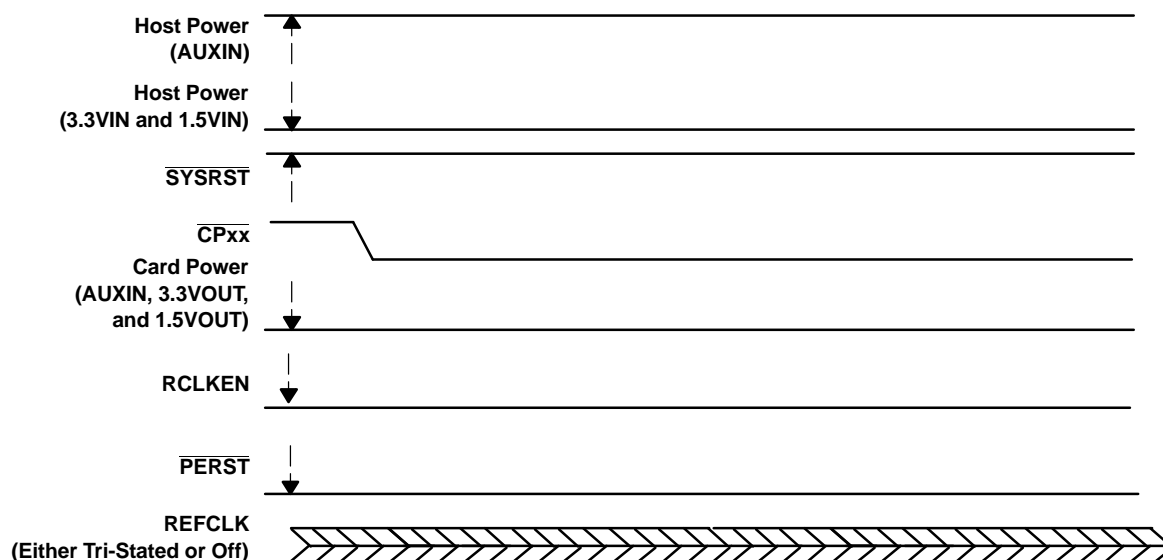


Figure 19. Timing Signals - Host Power Is On Prior to Card Insertion

APPLICATION INFORMATION (continued)



Note: Once 3.3 V and 1.5 V are applied, the power switch follows the power-up sequence of Figure 18 or Figure 19.

Figure 20. Timing Signals - Host System In Standby Prior to Card Insertion

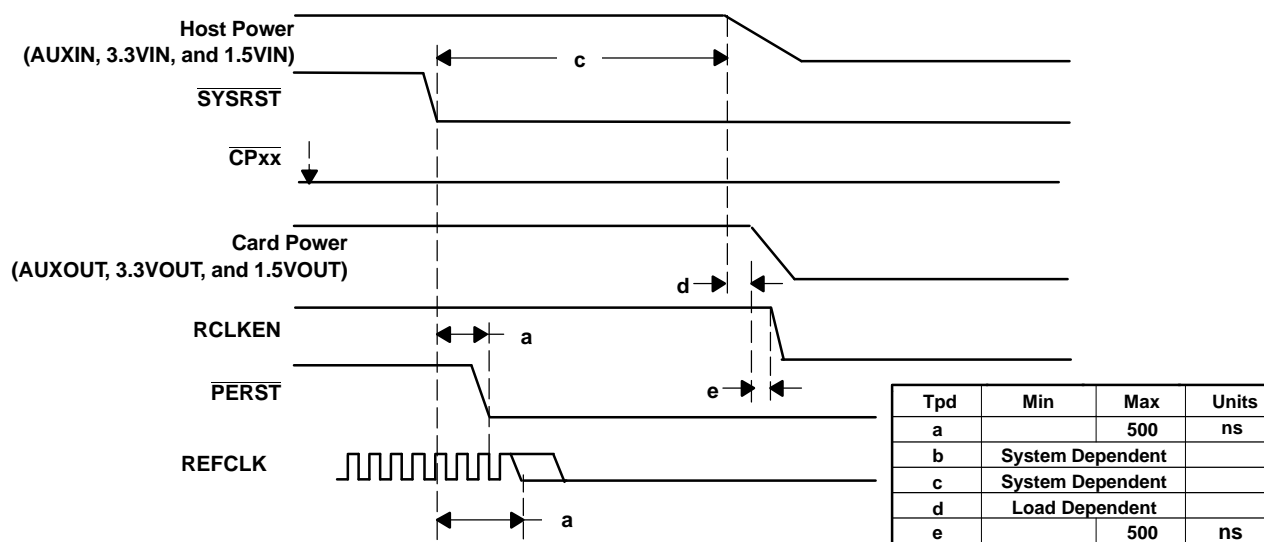


Figure 21. Timing Signals - Host-Controlled Power Down

APPLICATION INFORMATION (continued)

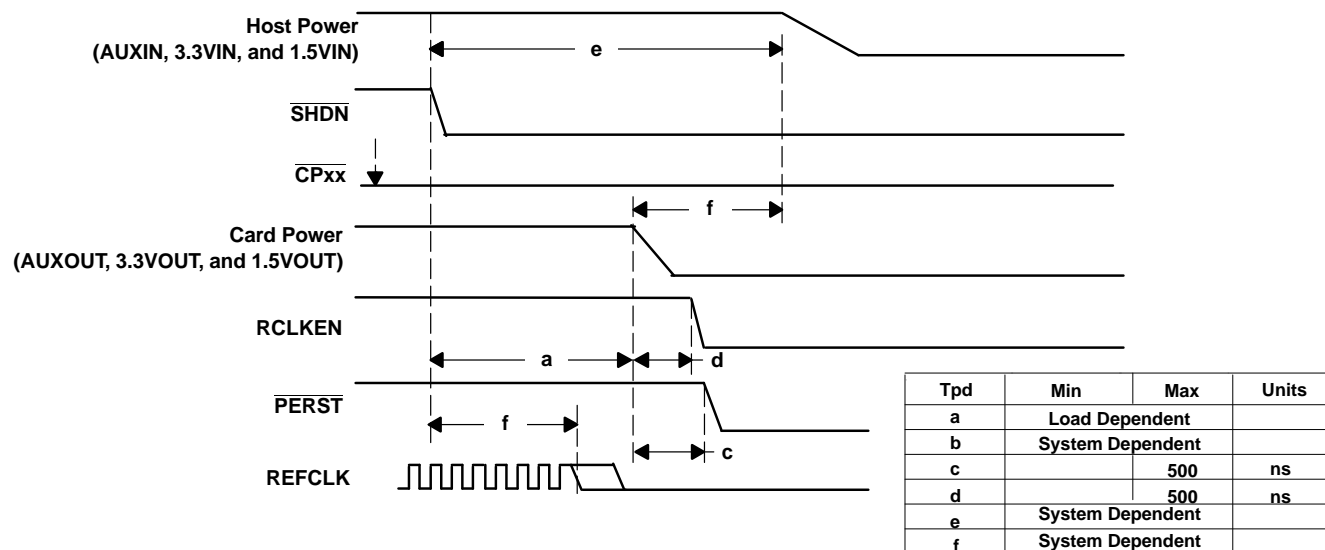


Figure 22. Timing Signals - Controlled Power Down When $\overline{\text{SHDN}}$ Asserted

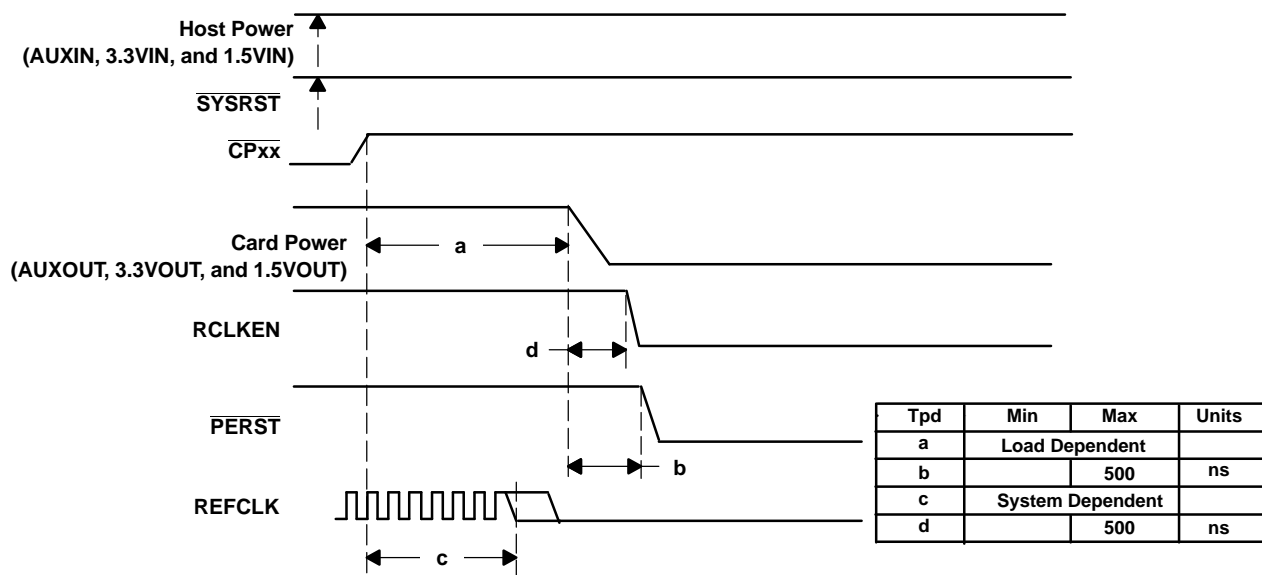
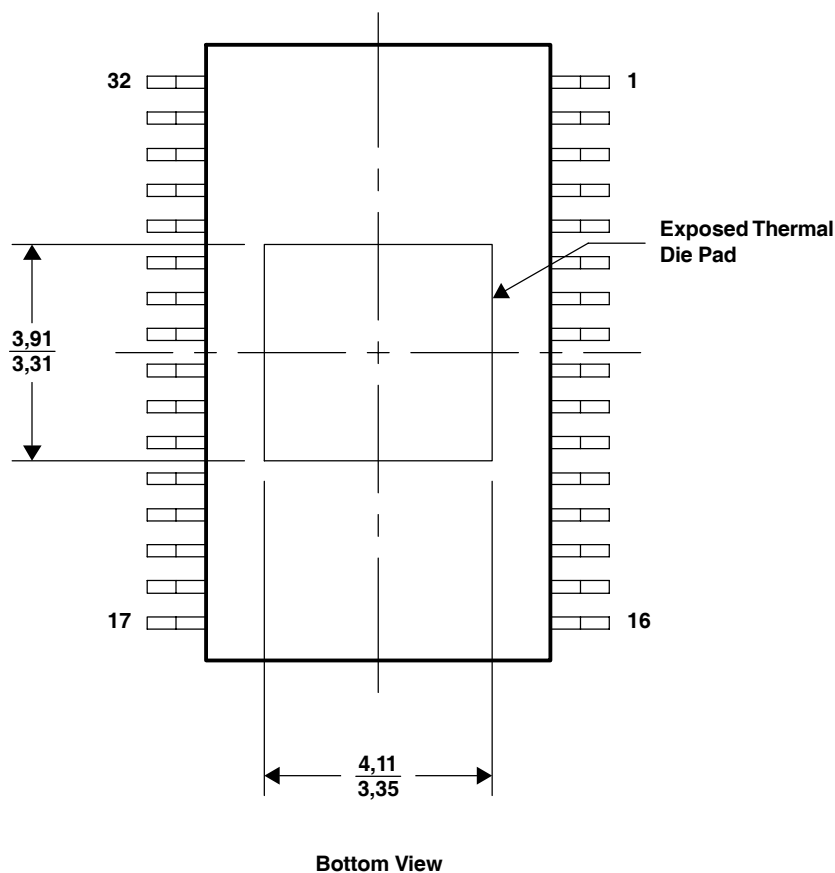


Figure 23. Timing Signals - Surprise Card Removal

THERMAL INFORMATION

The DAP PowerPAD™ package incorporates an exposed thermal die pad that is designed to be attached directly to an external heat sink. When the thermal die pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal die pad can be attached directly to a ground plane or special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com. See Figure 1 for DAP package exposed thermal die pad dimensions.



PPTD001

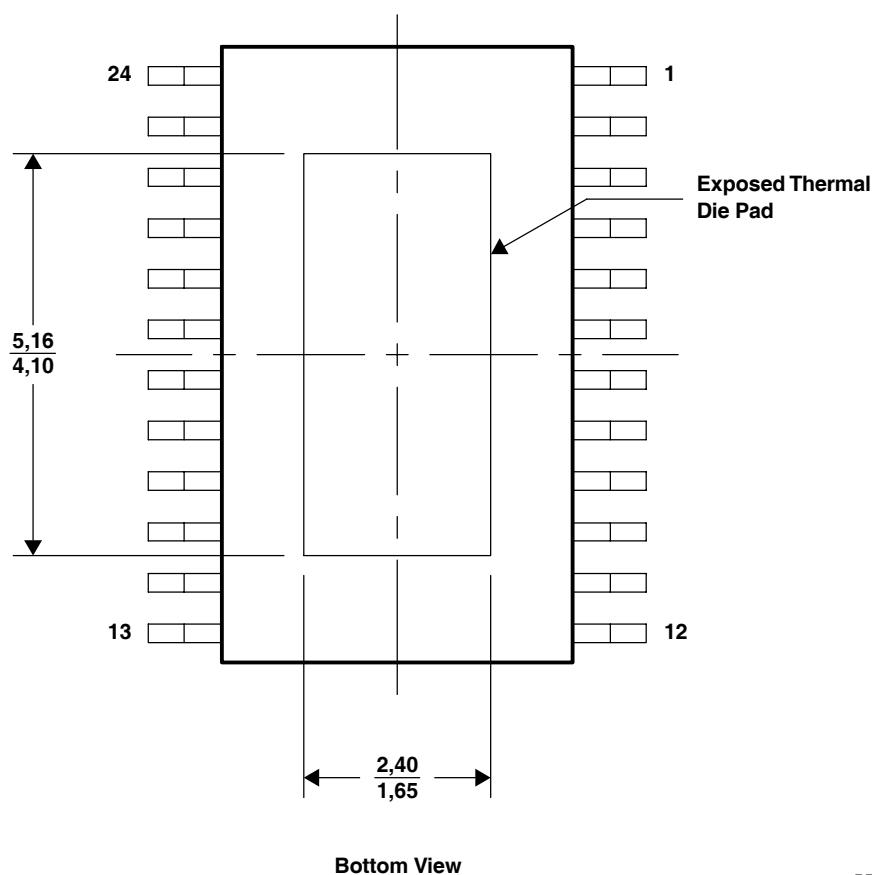
NOTE: All linear dimensions are in millimeters.

Figure 1. DAP Package Exposed Thermal Die Pad Dimensions

THERMAL INFORMATION

The PWP PowerPAD™ package incorporates an exposed thermal die pad that is designed to be attached directly to an external heat sink. When the thermal die pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal die pad can be attached directly to a ground plane or special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com. See Figure 1 for PWP package exposed thermal die pad dimensions.



PPTD031

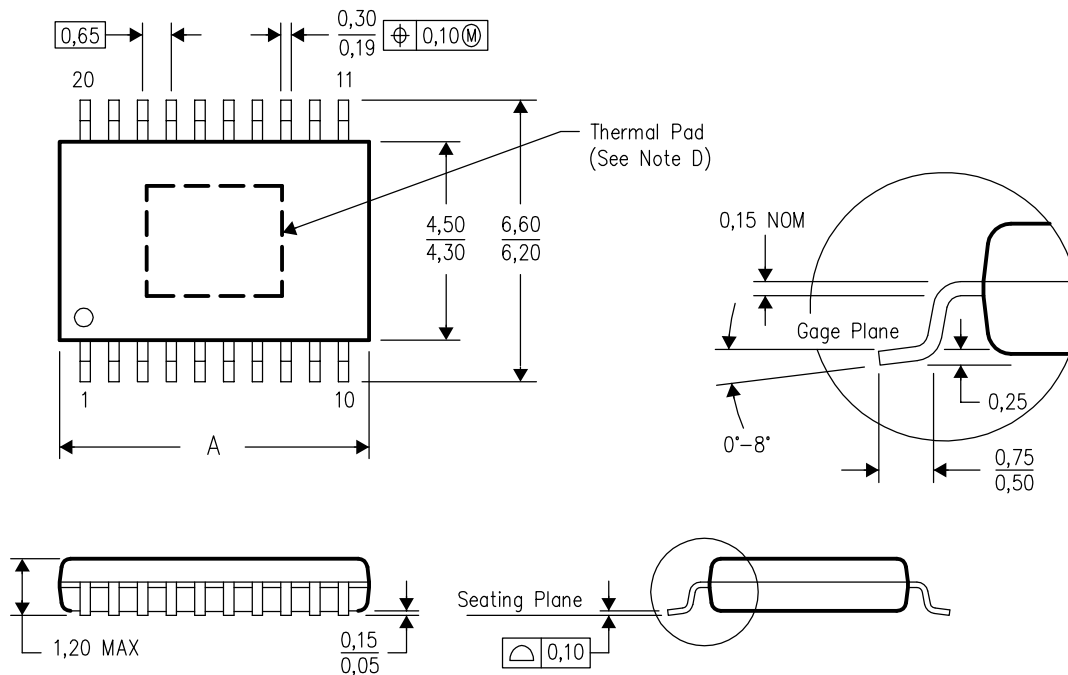
NOTE: All linear dimensions are in millimeters.

Figure 1. PWP Package Exposed Thermal Die Pad Dimensions

PWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



PINS **	14	16	20	24	28
DIM					
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

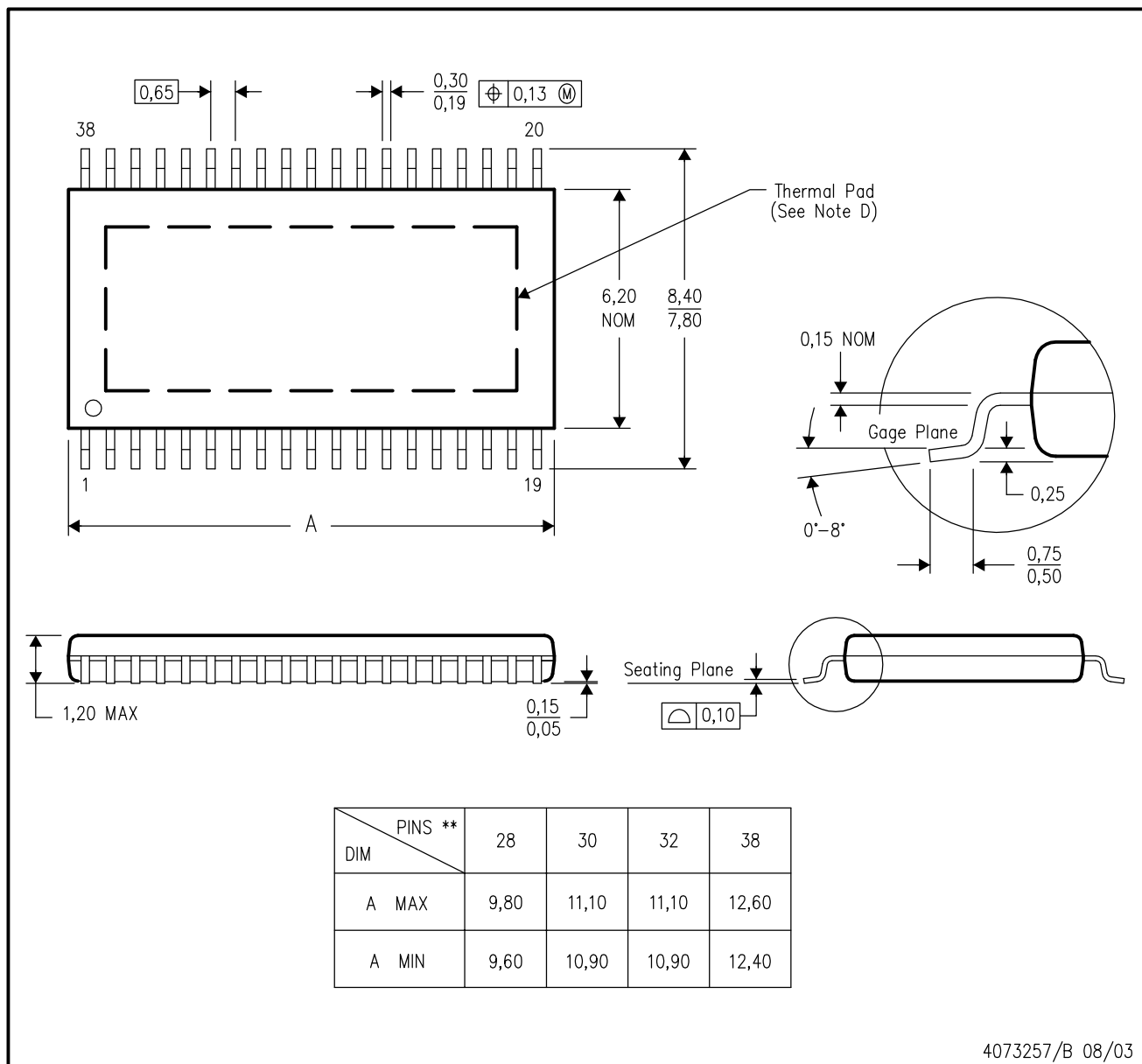
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

DAP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

38 PINS SHOWN



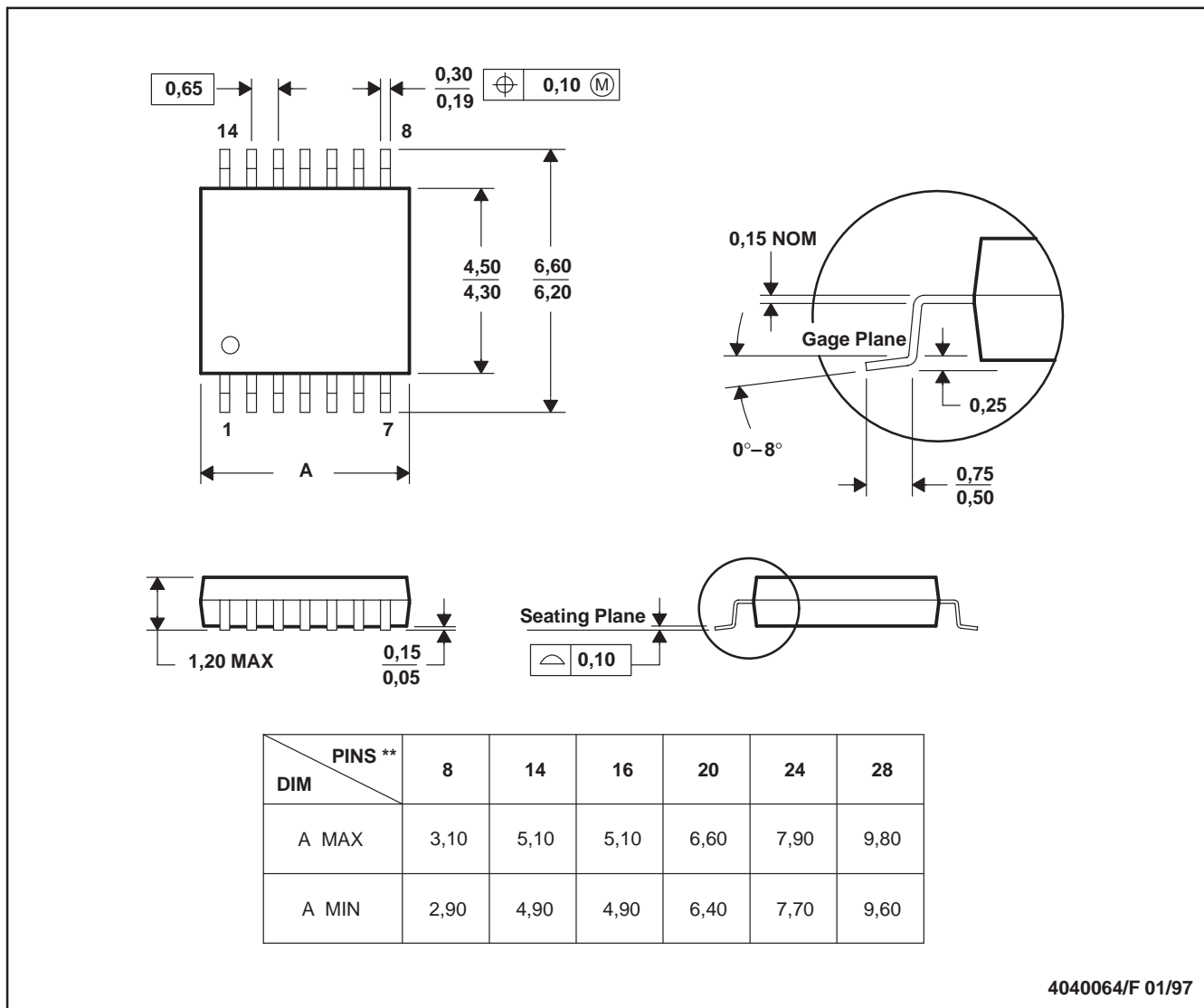
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated