S29WSxxxN MirrorBit™ Flash Family

S29WS256N, S29WS128N, S29WS064N

256/128/64 Megabit (16/8/4 M x 16-Bit) CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memory

SPANSION™

PRELIMINARY

Distinctive Characteristics

Architectural Advantages

- **Single 1.8 volt read, program and erase (1.70 to 1.95 volt)**
- **Manufactured on 110 nm MirrorBit™ process technology**
- **VersatileIO™ (V_{IO}) Feature**
  - Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{IO} pin
  - V_{IO} options available for 1.8 V (1.70 V – 1.95 V)
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency between read and write operations
  - Sixteen bank architecture: Each bank consists of 16Mb (WS256N) / 8Mb (WS128N) / 4Mb (WS064N)
- **Programable Burst Interface**
  - 2 Modes of Burst Read Operation
  - Linear Burst: 32, 16, and 8 words with or without wrap-around
  - Continuous Sequential Burst
- **SecSi™ (Secured Silicon) Sector region**
  - 256 words accessible through a command sequence, 128 words for the Factory SecSi Sector and 128 words for the Customer SecSi Sector.
  - Non-erasable region
- **Sector Architecture**
  - S29WS256N: Eight 16 Kword sectors and two-hundred-fifty-four 64 Kword sectors
  - S29WS128N: Eight 16 Kword sectors and one-hundred-twenty-six 64 Kword sectors
  - S29WS064N: Eight 16 Kword sectors and sixty-two 64 Kword sectors
  - Banks 0 and 15 each contain 16 Kword sectors and 64 Kword sectors; Other banks each contain 64 Kword sectors
  - Eight 16 Kword boot sectors, four at the top of the address range, and four at the bottom of the address range
- **Cycling Endurance: 100,000 cycles per sector typical**
- **Data Retention: 20 years typical**
- **MCP-Compatible Packages**
  - 84-ball (8 mm x 11.6 mm) FBGA package for WS256N
  - 84-ball (8 mm x 11.6 mm) FBGA package for WS128N
  - 80-ball (7 mm x 9 mm) FBGA package for WS064N

Performance Characteristics

- **Read access times at 80/66/54 MHz**
  - Burst access times of 9/11.2/13.5 ns
  - Synchronous initial latency of 69/69/69 ns
  - Asynchronous random access times of 70/70/70 ns
- **Program and Erase Performance**
  - Typical word programming time of 40 µs
  - Typical effective word programming time of 9.4 µs utilizing a 32-Word Write Buffer at V_{CC} Level
  - Typical effective word programming time of 6 µs utilizing a 32-Word Write Buffer at ACC Level
  - Typical sector erase time of 150 ms for 16 Kword sectors and 800 ms sector erase time for 64 Kword sectors
- **Power dissipation (typical values @ 66 MHz)**
  - Continuous Burst Mode Read: 35 mA
  - Simultaneous Operation: 50 mA
  - Program: 19 mA
  - Erase: 19 mA
  - Standby mode: 20 µA

Hardware Features

- **Sector Protection**
  - Write protect (WP#) function allows protection of eight outermost boot sectors, four at top and four at bottom of memory, regardless of sector protect status
- **Handshaking feature available**
  - Provides host system with minimum possible latency by monitoring RDY
- **Boot Option**
  - Dual Boot
- **Low V_{CC} write inhibit**

Security Features

- **Advanced Sector Protection consists of the two following modes of operation**
- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level

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- **Password Sector Protection**
  — A sophisticated sector protection method to lock combinations of individual sectors to prevent program or erase operations within that sector using a user-defined 64-bit password

Software Features

- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
- **Data# Polling and toggle bits**
  — Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Program Suspend/Resume**
  — Suspends a programming operation to read data from a sector other than the one being programmed, then resume the programming operation
- **Unlock Bypass Program command**
  — Reduces overall programming time when issuing multiple program command sequences

Additional Features

- **Program Operation**
  — Ability to perform synchronous and asynchronous program operation independent of burst control register setting
- **ACC input**
  — Acceleration function reduces programming and erase time in a factory setting.

General Description

The WSxxxN family consists of 256, 128, and 64 Mbit, 1.8 Volt-only, simultaneous Read/Write, Burst Mode Flash memory devices, organized as 16, 8, or 4 Mwords of 16 bits. These devices use a single V_{CC} of 1.70 to 1.95 V to read, program, and erase the memory array. A 9.0-volt V_{HH} on ACC may be used for faster program performance in a factory setting. These devices can be programmed in standard EPROM programmers.

At 80 MHz and 1.8V V_{IO}, the device provides a burst access of 9 ns at 30 pF with an initial latency of 69 ns at 30 pF. At 66 MHz and 1.8V V_{IO}, the device provides a burst access of 11.2 ns at 30 pF with an initial latency of 69 ns at 30 pF. At 54 MHz and 1.8V V_{IO}, the device provides a burst access of 13.5 ns at 30 pF with an initial latency of 69 ns at 30 pF. The device operates within the industrial temperature range of -40°C to +85°C or wireless temperature range of -25°C to +85°C. These devices are offered in MCP compatible FBGA packages. See the product selector guide for details

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into sixteen banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The devices are divided into banks and sectors as shown in the following table:

Bank	Quantity of Sectors (WS256N/WS128N/WS064N)	Sector Size
0	4/4/4	16 Kwords
	15/7/3	64 Kwords
1	16/8/4	64 Kwords
2	16/8/4	64 Kwords
3	16/8/4	64 Kwords
4	16/8/4	64 Kwords
5	16/8/4	64 Kwords
6	16/8/4	64 Kwords
7	16/8/4	64 Kwords
8	16/8/4	64 Kwords
9	16/8/4	64 Kwords
10	16/8/4	64 Kwords
11	16/8/4	64 Kwords
12	16/8/4	64 Kwords
13	16/8/4	64 Kwords
14	16/8/4	64 Kwords
15	15/7/3	64 Kwords
	4/4/4	16 Kwords

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin.

The device uses Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the device additionally requires Ready (RDY), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

The burst read mode feature gives system designers flexibility in the interface to the device. The user can preset the burst length and then wrap or non-wrap through the same memory space, or read the flash array in continuous mode.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** Algorithm — an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster program times by requiring only two write cycles to program data instead of four. The additional **Write Buffer Programming** feature provides superior programming performance by grouping locations being programmed.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** Algorithm — an internal algorithm that automatically preprograms the array (if it is not already fully programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The **Program Suspend/Program Resume** feature enables the user to put program on hold to read data from any sector that is not selected for programming. If a read is needed from the SecSi Sector area, Persistent Protection area, Dynamic Protection area, or the CFI area, after an program suspend, then the user must use the proper command sequence to enter and exit this region. The program suspend/resume functionality is also available when programming in erase suspend (1 level depth only).

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the SecSi Sector area, Persistent Protection area, Dynamic Protection area, or the CFI area, after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The host system can detect whether a memory array program or erase operation is complete by using the device status bit DQ7 (Data# Polling), DQ6/DQ2 (toggle bits), DQ5 (exceeded timing limit), DQ3 (sector erase start timeout state indicator), and DQ1 (write to buffer abort). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. ***The device is fully erased when shipped from the factory***.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers two types of data protection at the sector level. When at V_{IL}, **WP#** locks the four outermost boot sectors at the top of memory and the four outermost boot sectors at the bottom of memory.

When the ACC pin = V_{IL}, the entire flash memory array is protected.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

Spansion™ Flash memory products combine years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector. The data is programmed using hot electron injection.

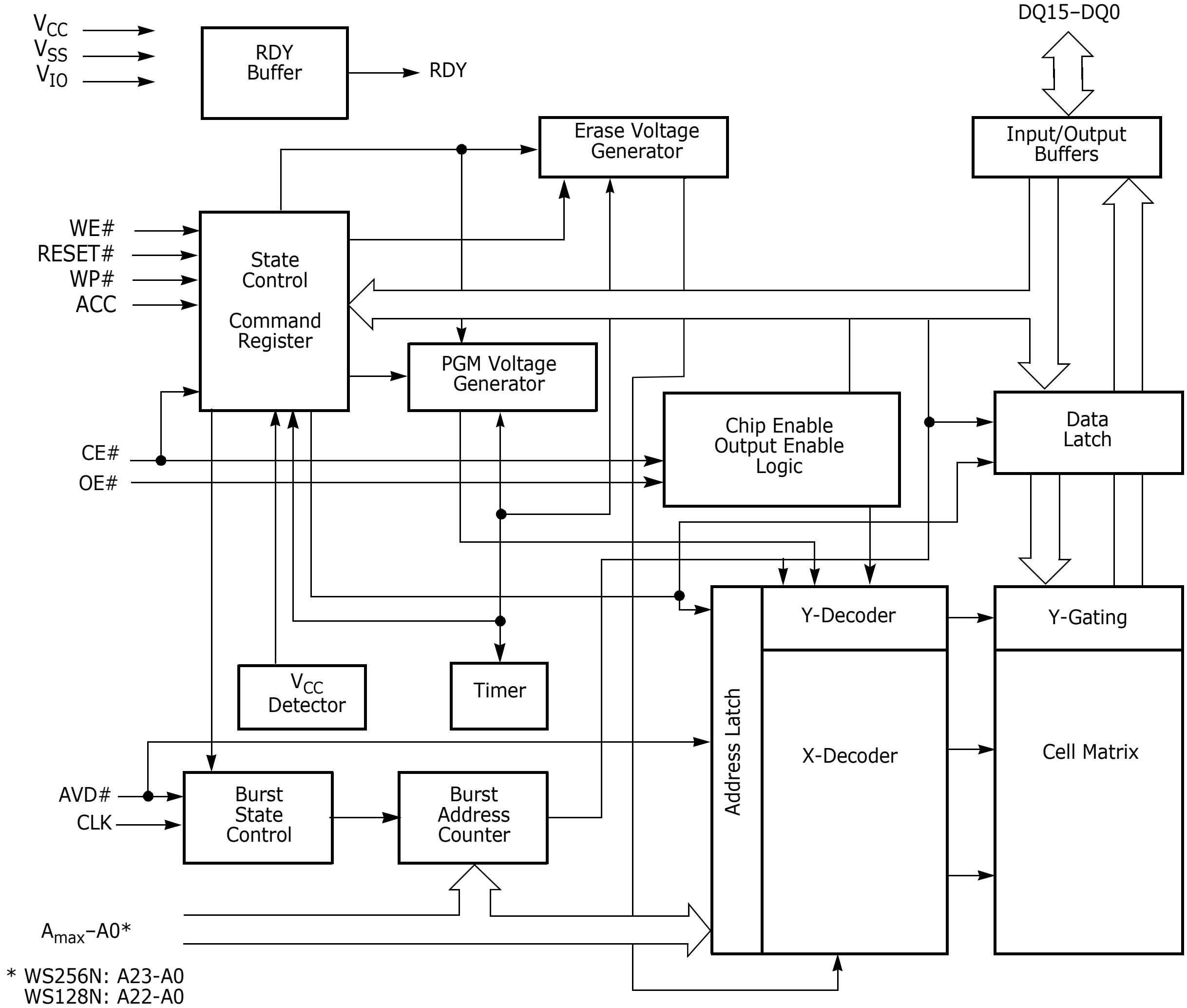
Table of Contents

Product Selector Guide

Part Number	S29WS256N, S29WS128N, S29WS064N		
Speed Option (Burst Frequency) (See Note)	**80 MHz**	**66 MHz**	**54 MHz**
Max Synchronous Latency, ns (t_{IACC})	69	69	69
Max Synchronous Burst Access Time, ns (t_{BACC})	9	11.2	13.5
Max Asynchronous Access Time t_{CE}), ns	70	70	70
Max CE# Access Time, ns (t_{CE}), ns	70	70	70
Max OE# Access Time, ns (t_{OE})	11.2	11.2	13.5

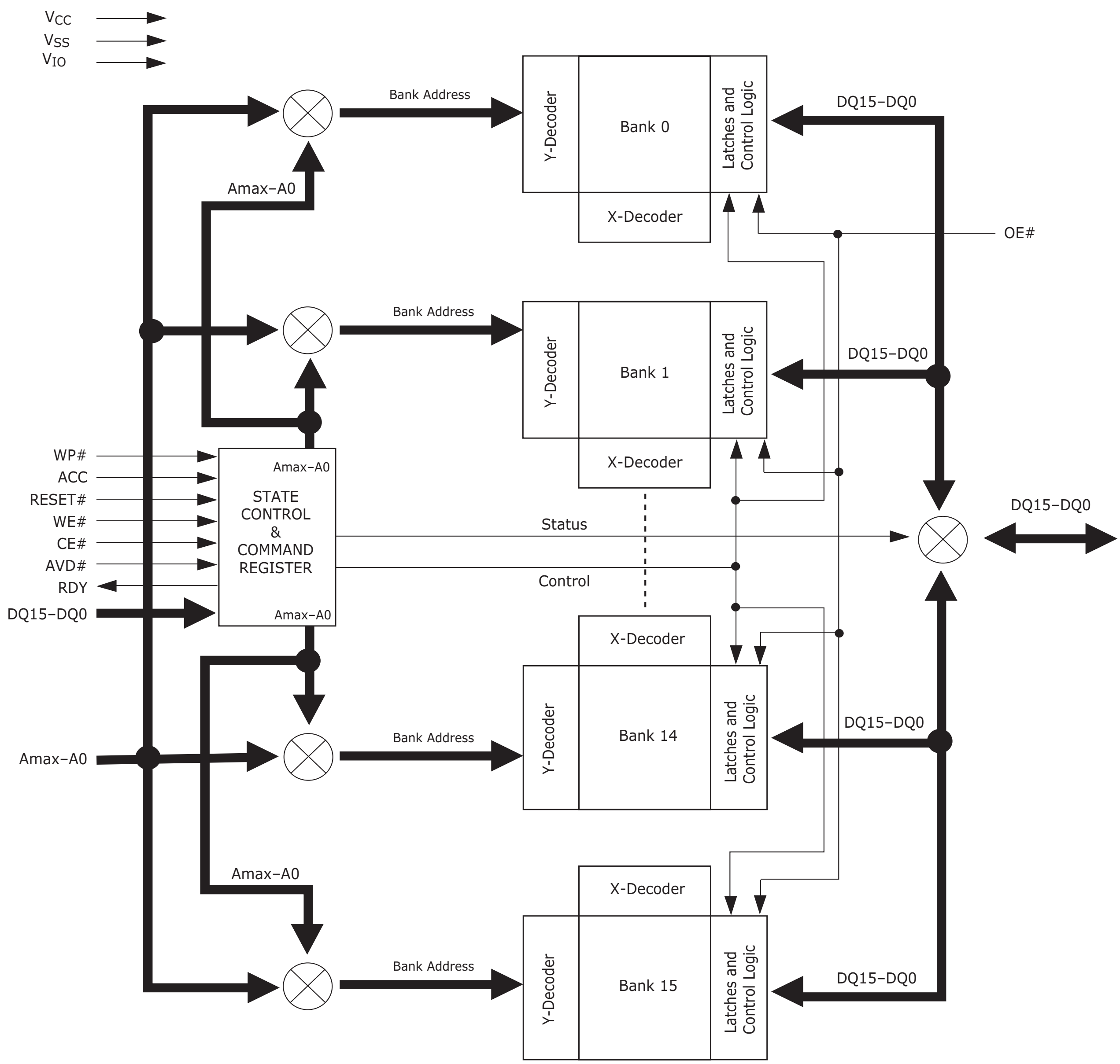
***Note:** 80 MHz available for standalone applications only, 66 MHz and 54 MHz available for both multi-chip and standalone applications.*

Block Diagram



* WS256N: A23-A0
WS128N: A22-A0
WS064N: A21-A0

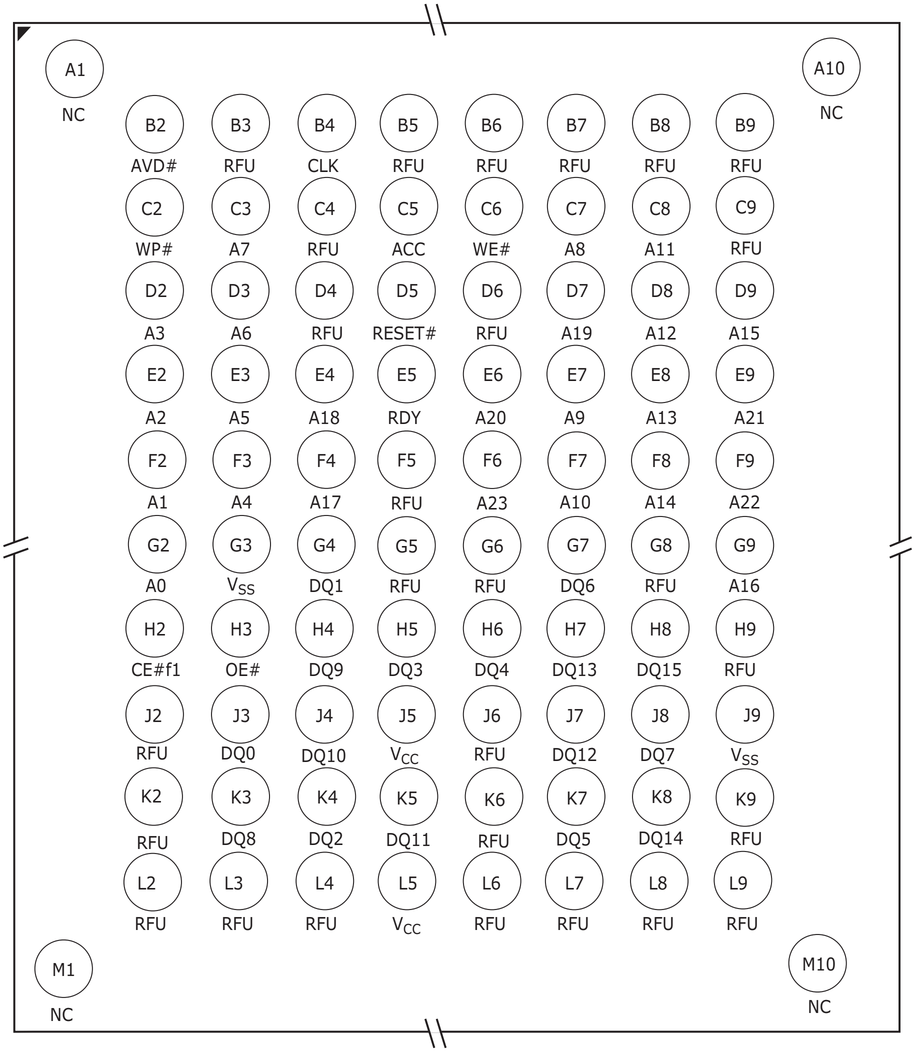
Block Diagram of Simultaneous Operation Circuit



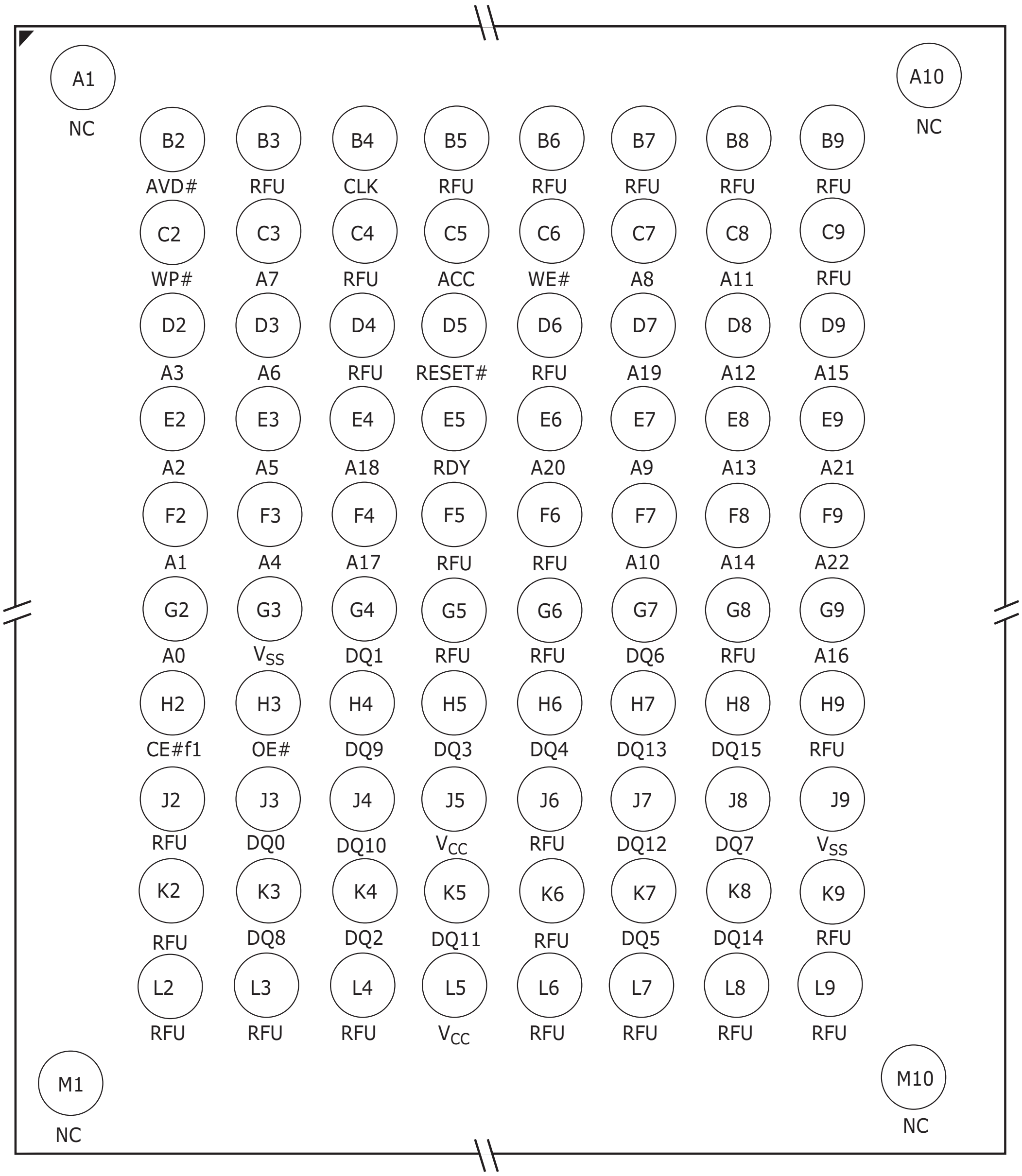
Note: *Amax=A23 for the WS256N, A22 for the WS128N, and A21 for the WS064N.*

Connection Diagrams

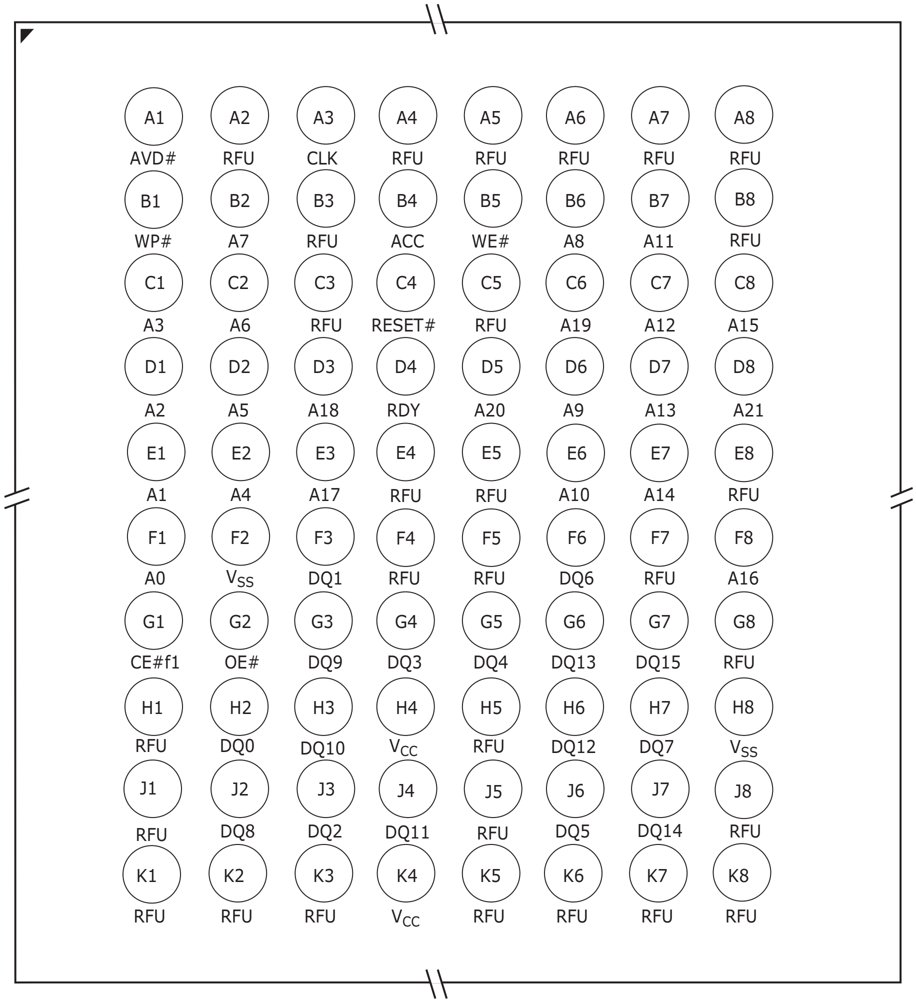
S29WS256N–MCP Compatible
84-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



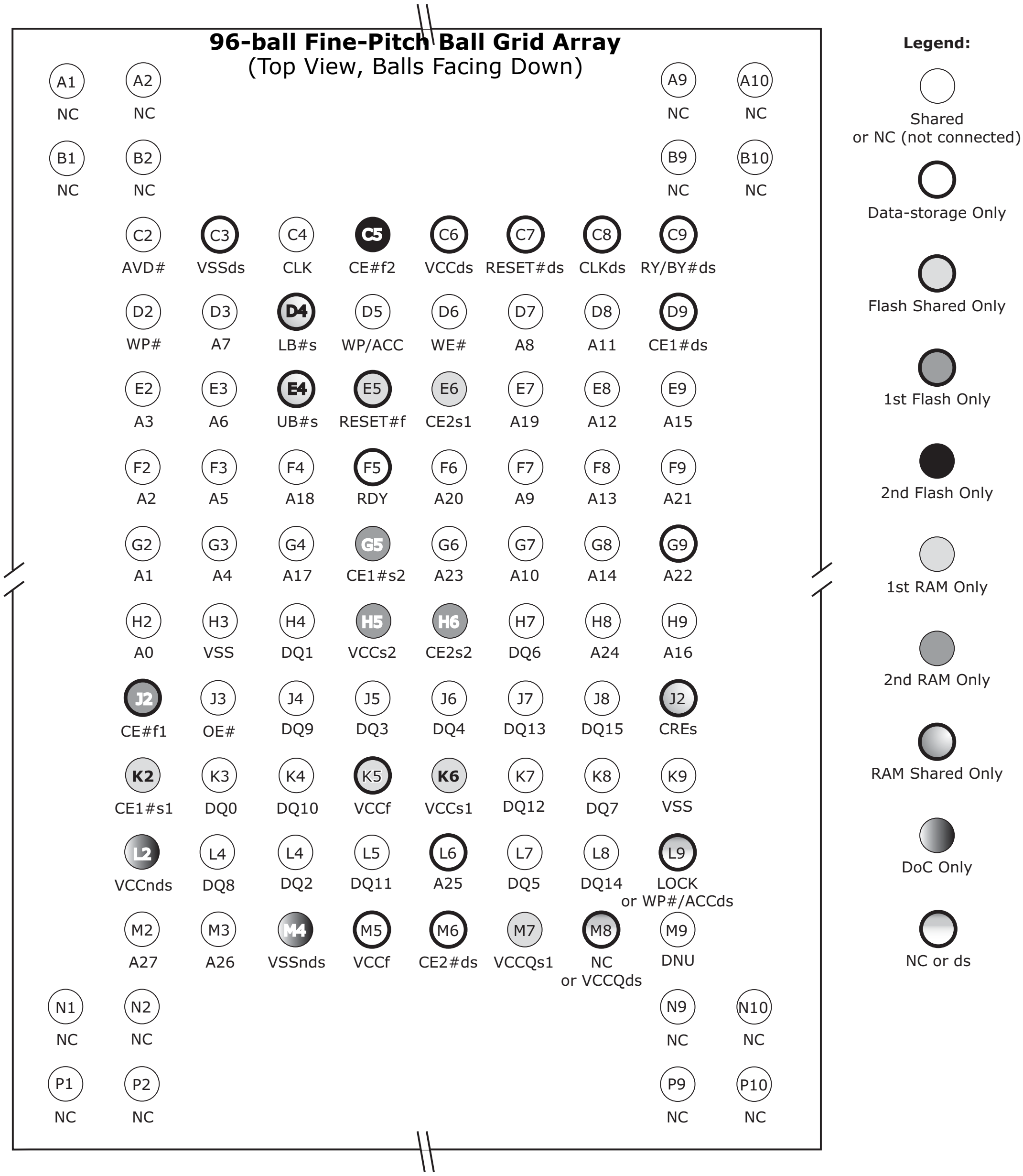
S29WS128N–MCP Compatible
84-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



S29WS064N–MCP Compatible
80-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



MCP Look-ahead Connection Diagram



Note: *To provide customers with a migration path to higher densities and an option to stack more die in a package, Spansion has prepared a standard pinout that supports*

- *NOR Flash and SRAM densities up to 4 Gigabits*
- *NOR Flash and pSRAM densities up to 4 Gigabits*
- *NOR Flash and pSRAM and DATA STORAGE densities up to 4 Gigabits*
- *See MCP data sheet (publication number S71WS256_512NC0) for input/output descriptions.*

The signal locations of the resultant MCP device are shown above. Note that for different densities, the actual package outline may vary. Any pinout in any MCP, however, will be a subset of the pinout above.

In some cases, there may be outrigger balls in locations outside the grid shown above. In such cases, treat them as reserved and do not connect them to any other signal.

For any further inquiries about the above look-ahead pinout, please refer to the application note on this subject or contact your sales office.

Multi-Chip Compatible Packages

For this family of products, a single multi-chip compatible package is offered for each density to allow both standalone and multi-chip qualification using a single, adaptable package. This new methodology allows package standardization resulting in faster development. The multi-chip compatible package includes all the pins required for standalone device operation and verification. In addition, extra pins are included for insertion of common data storage or logic devices to be used for multi-chip products. If a standalone device is required, the extra multi-chip specific pins are not connected and the standalone device operates normally. The multi-chip compatible package sizes were chosen to serve the largest number of combinations possible. There are only a few cases where a larger package size would be required to accommodate the multi-chip combination. This multi-chip compatible package set does not allow for direct package migration from legacy products.

Special Handling Instructions for FBGA Package

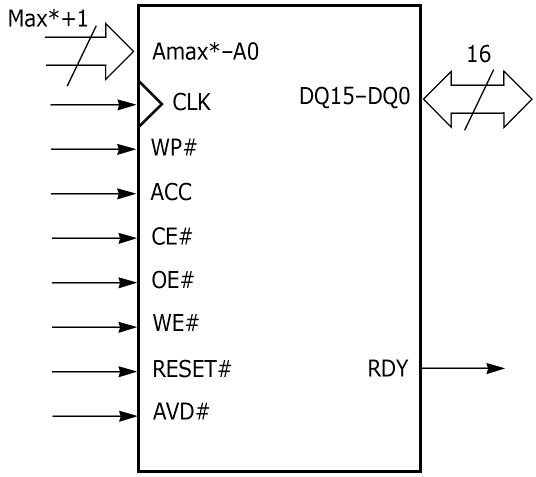
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Input/Output Descriptions

A23-A0	=	Address inputs for WS256N (A22-A0 for WS128 and A21-A0 for WS064N).
DQ15-DQ0	=	Data input/output.
CE#f1	=	Chip Enable input. Asynchronous relative to CLK for the Burst mode.
OE#	=	Output Enable input. Asynchronous relative to CLK for the Burst mode.
WE#	=	Write Enable input.
V_{CC}	=	Device Power Supply.
V_{SS}	=	Ground.
NC	=	No Connect; not connected internally.
RDY	=	Ready output. Indicates the status of the Burst read.
CLK	=	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode.
AVD#	=	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs.
RESET#	=	Hardware reset input. Low = device resets and returns to reading array data.
WP#	=	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.
ACC	=	Accelerated input. At V_{HH}, accelerates. programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.
RFU	=	Reserved for future use (see MCP look-ahead pinout for use with MCP).

Logic Symbol



* max = 23 for the WS256N, 22 for the WS128N, and 21 for the WS064N.

Ordering Information (256 Mb)

The ordering part number is formed by a valid combination of the following:

S29WS 256 N 0S BA W 01 0

PACKING TYPE
0 = Tray (standard; see Note 1)
2 = 7-inch Tape and Reel
3 = 13-inch Tape and Reel

MODEL NUMBER (Note 3)
(V_{IO} Range, Ball Count, Package Dimensions, DYB Protect/Unprotect After Power-up)
01 = 1.8 V V_{IO}, 84-ball, 8 mm x 11.6 mm, DYB Unprotect
11 = 1.8 V V_{IO}, 84-ball, 8 mm x 11.6 mm, DYB Protect

TEMPERATURE RANGE (Note 3)
W = Wireless (-25°C to +85°C)
I = Industrial (–40°C to +85°C)

PACKAGE TYPE AND MATERIAL
BA = Very Thin Fine-Pitch BGA, Lead (Pb)-free Compliant Package
BF = Very Thin Fine-Pitch BGA, Lead (Pb)-free Package

SPEED OPTION (BURST FREQUENCY)
0S = 80 MHz
0P = 66 MHz
0L = 54 MHz

PROCESS TECHNOLOGY
N = 110 nm MirrorBit™ Technology

FLASH DENSITY
256 = 256 Mb

DEVICE FAMILY
S29WS = 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memory

S29WS256N Valid Combinations					V_{IO} Range	DYB Power Up State	Package Type (Note 2)
Base Ordering Part Number	**Speed Option**	**Package Type, Material, & Temperature Range**	**Model Number**	**Packing Type**			
S29WS256N	0S, 0P, 0L	BAW (Lead (Pb)-free Compliant), BFW (Lead (Pb)-free)	01	0, 2, 3 (Note 1)	1.70–1.95 V	Unprotect	8 mm x 11.6 mm 84-ball MCP-Compatible
			11			Protect	

Notes:

1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S29" and packing type designator from ordering part number.*
3. *For 1.5 V_{IO} option, other boot options, or industrial temperature range, contact your local sales office.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Ordering Information (128 Mb)

The ordering part number is formed by a valid combination of the following:

S29WS 128 N 0S BA W 01 0

PACKING TYPE
0 = Tray (standard; see note 1)
2 = 7-inch Tape and Reel
3 = 13-inch Tape and Reel

MODEL NUMBER (Note 3)
(V_{IO} Range, Ball Count, Package Dimensions, DYB Protect/Unprotect After Power-up)
01 = 1.8 V V_{IO}, 84-ball, 8 mm x 11.6 mm, DYB Unprotect
11 = 1.8 V V_{IO}, 84-ball, 8 mm x 11.6 mm, DYB Protect

TEMPERATURE RANGE (Note 3)
W = Wireless (-25°C to +85°C)
I = Industrial (–40°C to +85°C)

PACKAGE TYPE AND MATERIAL
BA = Very Thin Fine-Pitch BGA, Lead (Pb)-free Compliant Package
BF = Very Thin Fine-Pitch BGA, Lead (Pb)-free Package

SPEED OPTION (BURST FREQUENCY)
0S = 80 MHz
0P = 66 MHz
0L = 54 MHz

PROCESS TECHNOLOGY
N = 110 nm MirrorBit™ Technology

FLASH DENSITY
128 = 128 Mb

DEVICE FAMILY
S29WS = 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memory

S29WS128N Valid Combinations					V_{IO} Range	DYB Power Up State	Package Type (Note 2)
Base Ordering Part Number	**Speed Option**	**Package Type, Material, & Temperature Range**	**Model Number**	**Packing Type**			
S29WS128N	0S, 0P, 0L	BAW (Lead (Pb)-free Compliant), BFW (Lead (Pb)-free)	01	0, 2, 3 (Note 1)	1.70–1.95 V	Unprotect	8 mm x 11.6 mm 84-ball MCP Compatible
			11			Protect	

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S29" and packing type designator from ordering part number.*
3. *For 1.5 V_{IO} option, other boot options, or industrial temperature range, contact your local sales office.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Ordering Information (64 Mb)

The ordering part number is formed by a valid combination of the following:

S29WS 064 N 0S BA W 05 0

PACKING TYPE
0 = Tray (standard; see note 1)
2 = 2-inch Tape and Reel
3 = 3-inch Tape and Reel

MODEL NUMBER (Note 3)
(V_{IO} Range, Ball Count, Package Dimensions, DYB Protect/Unprotect After Power-up)
01 = 1.8 V V_{IO}, 80-ball, 7 mm x 9 mm, DYB Unprotect
11 = 1.8 V V_{IO}, 80-ball, 7 mm x 9 mm, DYB Protect

TEMPERATURE RANGE (Note 3)
W = Wireless (-25°C to +85°C)
I = Industrial (–40°C to +85°C)

PACKAGE TYPE AND MATERIAL
BA = Very Thin Fine-Pitch BGA, Lead (Pb)-free Compliant Package
BF = Very Thin Fine-Pitch BGA, Lead (Pb)-free Package

SPEED OPTION (BURST FREQUENCY)
0S = 80 MHz
0P = 66 MHz
0L = 54 MHz

PROCESS TECHNOLOGY
N = 110 nm MirrorBit™ Technology

FLASH DENSITY
064 = 64 Mb

DEVICE FAMILY
S29WS = 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memory

S29WS064N Valid Combinations					V_{IO} Range	DYB Power Up State	Package Type (Note 2)
Base Ordering Part Number	**Speed Option**	**Package Type, Material, & Temperature Range**	**Model Number**	**Packing Type**			
S29WS064N	0S, 0P, 0L	BAW (Lead (Pb)-free Compliant), BFW (Lead (Pb)-free)	01	0, 2, 3 (Note 1)	1.70–1.95 V	Unprotect	7 mm x 9 mm 80-ball MCP-Compatible
			11			Protect	

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S29" and packing type designator from ordering part number.*
3. *For 1.5 V_{IO} option, other boot options, or industrial temperature range, contact your local sales office.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#	OE#	WE#	Addresses	DQ15–0	RESET#	CLK	AVD#
Asynchronous Read - Addresses Latched	L	L	H	Addr In	I/O	H	X	↑
Asynchronous Read - Addresses Steady State	L	L	H	Addr In	I/O	H	X	L
Asynchronous Write	L	H	L	Addr In	I/O	H	X	L
Synchronous Write	L	H	L	Addr In	I/O	H	↑	↑
Standby (CE#)	H	X	X	X	HIGH Z	H	X	X
Hardware Reset	X	X	X	X	HIGH Z	L	X	X
Burst Read Operations (Synchronous)								
Load Starting Burst Address	L	X	H	Addr In	X	H	↑	↑
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	X	Burst Data Out	H	↑	H
Terminate current Burst read cycle	H	X	H	X	HIGH Z	H	↑	X
Terminate current Burst read cycle via RESET#	X	X	H	X	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	X	H	Addr In	I/O	H	↑	↑

Legend: *L = Logic 0, H = Logic 1, X = Don't Care.*

VersatileIO™ (V_{IO}) Control

The VersatileIO (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin.

Requirements for Asynchronous (Non-Burst) Read Operation

To read data from the memory array, the system must first assert a valid address on A23–A0 for WS256N (A22–A0 for the WS128N, A21–A0 for WS064N), while driving AVD# and CE# to V_{IL}. WE# should remain at V_{IH}. The rising edge of AVD# latches the address. The data will appear on DQ15–DQ0.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data in asynchronous mode upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

Requirements for Synchronous (Burst) Read Operation

The device is capable of continuous sequential burst read and linear burst read of a preset length. When the device first powers up, it is enabled for asynchronous read operation.

Prior to entering burst mode, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst access, what mode of burst operation is desired, and how the RDY signal will transition with valid data. The system would then write the configuration register command sequence. See Set Configuration Register Command Sequence for further details.

The initial word is output t_{IACC} after the active edge of the first CLK cycle. Subsequent words are output t_{BACC} after the active edge of each successive clock cycle at which point the internal address counter is automatically incremented. Note that the device has a fixed internal address boundary that occurs every 128 words, starting at address 00007Fh. No boundary crossing latency is required when the device operates at or below 66 MHz to reach address 000080h. When the device operates above 66 MHz, a boundary crossing of one additional wait state is required. The timing diagram can be found in Figure 28.

When the starting burst address is not divisible by four, additional waits are required. For example, if the starting burst address is divisible by four A1:0 = 00, no additional wait state is required, but if the starting burst address is at address A1:0 = 01, 10, or 11, one, two or three wait states are required, respectively, until data D4 is read. The RDY output indicates this condition to the system by deasserting (see Table 2).

Table 2. Address Dependent Additional Latency

Initial Address A[10]	Cycle						
	X	X+1	X+2	X+3	X+4	X+5	X+6
00	D0	D1	D2	D3	D4	D5	D6
01	D1	D2	D3	—	D4	D5	D6
10	D2	D3	—	—	D4	D5	D6
11	D3	—	—	—	D4	D5	D6

Table 3 shows the address latency for variable wait state scheme, as implemented in WS256N.

Table 3. Address Latency for x Wait States (≤ 80 MHz)

Word	Wait States	Cycle								
0	x ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	x ws	D1	D2	D3	1 ws	D4	D5	D6	D7	D8
2	x ws	D2	D3	1 ws	1 ws	D4	D5	D6	D7	D8
3	x ws	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7	D8

Tables 4–7 show the address latency for variable wait state scheme, as implemented in WS128N and WS064N.

Table 4. Address Latency for 6 Wait States (≤ 80 MHz)

Word	Wait States	Cycle								
0	6 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	6 ws	D1	D2	D3	1 ws	D4	D5	D6	D7	D8
2	6 ws	D2	D3	1 ws	1 ws	D4	D5	D6	D7	D8
3	6 ws	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7	D8

Table 5. Address Latency for 5 Wait States (≤ 68 MHz)

Word	Wait States	Cycle								
0	5 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	5 ws	D1	D2	D3	D4	D5	D6	D7	D8	D9
2	5 ws	D2	D3	1 ws	D4	D5	D6	D7	D8	D9
3	5 ws	D3	1 ws	1 ws	D4	D5	D6	D7	D8	D9

Table 6. Address Latency for 4 Wait States (≤ 54 MHz)

Word	Wait States	Cycle								
0	4 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	4 ws	D1	D2	D3	D4	D5	D6	D7	D8	D9
2	4 ws	D2	D3	D4	D5	D6	D7	D8	D9	D10
3	4 ws	D3	1 ws	D4	D5	D6	D7	D8	D9	D10

Table 7. Address Latency for 3 Wait States (≤ 40 MHz)

Word	Wait States	Cycle								
0	3 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	3 ws	D1	D2	D3	D4	D5	D6	D7	D8	D9
2	3 ws	D2	D3	D4	D5	D6	D7	D8	D9	D10
3	3 ws	D3	D4	D5	D6	D7	D8	D9	D10	D11

Tables 8-11 show the address/boundary crossing latency for variable wait state if a boundary crossing occurs during initial access as implemented in WS128N and WS064N.

Table 8. Address/Boundary Crossing Latency for 6 Wait States (≤ 80 MHz)

Word	Wait States	Cycle								
0	6 ws	D0	D1	D2	D3	1 ws	D4	D5	D6	D7
1	6 ws	D1	D2	D3	1 ws	1 ws	D4	D5	D6	D7
2	6 ws	D2	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7
3	6 ws	D3	1 ws	1 ws	1 ws	1 ws	D4	D5	D6	D7

Table 9. Address/Boundary Crossing Latency for 5 Wait States (< 66 MHz)

Word	Wait States	Cycle								
0	5 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	5 ws	D1	D2	D3	1 ws	D4	D5	D6	D7	D8
2	5 ws	D2	D3	1 ws	1 ws	D4	D5	D6	D7	D8
3	5 ws	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7	D8

Table 10. Address/Boundary Crossing Latency for 4 Wait States (< 54 MHz)

Word	Wait States	Cycle								
0	4 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	4 ws	D1	D2	D3	D4	D5	D6	D7	D8	D9
2	4 ws	D2	D3	1 ws	D4	D5	D6	D7	D8	D9
3	4 ws	D3	1 ws	1 ws	D4	D5	D6	D7	D8	D9

Table 11. Address/Boundary Crossing Latency for 3 Wait States (< 40 MHz)

Word	Wait States	Cycle								
0	3 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	3 ws	D1	D2	D3	D4	D5	D6	D7	D8	D9
2	3 ws	D2	D3	D4	D5	D6	D7	D8	D9	D10
3	3 ws	D3	1 ws	D4	D5	D6	D7	D8	D9	D10

Continuous Burst

The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system drives CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 1.

If the host system crosses a 128-word line boundary while reading in burst mode, and the subsequent word line is not programming or erasing, a one-cycle latency is required as described above if the device is operating above 66 MHz. If the device is operating at or below 66 MHz, no boundary crossing latency is required. If the host system crosses the bank boundary while the subsequent bank is programming or erasing, the device will provide read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

8-, 16-, and 32-Word Linear Burst with Wrap Around

The next three burst read modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 12.)

Table 12. Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h,...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh,...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh,...

For example, if the starting address in the 8-word mode is 3Ch, the address range to be read would be 38-3Fh, and the burst sequence would be 3C-3D-3E-3F-38-39-3A-3Bh if wrap around is enabled. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group and stops at the group size, terminating the burst read. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 128 words; thus, no wait states are inserted (except during the initial access).** (See Figure 15.)

8-, 16-, and 32-Word Linear Burst without Wrap Around

If wrap around is not enabled, 8-word, 16-word, or 32-word burst will execute linearly up to the maximum memory address of the selected number of words. The burst will stop after 8, 16, or 32 addresses and will not wrap around to the first address of the selected group. For example: if the starting address in the 8-word mode is 3Ch, the address range to be read would be 39-40h, and the burst sequence would be 3C-3D-3E-3F-40-41-42-43h if wrap around is not enabled. The next address to be read will require a new address and AVD# pulse. Note that in this burst read mode, the address pointer may cross the boundary that occurs every 128 words.

Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, RDY configuration, and synchronous mode active. For more information, see Table 26.

RDY: Ready

The RDY is a dedicated output, controlled by CE#. When the device is configured in the Synchronous mode and RDY is at logic low, the system should wait 1 clock cycle before expecting the next word of data.

Handshaking

The device is equipped with a handshaking feature that allows the host system to simply monitor the RDY signal from the device to determine when the burst data is ready to be read. The host system should use the programmable wait state configuration to set the number of wait states for optimal burst mode operation. The initial word of burst data is indicated by the rising edge of RDY after OE# goes low.

For optimal burst mode performance, the host system must set the appropriate number of wait states in the flash device depending on clock frequency. See Set Configuration Register Command Sequence and Requirements for Synchronous (Burst) Read Operation for more information.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in another bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 31 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-program and read-while-erase current specifications.

Writing Commands/Command Sequences

The device has the capability of performing an asynchronous or synchronous write operation. While the device is configured in Asynchronous read it is able to perform Asynchronous write operations only. CLK is ignored when the device is configured in the Asynchronous mode. When in the Synchronous read mode configuration, the device is able to perform both Asynchronous and Synchronous write operations. CLK- and AVD#-induced address latches are supported in the Synchronous programming mode. During a synchronous write operation, to write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH} when writing commands or data. During an asynchronous write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing an address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE# (see Table 26).

An erase operation can erase one sector, multiple sectors, or the entire device. Table 21 indicates the address space that each sector occupies. The device address space is divided into sixteen banks: Banks 1 through 14 contain only 64 Kword sectors, while Banks 0 and 15 contain both 16 Kword boot sectors in addition to 64 Kword sectors. A “bank address” is the set of address bits required to uniquely select a bank. Similarly, a “sector address” is the address bits required to uniquely select a sector.

I_{CC2} in “DC Characteristics” represents the active current specification for the write mode. “AC Characteristics—Synchronous” and “AC Characteristics—Asynchronous” contain timing specification tables and timing diagrams for write operations.

Unlock Bypass Mode

The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a set of words, instead of four. See Unlock Bypass Command Sequence for more details.

Accelerated Program/Chip Erase Operations

The device offers accelerated program and accelerated chip/erase operations through the ACC function. ACC is intended to allow faster manufacturing throughput at the factory and not to be used in system operations.

If the system asserts V_{HH} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program and erase operations. The system can then use the Write Buffer Load command sequence provided by the Unlock Bypass mode. Note that if a “Write-to-Buffer-Abort Reset” is required while in Unlock Bypass mode, the **full 3-cycle RESET command sequence must be used to**

reset the device. Removing V_{HH} from the ACC input, upon completion of the embedded program or erase operation, returns the device to normal operation. Note that sectors must be unlocked prior to raising ACC to V_{HH}. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming and accelerated chip erase, or device damage may result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result*.

When at V_{IL}, ACC locks all sectors. ACC should be at V_{IH} for all other conditions.

Write Buffer Programming Operation

Write Buffer Programming allows the system to write a maximum of **32** words in one programming operation. This results in a faster effective word programming time than the standard "word" programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the starting address in which programming will occur. At this point, the system writes the number of "**word locations minus 1**" that will be loaded into the page buffer at the starting address in which programming will occur. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the "Program Buffer to Flash" confirm command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort. (NOTE: the number loaded = the number of locations to program minus 1. For example, if the system will program 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the "write-buffer-page" address. All subsequent address/data pairs **must** fall within the "selected-write-buffer-page".

The "write-buffer-page" is selected by using the addresses A_{MAX} - A5 where A_{MAX} is A23 for WS256N, A22 for WS128N, and A21 for WS064N.

The "write-buffer-page" addresses **must be the same for all address/data pairs loaded into the write buffer**. (This means Write Buffer Programming **cannot** be performed across multiple "write-buffer-pages". This also means that Write Buffer Programming **cannot** be performed across multiple sectors. If the system attempts to load programming data outside of the selected "write-buffer-page", the operation will ABORT.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

Note that if a Write Buffer address location is loaded multiple times, the "address/data pair" counter **will be decremented for every data load operation**. Also, the **last data loaded** at a location before the "Program Buffer to Flash" confirm command will be programmed into the device. It is the software's responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements **for each data load operation**, **NOT for each unique write-buffer-address location**.

Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" command at the Sector Address. Any other address/data write combinations will abort the Write Buffer Programming operation. The device will then "go busy." The Data Bar polling techniques should be used while monitoring the **last address location loaded into the write buffer**. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then data bar poll at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer "embedded" programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device will return to READ mode.

The Write Buffer Programming Sequence is ABORTED under any of the following conditions:

- Load a value that is greater than the page buffer size during the "Number of Locations to Program" step.
- Write to an address in a sector different than the one specified during the "Write-Buffer-Load" command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the "Starting Address" during the "write buffer data loading" stage of the operation.
- Write data other than the "Confirm Command" after the specified number of "data load" cycles.

The ABORT condition is indicated by DQ1 = 1, DQ7 = DATA# (for the "last address location loaded"), DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A "Write-to-Buffer-Abort reset" command sequence is required when using the Write-Buffer-Programming features in Unlock Bypass mode. Note that the SecSi™ sector, autoselect, and CFI functions are unavailable when a program operation is in progress.

Use of the write buffer is strongly recommended for programming when multiple words are to be programmed. Write buffer programming is allowed in any sequence of memory (or address) locations. These flash devices are capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. However, programming the same word address multiple times without intervening erases requires a modified programming method. Please contact your local Spansion™ representative for details.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output from the internal register (separate from the memory array) on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. The autoselect codes can also be accessed in-system.

When verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 21). The remaining address bits are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0. The autoselect codes can also be accessed in-system through the command register. See Command Definition Summary for command sequence requirements. *Note that if a Bank Address (BA) on the four uppermost address bits is asserted during the third write cycle of the autoselect command, the host system can read au-*

toselect data from that bank and then immediately read array data from the other bank, without exiting the autoselect mode.

To access the autoselect codes, the host system must issue the autoselect command via the command register, as shown in the Command Definition Summary section. See Autoselect Command Sequence for more information.

Advanced Sector Protection and Unprotection

This advanced security feature provides an additional level of protection to all sectors against inadvertant program or erase operations.

The advanced sector protection feature disables both programming and erase operations in a sector while the advanced sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented using either or both of the two methods

- Hardware method
- Software method

Persistent/Password Sector Protection is achieved by using the software method while the sector protection with WP# pin is achieved by using the hardware method.

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used.

- Persistent Mode Lock Bit
- Password Mode Lock Bit

If the customer decides to continue using the Persistent Sector Protection method, they must set the **Persistent Mode Lock Bit**. This will permanently set the part to operate using only Persistent Sector Protection. However, if the customer decides to use the Password Sector Protection method, they must set the **Password Mode Lock Bit**. This will permanently set the part to operate using only Password Sector Protection.

It is important to remember that setting either the **Persistent Mode Lock Bit** or the **Password Mode Lock Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone. If both are selected to be set at the same time, the operation will abort.** This is done so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Sector Protection Mode.

The device is shipped with all sectors unprotected. Optional Spansion™ programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for more details.

Persistent Mode Lock Bit

A Persistent Mode Lock Bit exists to guarantee that the device remain in software sector protection. Once programmed (set to "0"), the Persistent Mode Lock Bit prevents programming of the Password Mode Lock Bit. This allows protection from potential hackers locking the device by placing the device in password sector protection mode and then changing the password accordingly.

Password Mode Lock Bit

In order to select the Password Sector Protection scheme, the customer must first program the password. It is recommended that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

1.It permanently sets the device to operate using the Password Sector Protection Mode. It is not possible to reverse this function.

2.It also disables *all further commands* to the password region. All program and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Sector Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is after it is set. If the password is lost after setting the Password Mode Lock Bit, there will be no way to clear the PPB Lock Bit.

The Password Mode Lock Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. **The Password Mode Lock Bit is not erasable.** Once the Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors.

- Persistent Sector Protection

A software enabled command sector protection method that replaces the old 12 V controlled protection method.

- Password Sector Protection

A highly sophisticated software enabled protection method that requires a password before changes to certain sectors or sector groups are permitted

- WP# Hardware Protection

A write protect pin (WP#) can prevent program or erase operations in the outermost sectors.The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- Persistently Locked—A sector is protected and cannot be changed.
- Dynamically Locked—The sector is protected and can be changed by a simple command

- Unlocked—The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of "bits" namely Persistent Protection Bit (PPB), Dynamic Protection Bit (DYB), and Persistent Protection Bit Lock (PPB Lock) are used to achieve the desired sector protection scheme

Persistent Protection Bit (PPB)

PPB is used to as an advanced security feature to protect individual sectors from being programmed or erased thereby providing additional level of protection. Every sector is assigned a Persistent Protection Bit.

Each PPB is individually programmed through the **PPB Program Command**. However all PPBs are erased in parallel through the **All PPB Erase Command**. Prior to erasing, these bits don't have to be preprogrammed. The Embedded Erase algorithm automatically preprograms and verifies prior to an electrical erase. The system is not required to provide any controls or timings during these operations.

The PPBs retain their state across power cycles because they are Non-Volatile. The PPBs have the same endurance as the flash memory.

Persistent Protection Bit Lock (PPB Lock Bit) in Persistent Sector Protection Mode

PPB Lock Bit is a global volatile bit and provides an additional level of protection to the sectors. When **programmed (set to "0")**, all the PPBs are locked and hence none of them can be changed. When **erased (cleared to "1")**, the PPBs are changeable. There is only one PPB Lock Bit in every device. Only a hardware reset or a power-up clears the PPB Lock Bit. Note that there is no software solution; that is, there is no command sequence that would unlock the PPB Lock Bit.

Once all PPBs are configured to the desired settings, the PPB Lock Bit may be set (programmed to "0"). The PPB Lock Bit is set by issuing the PPB Lock Bit Set Command. Programming or setting the PPB Lock Bit disables program and erase commands to all the PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock Bit is to go through a hardware or power-up reset. System boot code can determine if any changes to the PPB are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can disable the PPB Lock Bit to prevent any further changes to the PPBs during system operation.

Dynamic Protection Bit (DYB)

DYB is another security feature used to protect individual sectors from being programmed or erased inadvertently. It is a volatile protection bit and is assigned to each sector. Each DYB can be individually modified through the DYB Set Command or the DYB Clear Command.

The Protection Status for a particular sector is determined by the status of the PPB and the DYB relative to that sector. For the sectors that have the PPBs cleared (erased to "1"), the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Set or Clear command sequences, the DYBs will be set (programmed to "0") or cleared (erased to "1"), thus placing each sector in the protected or unprotected state respectively. These states are the so-called **Dynamic Locked or Unlocked** states due to the fact that they can switch back and forth between the protected and unprotected states. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set (programmed to “0”) or cleared (erased to “1”) as often as needed.

When the parts are first shipped, the PPBs are cleared (erased to “1”) and upon power up or reset, the DYBs are set or cleared depending upon the ordering option chosen. If the option to clear the DYBs after power up is chosen, (erased to “1”), then the sectors may be modified depending upon the PPB state of that sector. (See Table 13) If the option to set the DYBs after power up is chosen (programmed to “0”), then the sectors would be in the protected state. The PPB Lock Bit defaults to the cleared state (erased to “1”) after power up and the PPBs retain their previous state as they are non-volatile.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Set command sequence is all that is necessary. The DYB Set or Clear command for the dynamic sectors signify protected or unprotected state of the sectors respectively. However, if there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again will lock the PPBs, and the device operates normally again.

To achieve the best protection, execute the PPB Lock Bit Set command early in the boot code and protect the boot code by holding WP# = V_{IL}. Note that the PPB and DYB bits have the same function when ACC = V_{HH} as they do when ACC = V_{IH}.

Table 13. Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
1	1	1	Sector Unprotected
0	1	1	Sector Protected through DYB
1	0	1	Sector Protected through PPB
0	0	1	Sector Protected through PPB and DYB
1	1	0	Sector Unprotected
0	1	0	Sector Protected through DYB
1	0	0	Sector Protected through PPB
0	0	0	Sector Protected through PPB and DYB

Table 13 contains all possible combinations of the DYB, PPB, and PPB Lock relating to the status of the sector.

In summary, if the PPB is set (programmed to “0”), and the PPB Lock is set (programmed to “0”), the sector is protected and the protection can not be removed until the next power cycle clears (erase to “1”) the PPB Lock Bit. Once the PPB Lock Bit is cleared (erased to “1”), the sector can be persistently locked or unlocked. Likewise, if both PPB Lock Bit or PPB is cleared (erased to “1”) the sector can then be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program or erase command to a protected sector enables status polling and returns to read mode without having modified the contents of the protected sector.

The programming of the DYB, PPB, and PPB Lock for a given sector can be verified by writing individual status read commands DYB Status, PPB Status, and PPB Lock Status to the device.

Password Sector Protection

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection Mode and the Password Sector Protection Mode:

- When the device is first powered up, or comes out of a reset cycle, the **PPB Lock Bit is set to the locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock Bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a **non-erasable** region of the flash memory. Once the Password Mode Lock Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock Bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock Bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 1 µs delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands. The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Persistent Protection Bit Lock (PPB Lock Bit) in Password Sector Protection Mode

The Persistent Protection Bit Lock (PPB Lock Bit) is a volatile bit that reflects the state of the Password Mode Lock Bit after power-up reset. If the Password Mode Lock Bit is also set, after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command to enter the entire password clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET# or taking the device through a power-on reset, resets the PPB Lock Bit to a "1".

If the Password Mode Lock Bit is not set (device is operating in the default Persistent Protection Mode). The Password Unlock command is ignored in Persistent Sector Protection Mode.

Lock Register

The Lock Register consists of 3 bits. The Customer SecSi Sector Protection Bit is DQ0, Persistent Protection Mode Lock Bit is DQ1, and the Password Protection Mode Lock Bit is DQ2. Each of these bits are non-volatile. DQ15-DQ3 are reserved and will be 1's.

Table 14. Lock Register

DQ15-3	DQ2	DQ1	DQ0
1's	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Customer SecSi Sector Protection Bit

Hardware Data Protection Mode

The device offers two types of data protection at the sector level:

- When WP# is at V_{IL}, the four outermost sectors are locked (device specific).
- When ACC is at V_{IL}, all sectors are locked.

The write protect pin (WP#) adds a final level of hardware program and erase protection to the outermost boot sectors. The outermost boot sectors are the sectors containing both the lower and upper set of outermost sectors in a dual-boot-configured device. **When this pin is low it is not possible to change the contents of these outermost sectors.** These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the four outermost sectors. This function is provided by the WP# pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP# pin during the command sequence, the device disables program and erase functions in the "outermost" boot sectors. The outermost boot sectors are the sectors containing both the lower and upper set of sectors in a dual-boot-configured device.

If the system asserts V_{IH} on the WP# pin, the device reverts to whether the boot sectors were last set to be protected or unprotected after the embedded operation. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

Note that the WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result. The WP# pin must be held stable during a command sequence.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than t_{WEP} on WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the standby mode when the CE# and RESET# inputs are both held at V_{CC}. The device requires standard access time (t_{CE}) for read access, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in "DC Characteristics" represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. While in asynchronous mode, the device automatically enables this mode when addresses remain stable for t_{ACC} + 20 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. While in synchronous mode, the automatic sleep mode is disabled. Note that a new burst operation is required to provide new data.

I_{CC6} in "DC Characteristics" represents the automatic sleep mode current specification.

RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not at V_{SS}, the standby current will be greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

See Hardware Reset (RESET#) for RESET# parameters and to Figure 20 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

SecSi™ (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides an extra Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 256 words in length. All reads outside of the 256 word address range will return non-valid data. The Factory Indicator Bit (DQ7) is used to indicate whether or not the Factory SecSi Sector is locked when shipped from the factory. The Customer Indicator Bit (DQ6) is used to indicate whether or not the Customer SecSi Sector is locked when shipped from the factory. The Factory SecSi bits are permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN and customer code once the product is shipped to the field.

The Factory portion of the SecSi Sector is locked when shipped and the Customer SecSi Sector that is either locked or is lockable. The Factory SecSi Sector is always protected when shipped from the factory, and has the Factory Indicator Bit (DQ7) permanently set to a "1". The Customer SecSi Sector is typically shipped unprotected (set to "0"), allowing customers to utilize that sector in any manner they choose. Once the Customer SecSi Sector area is protected, the Customer Indicator Bit will be permanently set to "1."

The system accesses the SecSi Sector through a command sequence (see Enter SecSi™ Sector/Exit SecSi Sector Command Sequence). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by sector SA0 within the memory array. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. While SecSi Sector access is enabled, Memory Array read access, program operations, and erase operations to all sectors other than SA0 are also available. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.

Factory Locked: Factor SecSi Sector Programmed and Protected At the Factory

In a factory sector locked device, the Factory SecSi Sector is protected when the device is shipped from the factory. The Factory SecSi Sector cannot be modified in any way. The device is pre programmed with both a random number and a secure ESN. The Factory SecSi Sector is located at addresses 000000h–00007Fh.

The device is available pre programmed with one of the following:

- A random, secure ESN only within the Factor SecSi Sector
- Customer code within the Customer SecSi Sector through the Spansion™ programming service
- Both a random, secure ESN and customer code through the Spansion™ programming service.

Table 15. SecSi™ Sector Addresses

Sector	Sector Size	Address Range
Customer	128 words	000080h-0000FFh
Factory	128 words	000000h-00007Fh

Customers may opt to have their code programmed through the Spansion™ programming services. Spansion programs the customer's code, with or without the random ESN. The devices are then shipped from the Spansion factory with the Factory SecSi Sector and Customer SecSi Sector permanently locked. Contact your local representative for details on using Spansion™ programming services.

Customer SecSi Sector

If the security feature is not required, the Customer SecSi Sector can be treated as an additional Flash memory space. The Customer SecSi Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Customer SecSi Sector, but reading in Banks 1 through 15 is available. The Customer SecSi Sector is located at addresses 000080h–0000FFh.

The Customer SecSi Sector area can be protected by writing the SecSi Sector Protection Bit Lock command sequence.

Once the Customer SecSi Sector is locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing the memory array. The device returns to the memory array at bank 0.

The Customer SecSi Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the Customer SecSi Sector area and none of the bits in the Customer SecSi Sector memory space can be modified in any way.

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address (BA)555h any time the device is ready to read array data. The system can read CFI information at valid addresses within that bank (see Tables 16– 19). All reads outside of the CFI address range, within the bank, will return non-valid data. Reads from other banks are allowed, writes are not. To terminate reading CFI data, the system must write the reset command.

For further information, please refer to the CFI Specification and CFI Publication 100. Please contact your sales office for copies of these documents.

Table 16. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 17. System Interface String

Addresses	Data	Description
1Bh	0017h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0006h	Typical timeout per single byte/word write 2^N µs
20h	0009h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0003h	Max. timeout for byte/word write 2^N times typical
24h	0001h	Max. timeout for buffer write 2^N times typical
25h	0002h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 18. Device Geometry Definition

Addresses	Data	Description
27h	0019h (WS256N) 0018h (WS128N) 0017h (WS064N)	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0006h 0000h	Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0003h 0000h 0080h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)

Table 18. Device Geometry Definition (Continued)

Addresses	Data	Description
31h	00FDh (WS256N) 007Dh (WS128N) 003Dh (WS064N)	Erase Block Region 2 Information
32h 33h 34h	0000h 0000h 0002h	
35h 36h 37h 38h	0003h 0000h 0080h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 19. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string "PRI"
43h	0031h	Major version number, ASCII
44h	0034h	Minor version number, ASCII
45h	0100h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Technology (Bits 5-2) 0100 = 0.11 µm
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0008h	Sector Protect/Unprotect scheme 08 = Advanced Sector Protection
4Ah	00DFh (WS256N) 006Fh (WS128N) 0037h (WS064N)	Simultaneous Operation Number of Sectors in all banks except boot bank
4Bh	0001h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page, 04 = 16 Word Page
4Dh	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 0001h = Dual Boot Device

Table 19. Primary Vendor-Specific Extended Query (Continued)

Addresses	Data	Description
50h	0001h	Program Suspend. 00h = not supported
51h	0001h	Unlock Bypass 00 = Not Supported, 01=Supported
52h	0007h	SecSi Sector (Customer OTP Area) Size 2^N bytes
53h	0014h	Hardware Reset Low Time-out during an embedded algorithm to read mode Maximum 2^N ns
54h	0014h	Hardware Reset Low Time-out not during an embedded algorithm to read mode Maximum 2^N ns
55h	0005h	Erase Suspend Time-out Maximum 2^N ns
56h	0005h	Program Suspend Time-out Maximum 2^N ns
57h	0010h	Bank Organization: X = Number of banks
58h	0013h (WS256N) 000Bh (WS128N) 0007h (WS064N)	Bank 0 Region Information. X = Number of sectors in bank
59h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 1 Region Information. X = Number of sectors in bank
5Ah	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 2 Region Information. X = Number of sectors in bank
5Bh	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 3 Region Information. X = Number of sectors in bank
5Ch	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 4 Region Information. X = Number of sectors in bank
5Dh	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 5 Region Information. X = Number of sectors in bank
5Eh	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 6 Region Information. X = Number of sectors in bank
5Fh	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 7 Region Information. X = Number of sectors in bank
60h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 8 Region Information. X = Number of sectors in bank
61h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 9 Region Information. X = Number of sectors in bank
62h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 10 Region Information. X = Number of sectors in bank
63h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 11 Region Information. X = Number of sectors in bank

Table 19. Primary Vendor-Specific Extended Query (Continued)

Addresses	Data	Description
64h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 12 Region Information. X = Number of sectors in bank
65h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 13 Region Information. X = Number of sectors in bank
66h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 14 Region Information. X = Number of sectors in bank
67h	0013h (WS256N) 000Bh (WS128N) 0007h (WS064N)	Bank 15 Region Information. X = Number of sectors in bank

Table 20. WS256N Sector & Memory Address Map

Bank	Sector	Sector Size	A23–A14	(x16) Address Range
Bank 0	SA0	16 Kwords	0000000000	000000h-003FFFh
	SA1	16 Kwords	0000000001	004000h-007FFFh
	SA2	16 Kwords	0000000010	008000h-00BFFFh
	SA3	16 Kwords	0000000011	00C000h-00FFFFh
	SA4	64 Kwords	00000001XX	010000h-01FFFFh
	SA5	64 Kwords	00000010XX	020000h-02FFFFh
	SA6	64 Kwords	00000011XX	030000h-03FFFFh
	SA7	64 Kwords	00000100XX	040000h-04FFFFh
	SA8	64 Kwords	00000101XX	050000h-05FFFFh
	SA9	64 Kwords	00000110XX	060000h-06FFFFh
	SA10	64 Kwords	00000111XX	070000h-07FFFFh
	SA11	64 Kwords	00001000XX	080000h-08FFFFh
	SA12	64 Kwords	00001001XX	090000h-09FFFFh
	SA13	64 Kwords	00001010XX	0A0000h-0AFFFFh
	SA14	64 Kwords	00001011XX	0B0000h-0BFFFFh
	SA15	64 Kwords	00001100XX	0C0000h-0CFFFFh
	SA16	64 Kwords	00001101XX	0D0000h-0DFFFFh
	SA17	64 Kwords	00001110XX	0E0000h-0EFFFFh
	SA18	64 Kwords	00001111XX	0F0000h-0FFFFFh

Table 20. WS256N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A23–A14	(x16) Address Range
Bank 1	SA19	64 Kwords	00010000XX	100000h-10FFFFh
	SA20	64 Kwords	00010001XX	110000h-11FFFFh
	SA21	64 Kwords	00010010XX	120000h-12FFFFh
	SA22	64 Kwords	00010011XX	130000h-13FFFFh
	SA23	64 Kwords	00010100XX	140000h-14FFFFh
	SA24	64 Kwords	00010101XX	150000h-15FFFFh
	SA25	64 Kwords	00010110XX	160000h-16FFFFh
	SA26	64 Kwords	00010111XX	170000h-17FFFFh
	SA27	64 Kwords	00011000XX	180000h-18FFFFh
	SA28	64 Kwords	00011001XX	190000h-19FFFFh
	SA29	64 Kwords	00011010XX	1A0000h-1AFFFFh
	SA30	64 Kwords	00011011XX	1B0000h-1BFFFFh
	SA31	64 Kwords	00011100XX	1C0000h-1CFFFFh
	SA32	64 Kwords	00011101XX	1D0000h-1DFFFFh
	SA33	64 Kwords	00011110XX	1E0000h-1EFFFFh
	SA34	64 Kwords	00011111XX	1F0000h-1FFFFFh
Bank 2	SA35	64 Kwords	00100000XX	200000h-20FFFFh
	SA36	64 Kwords	00100001XX	210000h-21FFFFh
	SA37	64 Kwords	00100010XX	220000h-22FFFFh
	SA38	64 Kwords	00100011XX	230000h-23FFFFh
	SA39	64 Kwords	00100100XX	240000h-24FFFFh
	SA40	64 Kwords	00100101XX	250000h-25FFFFh
	SA41	64 Kwords	00100110XX	260000h-26FFFFh
	SA42	64 Kwords	00100111XX	270000h-27FFFFh
	SA43	64 Kwords	00101000XX	280000h-28FFFFh
	SA44	64 Kwords	00101001XX	290000h-29FFFFh
	SA45	64 Kwords	00101010XX	2A0000h-2AFFFFh
	SA46	64 Kwords	00101011XX	2B0000h-2BFFFFh
	SA47	64 Kwords	00101100XX	2C0000h-2CFFFFh
	SA48	64 Kwords	00101101XX	2D0000h-2DFFFFh
	SA49	64 Kwords	00101110XX	2E0000h-2EFFFFh
	SA50	64 Kwords	00101111XX	2F0000h-2FFFFFh

Table 20. WS256N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A23–A14	(x16) Address Range
Bank 3	SA51	64 Kwords	00110000XX	300000h-30FFFFh
	SA52	64 Kwords	00110001XX	310000h-31FFFFh
	SA53	64 Kwords	00110010XX	320000h-32FFFFh
	SA54	64 Kwords	00110011XX	330000h-33FFFFh
	SA55	64 Kwords	00110100XX	340000h-34FFFFh
	SA56	64 Kwords	00110101XX	350000h-35FFFFh
	SA57	64 Kwords	00110110XX	360000h-36FFFFh
	SA58	64 Kwords	00110111XX	370000h-37FFFFh
	SA59	64 Kwords	00111000XX	380000h-38FFFFh
	SA60	64 Kwords	00111001XX	390000h-39FFFFh
	SA61	64 Kwords	00111010XX	3A0000h-3AFFFFh
	SA62	64 Kwords	00111011XX	3B0000h-3BFFFFh
	SA63	64 Kwords	00111100XX	3C0000h-3CFFFFh
	SA64	64 Kwords	00111101XX	3D0000h-3DFFFFh
	SA65	64 Kwords	00111110XX	3E0000h-3EFFFFh
	SA66	64 Kwords	00111111XX	3F0000h-3FFFFFh
Bank 4	SA67	64 Kwords	01000000XX	400000h-40FFFFh
	SA68	64 Kwords	01000001XX	410000h-41FFFFh
	SA69	64 Kwords	01000010XX	420000h-42FFFFh
	SA70	64 Kwords	01000011XX	430000h-43FFFFh
	SA71	64 Kwords	01000100XX	440000h-44FFFFh
	SA72	64 Kwords	01000101XX	450000h-45FFFFh
	SA73	64 Kwords	01000110XX	460000h-46FFFFh
	SA74	64 Kwords	01000111XX	470000h-47FFFFh
	SA75	64 Kwords	01001000XX	480000h-48FFFFh
	SA76	64 Kwords	01001001XX	490000h-49FFFFh
	SA77	64 Kwords	01001010XX	4A0000h-4AFFFFh
	SA78	64 Kwords	01001011XX	4B0000h-4BFFFFh
	SA79	64 Kwords	01001100XX	4C0000h-4CFFFFh
	SA80	64 Kwords	01001101XX	4D0000h-4DFFFFh
	SA81	64 Kwords	01001110XX	4E0000h-4EFFFFh
	SA82	64 Kwords	01001111XX	4F0000h-4FFFFFh

Table 20. WS256N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A23–A14	(x16) Address Range
Bank 5	SA83	64 Kwords	01010000XX	500000h-50FFFFh
	SA84	64 Kwords	01010001XX	510000h-51FFFFh
	SA85	64 Kwords	01010010XX	520000h-52FFFFh
	SA86	64 Kwords	01010011XX	530000h-53FFFFh
	SA87	64 Kwords	01010100XX	540000h-54FFFFh
	SA88	64 Kwords	01010101XX	550000h-55FFFFh
	SA89	64 Kwords	01010110XX	560000h-56FFFFh
	SA90	64 Kwords	01010111XX	570000h-57FFFFh
	SA91	64 Kwords	01011000XX	580000h-58FFFFh
	SA92	64 Kwords	01011001XX	590000h-59FFFFh
	SA93	64 Kwords	01011010XX	5A0000h-5AFFFFh
	SA94	64 Kwords	01011011XX	5B0000h-5BFFFFh
	SA95	64 Kwords	01011100XX	5C0000h-5CFFFFh
	SA96	64 Kwords	01011101XX	5D0000h-5DFFFFh
	SA97	64 Kwords	01011110XX	5E0000h-5EFFFFh
	SA98	64 Kwords	01011111XX	5F0000h-5FFFFFh
Bank 6	SA99	64 Kwords	01100000XX	600000h-60FFFFh
	SA100	64 Kwords	01100001XX	610000h-61FFFFh
	SA101	64 Kwords	01100010XX	620000h-62FFFFh
	SA102	64 Kwords	01100011XX	630000h-63FFFFh
	SA103	64 Kwords	01100100XX	640000h-64FFFFh
	SA104	64 Kwords	01100101XX	650000h-65FFFFh
	SA105	64 Kwords	01100110XX	660000h-66FFFFh
	SA106	64 Kwords	01100111XX	670000h-67FFFFh
	SA107	64 Kwords	01101000XX	680000h-68FFFFh
	SA108	64 Kwords	01101001XX	690000h-69FFFFh
	SA109	64 Kwords	01101010XX	6A0000h-6AFFFFh
	SA110	64 Kwords	01101011XX	6B0000h-6BFFFFh
	SA111	64 Kwords	01101100XX	6C0000h-6CFFFFh
	SA112	64 Kwords	01101101XX	6D0000h-6DFFFFh
	SA113	64 Kwords	01101110XX	6E0000h-6EFFFFh
	SA114	64 Kwords	01101111XX	6F0000h-6FFFFFh

Table 20. WS256N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A23–A14	(x16) Address Range
Bank 7	SA115	64 Kwords	01110000XX	700000h-70FFFFh
	SA116	64 Kwords	01110001XX	710000h-71FFFFh
	SA117	64 Kwords	01110010XX	720000h-72FFFFh
	SA118	64 Kwords	01110011XX	730000h-73FFFFh
	SA119	64 Kwords	01110100XX	740000h-74FFFFh
	SA120	64 Kwords	01110101XX	750000h-75FFFFh
	SA121	64 Kwords	01110110XX	760000h-76FFFFh
	SA122	64 Kwords	01110111XX	770000h-77FFFFh
	SA123	64 Kwords	01111000XX	780000h-78FFFFh
	SA124	64 Kwords	01111001XX	790000h-79FFFFh
	SA125	64 Kwords	01111010XX	7A0000h-7AFFFFh
	SA126	64 Kwords	01111011XX	7B0000h-7BFFFFh
	SA127	64 Kwords	01111100XX	7C0000h-7CFFFFh
	SA128	64 Kwords	01111101XX	7D0000h-7DFFFFh
	SA129	64 Kwords	01111110XX	7E0000h-7EFFFFh
	SA130	64 Kwords	01111111XX	7F0000h-7FFFFFh
Bank 8	SA131	64 Kwords	10000000XX	800000h-80FFFFh
	SA132	64 Kwords	10000001XX	810000h-81FFFFh
	SA133	64 Kwords	10000010XX	820000h-82FFFFh
	SA134	64 Kwords	10000011XX	830000h-83FFFFh
	SA135	64 Kwords	10000100XX	840000h-84FFFFh
	SA136	64 Kwords	10000101XX	850000h-85FFFFh
	SA137	64 Kwords	10000110XX	860000h-86FFFFh
	SA138	64 Kwords	10000111XX	870000h-87FFFFh
	SA139	64 Kwords	10001000XX	880000h-88FFFFh
	SA140	64 Kwords	10001001XX	890000h-89FFFFh
	SA141	64 Kwords	10001010XX	8A0000h-8AFFFFh
	SA142	64 Kwords	10001011XX	8B0000h-8BFFFFh
	SA143	64 Kwords	10001100XX	8C0000h-8CFFFFh
	SA144	64 Kwords	10001101XX	8D0000h-8DFFFFh
	SA145	64 Kwords	10001110XX	8E0000h-8EFFFFh
	SA146	64 Kwords	10001111XX	8F0000h-8FFFFFh

Table 20. WS256N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A23–A14	(x16) Address Range
Bank 9	SA147	64 Kwords	10010000XX	900000h-90FFFFh
	SA148	64 Kwords	10010001XX	910000h-91FFFFh
	SA149	64 Kwords	10010010XX	920000h-92FFFFh
	SA150	64 Kwords	10010011XX	930000h-93FFFFh
	SA151	64 Kwords	10010100XX	940000h-94FFFFh
	SA152	64 Kwords	10010101XX	950000h-95FFFFh
	SA153	64 Kwords	10010110XX	960000h-96FFFFh
	SA154	64 Kwords	10010111XX	970000h-97FFFFh
	SA155	64 Kwords	10011000XX	980000h-98FFFFh
	SA156	64 Kwords	10011001XX	990000h-99FFFFh
	SA157	64 Kwords	10011010XX	9A0000h-9AFFFFh
	SA158	64 Kwords	10011011XX	9B0000h-9BFFFFh
	SA159	64 Kwords	10011100XX	9C0000h-9CFFFFh
	SA160	64 Kwords	10011101XX	9D0000h-9DFFFFh
	SA161	64 Kwords	10011110XX	9E0000h-9EFFFFh
	SA162	64 Kwords	10011111XX	9F0000h-9FFFFFh
Bank 10	SA163	64 Kwords	10100000XX	A00000h-A0FFFFh
	SA164	64 Kwords	10100001XX	A10000h-A1FFFFh
	SA165	64 Kwords	10100010XX	A20000h-A2FFFFh
	SA166	64 Kwords	10100011XX	A30000h-A3FFFFh
	SA167	64 Kwords	10100100XX	A40000h-A4FFFFh
	SA168	64 Kwords	10100101XX	A50000h-A5FFFFh
	SA169	64 Kwords	10100110XX	A60000h-A6FFFFh
	SA170	64 Kwords	10100111XX	A70000h-A7FFFFh
	SA171	64 Kwords	10101000XX	A80000h-A8FFFFh
	SA172	64 Kwords	10101001XX	A90000h-A9FFFFh
	SA173	64 Kwords	10101010XX	AA0000h-AAFFFFh
	SA174	64 Kwords	10101011XX	AB0000h-ABFFFFh
	SA175	64 Kwords	10101100XX	AC0000h-ACFFFFh
	SA176	64 Kwords	10101101XX	AD0000h-ADFFFFh
	SA177	64 Kwords	10101110XX	AE0000h-AEFFFFh
	SA178	64 Kwords	10101111XX	AF0000h-AFFFFFh

Table 20. WS256N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A23–A14	(x16) Address Range
Bank 11	SA179	64 Kwords	10110000XX	B00000h-B0FFFFh
	SA180	64 Kwords	10110001XX	B10000h-B1FFFFh
	SA181	64 Kwords	10110010XX	B20000h-B2FFFFh
	SA182	64 Kwords	10110011XX	B30000h-B3FFFFh
	SA183	64 Kwords	10110100XX	B40000h-B4FFFFh
	SA184	64 Kwords	10110101XX	B50000h-B5FFFFh
	SA185	64 Kwords	10110110XX	B60000h-B6FFFFh
	SA186	64 Kwords	10110111XX	B70000h-B7FFFFh
	SA187	64 Kwords	10111000XX	B80000h-B8FFFFh
	SA188	64 Kwords	10111001XX	B90000h-B9FFFFh
	SA189	64 Kwords	10111010XX	BA0000h-BAFFFFh
	SA190	64 Kwords	10111011XX	BB0000h-BBFFFFh
	SA191	64 Kwords	10111100XX	BC0000h-BCFFFFh
	SA192	64 Kwords	10111101XX	BD0000h-BDFFFFh
	SA193	64 Kwords	10111110XX	BE0000h-BEFFFFh
	SA194	64 Kwords	10111111XX	BF0000h-BFFFFFh
Bank 12	SA195	64 Kwords	11000000XX	C00000h-C0FFFFh
	SA196	64 Kwords	11000001XX	C10000h-C1FFFFh
	SA197	64 Kwords	11000010XX	C20000h-C2FFFFh
	SA198	64 Kwords	11000011XX	C30000h-C3FFFFh
	SA199	64 Kwords	11000100XX	C40000h-C4FFFFh
	SA200	64 Kwords	11000101XX	C50000h-C5FFFFh
	SA201	64 Kwords	11000110XX	C60000h-C6FFFFh
	SA202	64 Kwords	11000111XX	C70000h-C7FFFFh
	SA203	64 Kwords	11001000XX	C80000h-C8FFFFh
	SA204	64 Kwords	11001001XX	C90000h-C9FFFFh
	SA205	64 Kwords	11001010XX	CA0000h-CAFFFFh
	SA206	64 Kwords	11001011XX	CB0000h-CBFFFFh
	SA207	64 Kwords	11001100XX	CC0000h-CCFFFFh
	SA208	64 Kwords	11001101XX	CD0000h-CDFFFFh
	SA209	64 Kwords	11001110XX	CE0000h-CEFFFFh
	SA210	64 Kwords	11001111XX	CF0000h-CFFFFFh

Table 20. WS256N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A23–A14	(x16) Address Range
Bank 13	SA211	64 Kwords	11010000XX	D00000h-D0FFFFh
	SA212	64 Kwords	11010001XX	D10000h-D1FFFFh
	SA213	64 Kwords	11010010XX	D20000h-D2FFFFh
	SA214	64 Kwords	11010011XX	D30000h-D3FFFFh
	SA215	64 Kwords	11010100XX	D40000h-D4FFFFh
	SA216	64 Kwords	11010101XX	D50000h-D5FFFFh
	SA217	64 Kwords	11010110XX	D60000h-D6FFFFh
	SA218	64 Kwords	11010111XX	D70000h-D7FFFFh
	SA219	64 Kwords	11011000XX	D80000h-D8FFFFh
	SA220	64 Kwords	11011001XX	D90000h-D9FFFFh
	SA221	64 Kwords	11011010XX	DA0000h-DAFFFFh
	SA222	64 Kwords	11011011XX	DB0000h-DBFFFFh
	SA223	64 Kwords	11011100XX	DC0000h-DCFFFFh
	SA224	64 Kwords	11011101XX	DD0000h-DDFFFFh
	SA225	64 Kwords	11011110XX	DE0000h-DEFFFFh
	SA226	64 Kwords	11011111XX	DF0000h-DFFFFFh
Bank 14	SA227	64 Kwords	11100000XX	E00000h-E0FFFFh
	SA228	64 Kwords	11100001XX	E10000h-E1FFFFh
	SA229	64 Kwords	11100010XX	E20000h-E2FFFFh
	SA230	64 Kwords	11100011XX	E30000h-E3FFFFh
	SA231	64 Kwords	11100100XX	E40000h-E4FFFFh
	SA232	64 Kwords	11100101XX	E50000h-E5FFFFh
	SA233	64 Kwords	11100110XX	E60000h-E6FFFFh
	SA234	64 Kwords	11100111XX	E70000h-E7FFFFh
	SA235	64 Kwords	11101000XX	E80000h-E8FFFFh
	SA236	64 Kwords	11101001XX	E90000h-E9FFFFh
	SA237	64 Kwords	11101010XX	EA0000h-EAFFFFh
	SA238	64 Kwords	11101011XX	EB0000h-EBFFFFh
	SA239	64 Kwords	11101100XX	EC0000h-ECFFFFh
	SA240	64 Kwords	11101101XX	ED0000h-EDFFFFh
	SA241	64 Kwords	11101110XX	EE0000h-EEFFFFh
	SA242	64 Kwords	11101111XX	EF0000h-EFFFFFh

Table 20. WS256N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A23–A14	(x16) Address Range
Bank 15	SA243	64 Kwords	11110000XX	F00000h-F0FFFFh
	SA244	64 Kwords	11110001XX	F10000h-F1FFFFh
	SA245	64 Kwords	11110010XX	F20000h-F2FFFFh
	SA246	64 Kwords	11110011XX	F30000h-F3FFFFh
	SA247	64 Kwords	11110100XX	F40000h-F4FFFFh
	SA248	64 Kwords	11110101XX	F50000h-F5FFFFh
	SA249	64 Kwords	11110110XX	F60000h-F6FFFFh
	SA250	64 Kwords	11110111XX	F70000h-F7FFFFh
	SA251	64 Kwords	11111000XX	F80000h-F8FFFFh
	SA252	64 Kwords	11111001XX	F90000h-F9FFFFh
	SA253	64 Kwords	11111010XX	FA0000h-FAFFFFh
	SA254	64 Kwords	11111011XX	FB0000h-FBFFFFh
	SA255	64 Kwords	11111100XX	FC0000h-FCFFFFh
	SA256	64 Kwords	11111101XX	FD0000h-FDFFFFh
	SA257	64 Kwords	11111110XX	FE0000h-FEFFFFh
	SA258	16 Kwords	1111111100	FF0000h-FF3FFFh
	SA259	16 Kwords	1111111101	FF4000h-FF7FFFh
	SA260	16 Kwords	1111111110	FF8000h-FFBFFFh
	SA261	16 Kwords	1111111111	FFC000h-FFFFFFh

Table 21. WS128N Sector & Memory Address Map

Bank	Sector	Sector Size	A22–A14	(x16) Address Range
Bank 0	SA0	16 Kwords	000000000	000000h-003FFFh
	SA1	16 Kwords	000000001	004000h-007FFFh
	SA2	16 Kwords	000000010	008000h-00BFFFh
	SA3	16 Kwords	000000011	00C000h-00FFFFh
	SA4	64 Kwords	0000001XX	010000h-01FFFFh
	SA5	64 Kwords	0000010XX	020000h-02FFFFh
	SA6	64 Kwords	0000011XX	030000h-03FFFFh
	SA7	64 Kwords	0000100XX	040000h-04FFFFh
	SA8	64 Kwords	0000101XX	050000h-05FFFFh
	SA9	64 Kwords	0000110XX	060000h-06FFFFh
	SA10	64 Kwords	0000111XX	070000h-07FFFFh
Bank 1	SA11	64 Kwords	0001000XX	080000h-08FFFFh
	SA12	64 Kwords	0001001XX	090000h-09FFFFh
	SA13	64 Kwords	0001010XX	0A0000h-0AFFFFh
	SA14	64 Kwords	0001011XX	0B0000h-0BFFFFh
	SA15	64 Kwords	0001100XX	0C0000h-0CFFFFh
	SA16	64 Kwords	0001101XX	0D0000h-0DFFFFh
	SA17	64 Kwords	0001110XX	0E0000h-0EFFFFh
	SA18	64 Kwords	0001111XX	0F0000h-0FFFFFh

Table 21. WS128N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A22–A14	(x16) Address Range
Bank 2	SA19	64 Kwords	0010000XX	100000h-10FFFFh
	SA20	64 Kwords	0010001XX	110000h-11FFFFh
	SA21	64 Kwords	0010010XX	120000h-12FFFFh
	SA22	64 Kwords	0010011XX	130000h-13FFFFh
	SA23	64 Kwords	0010100XX	140000h-14FFFFh
	SA24	64 Kwords	0010101XX	150000h-15FFFFh
	SA25	64 Kwords	0010110XX	160000h-16FFFFh
	SA26	64 Kwords	0010111XX	170000h-17FFFFh
Bank 3	SA27	64 Kwords	0011000XX	180000h-18FFFFh
	SA28	64 Kwords	0011001XX	190000h-19FFFFh
	SA29	64 Kwords	0011010XX	1A0000h-1AFFFFh
	SA30	64 Kwords	0011011XX	1B0000h-1BFFFFh
	SA31	64 Kwords	0011100XX	1C0000h-1CFFFFh
	SA32	64 Kwords	0011101XX	1D0000h-1DFFFFh
	SA33	64 Kwords	0011110XX	1E0000h-1EFFFFh
	SA34	64 Kwords	0011111XX	1F0000h-1FFFFFh
Bank 4	SA35	64 Kwords	0100000XX	200000h-20FFFFh
	SA36	64 Kwords	0100001XX	210000h-21FFFFh
	SA37	64 Kwords	0100010XX	220000h-22FFFFh
	SA38	64 Kwords	0100011XX	230000h-23FFFFh
	SA39	64 Kwords	0100100XX	240000h-24FFFFh
	SA40	64 Kwords	0100101XX	250000h-25FFFFh
	SA41	64 Kwords	0100110XX	260000h-26FFFFh
	SA42	64 Kwords	0100111XX	270000h-27FFFFh
Bank 5	SA43	64 Kwords	0101000XX	280000h-28FFFFh
	SA44	64 Kwords	0101001XX	290000h-29FFFFh
	SA45	64 Kwords	0101010XX	2A0000h-2AFFFFh
	SA46	64 Kwords	0101011XX	2B0000h-2BFFFFh
	SA47	64 Kwords	0101100XX	2C0000h-2CFFFFh
	SA48	64 Kwords	0101101XX	2D0000h-2DFFFFh
	SA49	64 Kwords	0101110XX	2E0000h-2EFFFFh
	SA50	64 Kwords	0101111XX	2F0000h-2FFFFFh
Bank 6	SA51	64 Kwords	0110000XX	300000h-30FFFFh
	SA52	64 Kwords	0110001XX	310000h-31FFFFh
	SA53	64 Kwords	0110010XX	320000h-32FFFFh
	SA54	64 Kwords	0110011XX	330000h-33FFFFh
	SA55	64 Kwords	0110100XX	340000h-34FFFFh
	SA56	64 Kwords	0110101XX	350000h-35FFFFh
	SA57	64 Kwords	0110110XX	360000h-36FFFFh
	SA58	64 Kwords	0110111XX	370000h-37FFFFh

Table 21. WS128N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A22–A14	(x16) Address Range
Bank 7	SA59	64 Kwords	0111000XX	380000h-38FFFFh
	SA60	64 Kwords	0111001XX	390000h-39FFFFh
	SA61	64 Kwords	0111010XX	3A0000h-3AFFFFh
	SA62	64 Kwords	0111011XX	3B0000h-3BFFFFh
	SA63	64 Kwords	0111100XX	3C0000h-3CFFFFh
	SA64	64 Kwords	0111101XX	3D0000h-3DFFFFh
	SA65	64 Kwords	0111110XX	3E0000h-3EFFFFh
	SA66	64 Kwords	0111111XX	3F0000h-3FFFFFh
Bank 8	SA67	64 Kwords	1000000XX	400000h-40FFFFh
	SA68	64 Kwords	1000001XX	410000h-41FFFFh
	SA69	64 Kwords	1000010XX	420000h-42FFFFh
	SA70	64 Kwords	1000011XX	430000h-43FFFFh
	SA71	64 Kwords	1000100XX	440000h-44FFFFh
	SA72	64 Kwords	1000101XX	450000h-45FFFFh
	SA73	64 Kwords	1000110XX	460000h-46FFFFh
	SA74	64 Kwords	1000111XX	470000h-47FFFFh
Bank 9	SA75	64 Kwords	1001000XX	480000h-48FFFFh
	SA76	64 Kwords	1001001XX	490000h-49FFFFh
	SA77	64 Kwords	1001010XX	4A0000h-4AFFFFh
	SA78	64 Kwords	1001011XX	4B0000h-4BFFFFh
	SA79	64 Kwords	1001100XX	4C0000h-4CFFFFh
	SA80	64 Kwords	1001101XX	4D0000h-4DFFFFh
	SA81	64 Kwords	1001110XX	4E0000h-4EFFFFh
	SA82	64 Kwords	1001111XX	4F0000h-4FFFFFh
Bank 10	SA83	64 Kwords	1010000XX	500000h-50FFFFh
	SA84	64 Kwords	1010001XX	510000h-51FFFFh
	SA85	64 Kwords	1010010XX	520000h-52FFFFh
	SA86	64 Kwords	1010011XX	530000h-53FFFFh
	SA87	64 Kwords	1010100XX	540000h-54FFFFh
	SA88	64 Kwords	1010101XX	550000h-55FFFFh
	SA89	64 Kwords	1010110XX	560000h-56FFFFh
	SA90	64 Kwords	1010111XX	570000h-57FFFFh
Bank 11	SA91	64 Kwords	1011000XX	580000h-58FFFFh
	SA92	64 Kwords	1011001XX	590000h-59FFFFh
	SA93	64 Kwords	1011010XX	5A0000h-5AFFFFh
	SA94	64 Kwords	1011011XX	5B0000h-5BFFFFh
	SA95	64 Kwords	1011100XX	5C0000h-5CFFFFh
	SA96	64 Kwords	1011101XX	5D0000h-5DFFFFh
	SA97	64 Kwords	1011110XX	5E0000h-5EFFFFh
	SA98	64 Kwords	1011111XX	5F0000h-5FFFFFh

Table 21. WS128N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A22–A14	(x16) Address Range
Bank 12	SA99	64 Kwords	1100000XX	600000h-60FFFFh
	SA100	64 Kwords	1100001XX	610000h-61FFFFh
	SA101	64 Kwords	1100010XX	620000h-62FFFFh
	SA102	64 Kwords	1100011XX	630000h-63FFFFh
	SA103	64 Kwords	1100100XX	640000h-64FFFFh
	SA104	64 Kwords	1100101XX	650000h-65FFFFh
	SA105	64 Kwords	1100110XX	660000h-66FFFFh
	SA106	64 Kwords	1100111XX	670000h-67FFFFh
Bank 13	SA107	64 Kwords	1101000XX	680000h-68FFFFh
	SA108	64 Kwords	1101001XX	690000h-69FFFFh
	SA109	64 Kwords	1101010XX	6A0000h-6AFFFFh
	SA110	64 Kwords	1101011XX	6B0000h-6BFFFFh
	SA111	64 Kwords	1101100XX	6C0000h-6CFFFFh
	SA112	64 Kwords	1101101XX	6D0000h-6DFFFFh
	SA113	64 Kwords	1101110XX	6E0000h-6EFFFFh
	SA114	64 Kwords	1101111XX	6F0000h-6FFFFFh
Bank 14	SA115	64 Kwords	1110000XX	700000h-70FFFFh
	SA116	64 Kwords	1110001XX	710000h-71FFFFh
	SA117	64 Kwords	1110010XX	720000h-72FFFFh
	SA118	64 Kwords	1110011XX	730000h-73FFFFh
	SA119	64 Kwords	1110100XX	740000h-74FFFFh
	SA120	64 Kwords	1110101XX	750000h-75FFFFh
	SA121	64 Kwords	1110110XX	760000h-76FFFFh
	SA122	64 Kwords	1110111XX	770000h-77FFFFh
Bank 15	SA123	64 Kwords	1111000XX	780000h-78FFFFh
	SA124	64 Kwords	1111001XX	790000h-79FFFFh
	SA125	64 Kwords	1111010XX	7A0000h-7AFFFFh
	SA126	64 Kwords	1111011XX	7B0000h-7BFFFFh
	SA127	64 Kwords	1111100XX	7C0000h-7CFFFFh
	SA128	64 Kwords	1111101XX	7D0000h-7DFFFFh
	SA129	64 Kwords	1111110XX	7E0000h-7EFFFFh
	SA130	16 Kwords	111111100	7F0000h-7F3FFFh
	SA131	16 Kwords	111111101	7F4000h-7F7FFFh
	SA132	16 Kwords	111111110	7F8000h-7FBFFFh
	SA133	16 Kwords	111111111	7FC000h-7FFFFFh

Table 22. WS064N Sector & Memory Address Map

Bank	Sector	Sector Size	A21–A14	(x16) Address Range
Bank 0	SA0	16 Kwords	00000000	000000h-003FFFh
	SA1	16 Kwords	00000001	004000h-007FFFh
	SA2	16 Kwords	00000010	008000h-00BFFFh
	SA3	16 Kwords	00000011	00C000h-00FFFFh
	SA4	64 Kwords	000001XX	010000h-01FFFFh
	SA5	64 Kwords	000010XX	020000h-02FFFFh
	SA6	64 Kwords	000011XX	030000h-03FFFFh
Bank 1	SA7	64 Kwords	000100XX	040000h-04FFFFh
	SA8	64 Kwords	000101XX	050000h-05FFFFh
	SA9	64 Kwords	000110XX	060000h-06FFFFh
	SA10	64 Kwords	000111XX	070000h-07FFFFh
Bank 2	SA11	64 Kwords	001000XX	080000h-08FFFFh
	SA12	64 Kwords	001001XX	090000h-09FFFFh
	SA13	64 Kwords	001010XX	0A0000h-0AFFFFh
	SA14	64 Kwords	001011XX	0B0000h-0BFFFFh
Bank 3	SA15	64 Kwords	001100XX	0C0000h-0CFFFFh
	SA16	64 Kwords	001101XX	0D0000h-0DFFFFh
	SA17	64 Kwords	001110XX	0E0000h-0EFFFFh
	SA18	64 Kwords	001111XX	0F0000h-0FFFFFh
Bank 4	SA19	64 Kwords	010000XX	100000h-10FFFFh
	SA20	64 Kwords	010001XX	110000h-11FFFFh
	SA21	64 Kwords	010010XX	120000h-12FFFFh
	SA22	64 Kwords	010011XX	130000h-13FFFFh
Bank 5	SA23	64 Kwords	010100XX	140000h-14FFFFh
	SA24	64 Kwords	010101XX	150000h-15FFFFh
	SA25	64 Kwords	010110XX	160000h-16FFFFh
	SA26	64 Kwords	010111XX	170000h-17FFFFh
Bank 6	SA27	64 Kwords	011000XX	180000h-18FFFFh
	SA28	64 Kwords	011001XX	190000h-19FFFFh
	SA29	64 Kwords	011010XX	1A0000h-1AFFFFh
	SA30	64 Kwords	011011XX	1B0000h-1BFFFFh
Bank 7	SA31	64 Kwords	011100XX	1C0000h-1CFFFFh
	SA32	64 Kwords	011101XX	1D0000h-1DFFFFh
	SA33	64 Kwords	011110XX	1E0000h-1EFFFFh
	SA34	64 Kwords	011111XX	1F0000h-1FFFFFh
Bank 8	SA35	64 Kwords	100000XX	200000h-20FFFFh
	SA36	64 Kwords	100001XX	210000h-21FFFFh
	SA37	64 Kwords	100010XX	220000h-22FFFFh
	SA38	64 Kwords	100011XX	230000h-23FFFFh

Table 22. WS064N Sector & Memory Address Map (Continued)

Bank	Sector	Sector Size	A21–A14	(x16) Address Range
Bank 9	SA39	64 Kwords	100100XX	240000h-24FFFFh
	SA40	64 Kwords	100101XX	250000h-25FFFFh
	SA41	64 Kwords	100110XX	260000h-26FFFFh
	SA42	64 Kwords	100111XX	270000h-27FFFFh
Bank 10	SA43	64 Kwords	101000XX	280000h-28FFFFh
	SA44	64 Kwords	101001XX	290000h-29FFFFh
	SA45	64 Kwords	101010XX	2A0000h-2AFFFFh
	SA46	64 Kwords	101011XX	2B0000h-2BFFFFh
Bank 11	SA47	64 Kwords	101100XX	2C0000h-2CFFFFh
	SA48	64 Kwords	101101XX	2D0000h-2DFFFFh
	SA49	64 Kwords	101110XX	2E0000h-2EFFFFh
	SA50	64 Kwords	101111XX	2F0000h-2FFFFFh
Bank 12	SA51	64 Kwords	110000XX	300000h-30FFFFh
	SA52	64 Kwords	110001XX	310000h-31FFFFh
	SA53	64 Kwords	110010XX	320000h-32FFFFh
	SA54	64 Kwords	110011XX	330000h-33FFFFh
Bank 13	SA55	64 Kwords	110100XX	340000h-34FFFFh
	SA56	64 Kwords	110101XX	350000h-35FFFFh
	SA57	64 Kwords	110110XX	360000h-36FFFFh
	SA58	64 Kwords	110111XX	370000h-37FFFFh
Bank 14	SA59	64 Kwords	111000XX	380000h-38FFFFh
	SA60	64 Kwords	111001XX	390000h-39FFFFh
	SA61	64 Kwords	111010XX	3A0000h-3AFFFFh
	SA62	64 Kwords	111011XX	3B0000h-3BFFFFh
Bank 15	SA63	64 Kwords	111100XX	3C0000h-3CFFFFh
	SA64	64 Kwords	111101XX	3D0000h-3DFFFFh
	SA65	64 Kwords	111110XX	3E0000h-3EFFFFh
	SA66	16 Kwords	11111100	3F0000h-3F3FFFh
	SA67	16 Kwords	11111101	3F4000h-3F7FFFh
	SA68	16 Kwords	11111110	3F8000h-3FBFFFh
	SA69	16 Kwords	11111111	3FC000h-3FFFFFh

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. The Command Definition Summary section defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data. See "AC Characteristics—Synchronous" and "AC Characteristics—Asynchronous" for timing diagrams.

Reading Array Data

The device is automatically set to reading asynchronous array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data from any non-erase-suspended sector within the same bank. See Erase Suspend/Erase Resume Commands for more information.

After the device accepts a Program Suspend command, the corresponding bank enters the program-suspend-read mode, after which the system can read data from any non-program-suspended sector within the same bank. See Program Suspend/Program Resume Commands for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See Reset Command for more information. If DQ1 goes high during Write Buffer Programming, the system must issue the Write Buffer Abort Reset command.

See also Requirements for Asynchronous (Non-Burst) Read Operation and Requirements for Synchronous (Burst) Read Operation for more information. The Asynchronous Read and Synchronous/Burst Read tables provide the read parameters, and Figure 14, and Figure 18 show the timings.

Set Configuration Register Command Sequence

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, RDY configuration, and synchronous mode active (see Figure 26 for details). The configuration register must be set before the device will enter burst mode. On power up or reset, the device is set in asynchronous read mode and the configuration register is reset. The configuration register is not reset after deasserting CE#.

The configuration register is loaded with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be D0h and address bits should be 555h. During the fourth cycle, the configuration code should be entered onto the data bus with the address bus set to address 000h. Once the data has been programmed into the configuration register, a software reset command is required to set the device into the correct state. The device will power up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The configuration register can not be changed during device operations (program, erase, or sector lock).

Read Configuration Register Command Sequence

The configuration register can be read with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C6h and address bits should be 555h. During the fourth cycle, the configuration code should be read out of the data bus with the address bus set to address 000h. Once the data has been read from the configuration register, a software reset command is required to set the device into the array read mode.

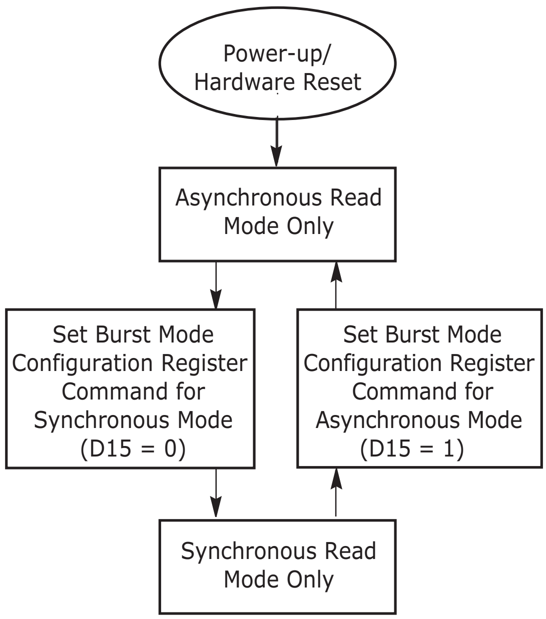


Figure 1. Synchronous/Asynchronous State Diagram

Read Mode Setting

This setting allows the system to enable or disable burst mode during system operations. **Configuration Bit CR15** determines this setting: "1' for asynchronous mode, "0" for synchronous mode.

Programmable Wait State Configuration

The programmable wait state feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. **Configuration Bit CR13–CR11** determine the setting (see Table 23).

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Table 23. Programmable Wait State Settings

CR13	CR12	CR11	Total Initial Access Cycles
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7 (default)
1	1	0	Reserved
1	1	1	Reserved

Notes:
1. *Upon power-up or hardware reset, the default setting is seven wait states.*
2. *RDY will default to being active with data when the Wait State Setting is set to a total initial access cycle of 2.*

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

Programmable Wait State

If the device is equipped with the handshaking option, the host system should set **CR13-CR11** to 010 for a clock frequency of 54 MHz, to 011 for a clock frequency of 66 MHz, or to 100 for a clock frequency of 80 MHz for the system/device to execute at maximum speed.

Table 24 describes the typical number of clock cycles (wait states) for various conditions.

Boundary Crossing Latency

If the device is operating above 66 MHz, an additional wait state must be inserted to account for boundary crossing latency. This is done by setting **CR14** to a '1' (default). If the device is operating at or below 66 MHz, the additional wait state for boundary crossing is not needed. Therefore the **CR14** can be changed to a '0' to remove boundary crossing latency.

Table 24. Wait States for Handshaking

Conditions at Address	Typical No. of Clock Cycles after AVD# Low		
	54 MHz	66 MHz	80 MHz
Initial address (V_{IO} = 1.8 V)	4	5	6

Handshaking

For optimal burst mode performance, the host system must set the appropriate number of wait states in the flash device depending on the clock frequency.

The autoselect function allows the host system to determine whether the flash device is enabled for handshaking. See Autoselect Command Sequence for more information.

Burst Length Configuration

The device supports four different read modes: continuous mode, and 8, 16, and 32 word linear with or without wrap around modes. A continuous sequence (default) begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear read with wrap around begins on the starting address written to the device and then advances to the next 8 word boundary. The address pointer then returns to the 1st word after the previous eight word boundary, wrapping through the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

Table 25 shows the **CR2-CR0** and settings for the four read modes.

Table 25. Burst Length Configuration

Burst Modes	Address Bits		
	CR2	**CR1**	**CR0**
Continuous	0	0	0
8-word linear	0	1	0
16-word linear	0	1	1
32-word linear	1	0	0

Note: *Upon power-up or hardware reset the default setting is continuous.*

Burst Wrap Around

By default, the device will perform burst wrap around with **CR3** set to a '1'. Changing the **CR3** to a '0' disables burst wrap around.

RDY Configuration

By default, the device is set so that the RDY pin will output V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. **CR8** determines this setting; "1" for RDY active (default) with data, "0" for RDY active one clock cycle before valid data.

RDY Polarity

By default, the RDY pin will always indicate that the device is ready to handle a new transaction with **CR10** set to a '1'. In this case, the RDY pin is active high. Changing the **CR10** to a '0' sets the RDY pin to be active low. In this case, the RDY pin will always indicate that the device is ready to handle a new transaction when low.

Configuration Register

Table 26 shows the address bits that determine the configuration register settings for various device functions.

Table 26. Configuration Register

CR Bit	Function	Settings (Binary)
CR15	Set Device Read Mode	0 = Synchronous Read (Burst Mode) Enabled 1 = Asynchronous Mode (default)
CR14	Boundary Crossing	0 = No extra boundary crossing latency 1 = With extra boundary crossing latency (default)
CR13 CR12 CR11	Programmable Wait State	000 = Data is valid on the 2nd active CLK edge after addresses are latched 001 = Data is valid on the 3rd active CLK edge after addresses are latched 010 = Data is valid on the 4th active CLK edge after addresses are latched 011 = Data is valid on the 5th active CLK edge after addresses are latched 100 = Data is valid on the 6th active CLK edge after addresses are latched 101 = Data is valid on the 7th active CLK edge after addresses are latched (default) 110 = Reserved 111 = Reserved
CR10	RDY Polarity	0 = RDY signal is active low 1 = RDY signal is active high (default)
CR9	Reserved	1 = default
CR8	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data (default)
CR7	Reserved	1 = default
CR6	Reserved	1 = default
CR5	Reserved	0 = default
CR4	Reserved	0 = default
CR3	Burst Wrap Around	0 = No Wrap Around Burst 1 = Wrap Around Burst (default)
CR2 CR1 CR0	Burst Length	000 = Continuous (default) 010 = 8-Word Linear Burst 011 = 16-Word Linear Burst 100 = 32-Word Linear Burst (All other bit settings are reserved)

Note: *Device will be in the default state upon power-up or hardware reset.*

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. **Once erasure begins, however, the device ignores reset commands until the operation is complete.**

The reset command may be written between the sequence cycles in a program command sequence before programming begins (prior to the third cycle). This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. **Once programming begins, however, the device ignores reset commands until the operation is complete.**

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend and program-suspend-read mode if that bank was in Program Suspend).

Note: If DQ1 goes high during a Write Buffer Programming operation, the system must write the "Write to Buffer Abort Reset" command sequence to RESET the device to reading array data. The standard RESET command will not work. See Table 17 for details on this command sequence.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The Command Definition Summary shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank. Autoselect does not support simultaneous operations nor burst mode.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. Read commands to other banks will return data from the array. Writes to other banks is not allowed. The following table describes the address requirements for the various autoselect functions, and the resulting data. BA represents the bank address. The device ID is read in three cycles.

Table 27. Autoselect Addresses

Description	Address	Read Data
Manufacturer ID	(BA) + 00h	0001h
Device ID, Word 1	(BA) + 01h	227Eh
Device ID, Word 2	(BA) + 0Eh	2230 (WS256N) 2232 (WS064N) 2231 (WS128N)
Device ID, Word 3	(BA) + 0Fh	2200
Indicator Bits	(BA) + 03h	DQ15 - DQ8 = Reserved DQ7 (Factory Lock Bit): 1 = Locked, 0 = Not Locked DQ6 (Customer Lock Bit): 1 = Locked, 0 = Not Locked DQ5 (Handshake Bit): 1 = Reserved, 0 = Standard Handshake DQ4, DQ3 (WP# Protection Boot Code): 00 = WP# Protects both Top Boot and Bottom Boot Sectors. 01, 10, 11 = Reserved DQ2 = Reserved DQ1 (DYB Power up State [Lock Register DQ4]): 1 = Unlocked (user option), 0 = Locked (default) DQ0 (PPB Eraseability [Lock Register DQ3]): 1 = Erase allowed, 0 = Erase disabled
Sector Block Lock/ Unlock	(SA) + 02h	0001h = Locked, 0000h = Unlocked

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter SecSi™ Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. The SecSi Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. See Command Definition Summary for address and data requirements for both command sequences.

Word Program Command Sequence

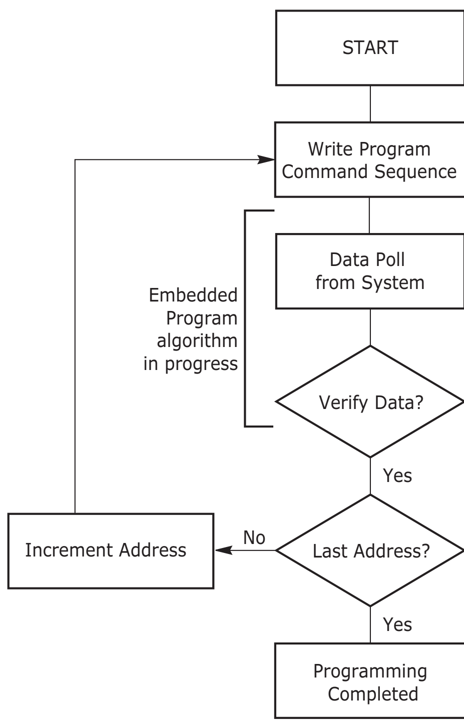
Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin (see Figure 2).

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored except the Program Suspend command. ***Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program***

operation is in progress. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. Programming to the same word address multiple times without intervening erases is limited. For such application requirements, please contact your local Spansion representative. **A "0" cannot be programmed back to a "1."** Attempting to do so will cause the device to set DQ5 = 1 (halting any further operation and requiring a reset command). A succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."



Note: *See Command Definition Summary for program command sequence.*

Figure 2. Word Program Operation

Write Buffer Programming Command Sequence

Write Buffer Programming Command Sequence allows for faster programming compared to the standard Program Command Sequence. Write Buffer Programming allows the system to write 32 words in one programming operation. See Write Buffer Programming Operation section for the program command sequence.

Table 28. Write Buffer Command Sequence

Sequence	Address	Data	Comment
Unlock Command 1	555	00AA	Not required in the Unlock Bypass mode
Unlock Command 2	2AA	0055	Same as above
Write Buffer Load	Starting Address	0025h	
Specify the Number of Program Locations	Starting Address	Word Count	Number of locations to program minus 1 (must be 32 - 1 = 31)
Load 1st data word	Starting Address	Program Data	All addresses must be within write-buffer-page boundaries, but do not have to be loaded in any order
Load next data word	Write Buffer Location	Program Data	Same as above
...	...	...	Same as above
Load last data word	Write Buffer Location	Program Data	Same as above
Write Buffer Program Confirm	Sector Address	0029h	This command must follow the last write buffer location loaded, or the operation will ABORT
Device goes busy			
Status monitoring through DQ pins (Perform Data Bar Polling on the **Last Loaded Address**)			

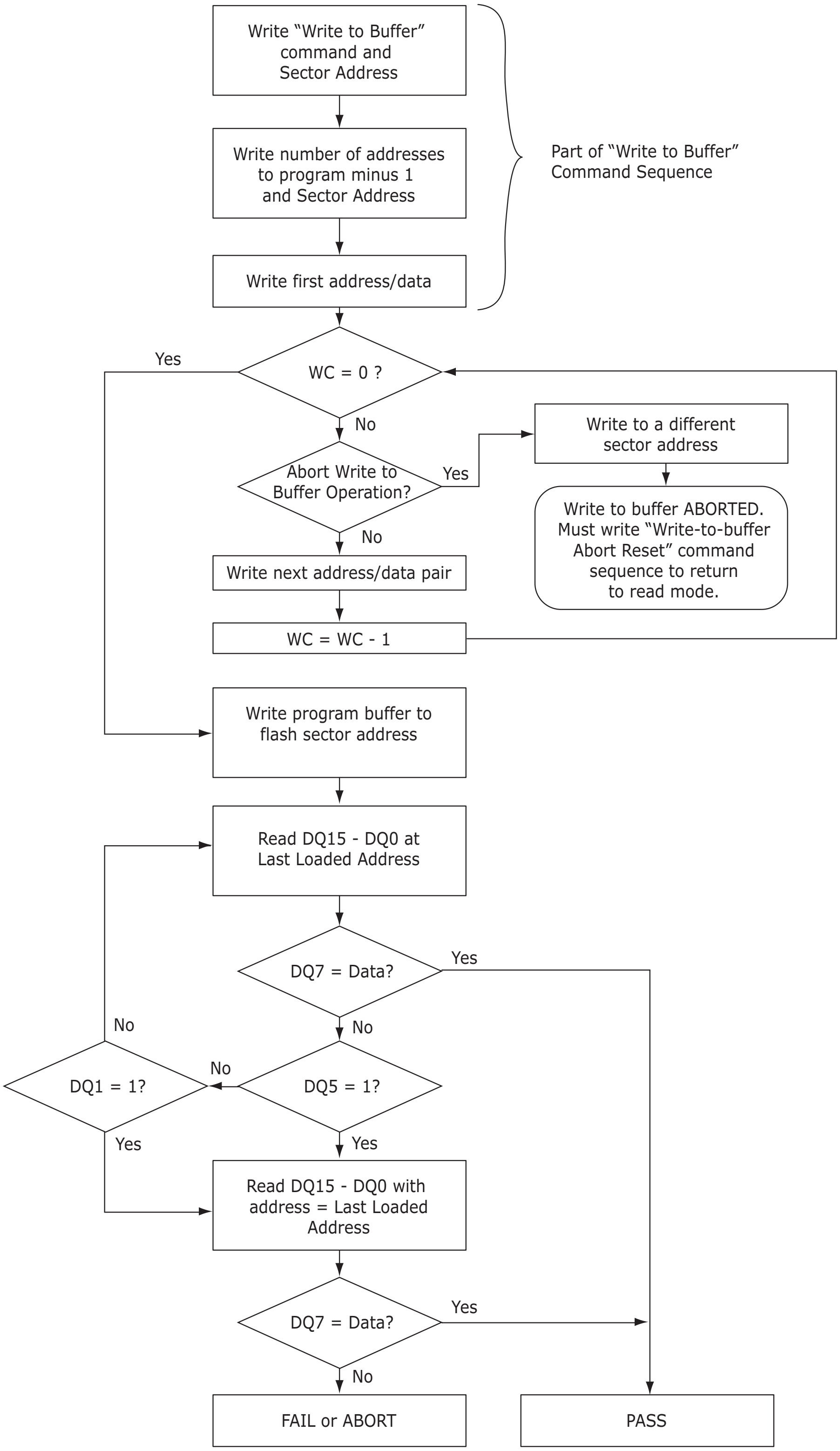


Figure 3. Write Buffer Programming Operation

Unlock Bypass Command Sequence

The unlock bypass feature allows faster programming than the standard word program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. See Command Definition Summary for the unlock bypass command sequences requirements.

During the unlock bypass mode, only the Read, Unlock Bypass Program, and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. See Command Definition Summary for chip erase command sequence address and data requirements.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. See Write Operation Status for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. See Erase/Program Timing Operations for parameters and timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. See Command Definition Summary for sector erase command sequence address and data requirements.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

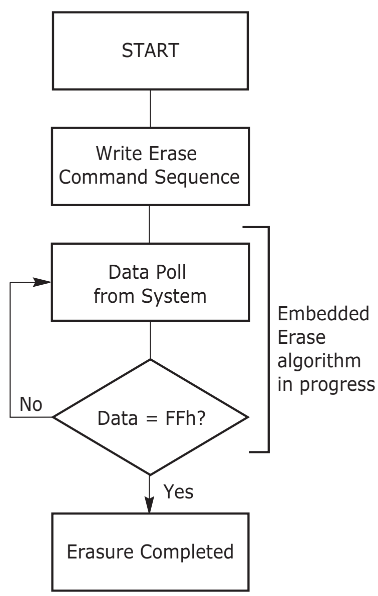
After the command sequence is written, a sector erase time-out of no less than t_{SEA} occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than t_{SEA}. Any sector erase address and command following the exceeded time-out (t_{SEA}) may or may not be accepted. Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See DQ3: Sector Erase Timer.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing banks. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2 in the erasing bank. See Write Operation Status for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. See Erase/Program Timing Operations for parameters and timing diagrams.



Notes:
1. *See Command Definition Summary for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 4. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the t_{SEA} time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation.

When the Erase Suspend command is written during the sector erase operation, the device requires t_{SEL} (erase suspend latency) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to Table 32 for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. See Write Buffer Programming Operation and the Autoselect Command Sequence for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt an embedded programming operation or a "Write to Buffer" programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL} (program suspend latency) and updates the status bits. Addresses are "don't-cares" when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area, then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in Program Suspend mode. The device allows reading autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system must write the Program Resume command (address bits are "don't care") to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

Lock Register Command Set Definitions

The Lock Register Command Set permits the user to program the SecSi Sector Protection Bit, Persistent Protection Mode Lock Bit, or Password Protection Mode Lock Bit one time. The Lock Command Set also allows for the reading of the SecSi Sector Protection Bit, Persistent Protection Mode Lock Bit, or Password Protection Mode Lock Bit.

The **Lock Register Command Set Entry** command sequence must be issued prior to any of the following commands to enable proper command execution.

- Lock Register Program Command
- Lock Register Read Command
- Lock Register Exit Command

Note that issuing the Lock Register Command Set Entry command disables reads and writes for Bank 0. Reads from other banks excluding Bank 0 are allowed.

The Lock Register Command Set Exit command **must** be issued after the execution of the commands to reset the device to read mode, and re-enables reads and writes for Bank 0.

Note that if the Persistent Protection Mode Locking Bit and the Password Protection Mode Locking Bit are programmed at the same time, neither will be programmed.

Password Protection Command Set Definitions

The Password Protection Command Set permits the user to program the 64-bit password, verify the programming of the 64-bit password, and then later unlock the device by issuing the valid 64-bit password.

The **Password Protection Command Set Entry** command sequence must be issued prior to any of the following commands to enable proper command execution.

- Password Program Command
- Password Read Command
- Password Unlock Command

Note that issuing the **Password Protection Command Set Entry** command disables reads and writes for Bank 0. Reads and writes for other banks excluding Bank 0 are allowed.

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64 bits long. There is no special addressing order required for programming the password.

Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm with the cell remaining as a "0". The password is all "1"s when shipped from the factory. All 64-bit password combinations are valid as a password.

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all "1"s onto the DQ data bus.

The lower two address bits (A1–A0) are valid during the Password Read, Password Program, and Password Unlock.

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 1 µs at a time to prevent a hacker from running through all the 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 1 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. The password is 64 bits long. A1 and A0 are used for matching. Writing the Password Unlock command does not need to be address order specific. An example sequence is starting with the lower address A1–A0= 00, followed by A1–A0= 01, A1–A0= 10, and A1–A0= 11.

Approximately 1 µSec is required for unlocking the device after the valid 64-bit password is given to the device. It is the responsibility of the microprocessor to keep track of the 64-bit password as it is entered with the Password Unlock command, the order, and when to read the PPB Lock bit to confirm successful password unlock. In order to re-lock the device into the Password Mode, the PPB Lock Bit Set command can be re-issued.

The **Password Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode, otherwise the device will hang. Note that issuing the **Password Protection Command Set Exit** command re-enables reads and writes for Bank 0.

Non-Volatile Sector Protection Command Set Definitions

The Non-Volatile Sector Protection Command Set permits the user to program the Persistent Protection Bits (PPBs), erase all of the Persistent Protection Bits (PPBs), and read the logic state of the Persistent Protection Bits (PPBs).

The **Non-Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the following commands to enable proper command execution.

- PPB Program Command
- All PPB Erase Command
- PPB Status Read Command

Note that issuing the **Non-Volatile Sector Protection Command Set Entry** command disables reads and writes for the bank selected. Reads within that bank will return the PPB status for that sector. Reads from other banks are allowed; writes are not allowed. All Reads must be performed using the Asynchronous mode.

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (A23–A14 WS256N, A22–A14 WS128N, A21–A14 WS064N) are written at the same time as the program command. If the PPB Lock Bit is set, the PPB Program command will not execute and the command will time-out without programming the PPB.

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written, all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs.

The device will preprogram all PPBs prior to erasing when issuing the All PPB Erase command. Also note that the total number of PPB program/erase cycles has the same endurance as the flash memory array.

The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Command to the device.

The **Non-Volatile Sector Protection Command Set Exit** command **must** be issued after the execution of the commands listed previously to reset the device to read mode. Note that issuing the **Non-Volatile Sector Protection Command Set Exit** command re-enables reads and writes for Bank 0.

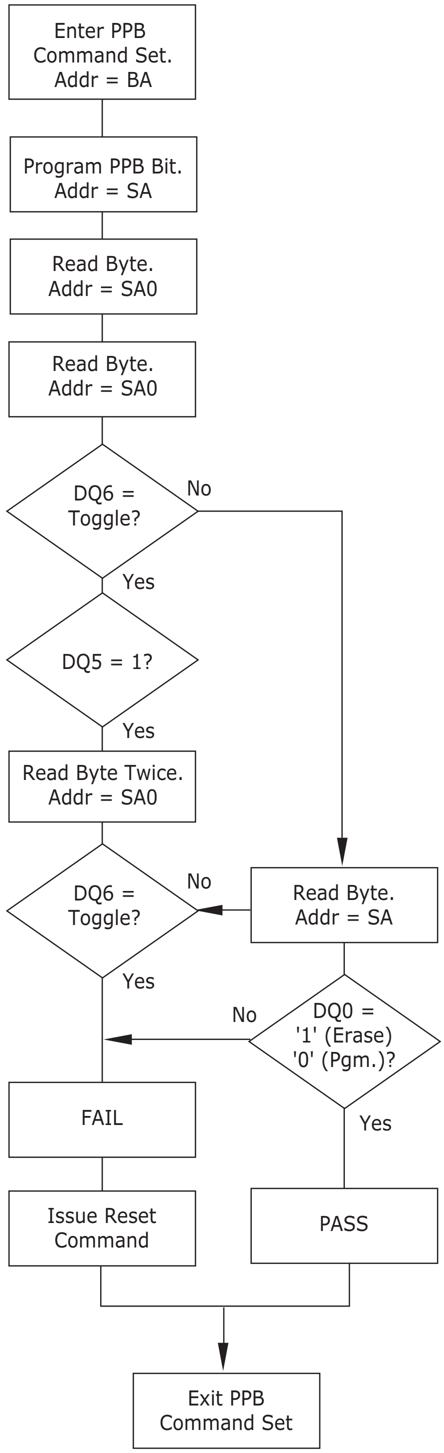


Figure 5. PPB Program/Erase Algorithm

Global Volatile Sector Protection Freeze Command Set

The Global Volatile Sector Protection Freeze Command Set permits the user to set the PPB Lock Bit and read the logic state of the PPB Lock Bit.

The **Volatile Sector Protection Freeze Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution:

- PPB Lock Bit Set Command
- PPB Lock Bit Status Read Command

Reads from all remaining 15 banks are allowed.

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear (for Persistent Sector Protection Mode) or the Password Unlock command is executed (for Password Sector Protection Mode). If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle.

The programming state of the PPB Lock Bit can be verified by executing a PPB Lock Bit Status Read Command to the device.

The **Global Volatile Sector Protection Freeze Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Volatile Sector Protection Command Set

The Volatile Sector Protection Command Set permits the user to set the Dynamic Protection Bit (DYB), clear the Dynamic Protection Bit (DYB), and read the logic state of the Dynamic Protection Bit (DYB).

The **Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the following commands to enable proper command execution.

- DYB Set Command
- DYB Clear Command
- DYB Status Read Command

Note that issuing the **Volatile Sector Protection Command Set Entry** command disables reads and writes for the bank selected with the command. Reads within that bank will return the DYB status for that sector. Writes within that bank will set the DYB for that sector. Reads for other banks excluding that bank are allowed; writes are not allowed. All Reads must be performed using the Asynchronous mode.

The DYB Set/Clear command is used to set or clear a DYB for a given sector. The high order address bits (A23–A14 for the WS256N, A22–A14 for the WS128N, A21–A14 for the WS064N) are issued at the same time as the code 00h or 01h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are cleared at power-up or hardware reset.

The programming state of the DYB for a given sector can be verified by writing a DYB Status Read Command to the device.

The **Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode. Note that issuing the **Volatile Sector Protection Command Set Exit** command re-enables reads and writes for Bank 0.

SecSi Sector Entry Command

The SecSi Sector Entry Command allows the following commands to be executed

- Read from SecSi Sector
- Program to SecSi Sector

Sector 0 is remapped from memory array to SecSi Sector array. Reads can be performed using the Asynchronous or Synchronous mode. Burst mode reads within SecSi Sector will wrap from address FFh back to address 00h. Reads outside of sector 0 will return memory array data. Continuous burst read past the maximum address is undefined.

Simultaneous operations are allowed except for Bank 0. Once the SecSi Sector Entry Command is issued, the SecSi Sector Exit command has to be issued to exit SecSi Sector Mode.

Command Definition Summary

Table 29. Memory Array Commands

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (6)		1	RA	RD										
Reset (7)		1	XXX	F0										
Auto-select (8)	Manufacturer ID	4	555	AA	2AA	55	[BA]555	90	[BA]X00	0001				
	Device ID (9)	6	555	AA	2AA	55	[BA]555	90	[BA]X01	227E	BA+X0E	Data	BA+X0F	2200
	Indicator Bits (10)	4	555	AA	2AA	55	[BA]555	90	[BA]X03	Data				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (11)		6	555	AA	2AA	55	PA	25	PA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (12)		3	555	AA	2AA	55	555	F0						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase/Program Suspend (13)		1	BA	B0										
Erase/Program Resume (14)		1	BA	30										
Set Configuration Register (18)		4	555	AA	2AA	55	555	D0	X00	CR				
Read Configuration Register		4	555	AA	2AA	55	555	C6	X00	CR				
CFI Query (15)		1	[BA]555	98										
Unlock Bypass Mode	Entry	3	555	AA	2AA	55	555	20						
	Program (16)	2	XXX	A0	PA	PD								
	CFI (16)	1	XXX	98										
	Reset	2	XXX	90	XXX	00								
SecSi Sector	Entry	3	555	AA	2AA	55	555	88						
	Program (17)	4	555	AA	2AA	55	555	A0	PA	PD				
	Read (17)	1	00	Data										
	Exit (17)	4	555	AA	2AA	55	555	90	XXX	00				

Legend:

X = Don't care.

RA = Read Address.

RD = Read Data.

PA = Program Address. Addresses latch on the rising edge of the AVD# pulse or active edge of CLK, whichever occurs first.

PD = Program Data. Data latches on the rising edge of WE# or CE# pulse, whichever occurs first.

SA = Sector Address. WS256N = A23–A14; WS128N = A22–A14; WS064N = A21–A14.

BA = Bank Address. WS256N = A23–A20; WS128N = A22–A20; WS064N = A21–A18.

CR = Configuration Register data bits D15–D0.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells indicate read cycles.*
4. *Address and data bits not specified in table, legend, or notes are don't cares (each hex digit implies 4 bits of data).*
5. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
6. *No unlock or command cycles required when bank is reading array data.*
7. *Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information) or performing sector lock/unlock.*
8. *The system must provide the bank address. See Autoselect Command Sequence section for more information.*
9. *Data in cycle 5 is 2230 (WS256N), 2232 (WS064N), or 2231 (WS128N).*
10. *See Table 27 for indicator bit values.*
11. *Total number of cycles in the command sequence is determined by the number of words written to the write buffer. The number of cycles in the command sequence is 37 for full page programming (32 words). Less than 32 word programming is not recommended.*
12. *Command sequence resets device for next command after write-to-buffer operation.*
13. *System may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
14. *Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
15. *Command is valid when device is ready to read array data or when device is in autoselect mode. Address will equal 55h on all future devices, but 555h for WS256N/128N/064N.*
16. *Requires Entry command sequence prior to execution. Unlock Bypass Reset command is required to return to reading array data.*
17. *Requires Entry command sequence prior to execution. SecSi Sector Exit Reset command is required to exit this mode; device may otherwise be placed in an unknown state.*
18. *Requires reset command to configure the Configuration Register.*

Table 30. Sector Protection Commands

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–4)														
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register Bits	Command Set Entry (5)	3	555	AA	2AA	55	555	40								
	Program (6)	2	XX	A0	77	data										
	Read (6)	1	77	data												
	Command Set Exit (7)	2	XX	90	XX	00										
Password Protection	Command Set Entry (5)	3	555	AA	2AA	55	555	60								
	Program [0-3] (8)	2	XX	A0	00	PWD[0-3]										
	Read (9)	4	0...00	PWD0	0...01	PWD1	0...02	PWD2	0...03	PWD3						
	Unlock	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
	Command Set Exit (7)	2	XX	90	XX	00										
Non-Volatile Sector Protection (PPB)	Command Set Entry (5)	3	555	AA	2AA	55	[BA]555	C0								
	PPB Program (10)	2	XX	A0	SA	00										
	All PPB Erase (10, 11)	2	XX	80	00	30										
	PPB Status Read	1	SA	RD(0)												
	Command Set Exit (7)	2	XX	90	XX	00										
Global Volatile Sector Protection Freeze (PPB Lock)	Command Set Entry (5)	3	555	AA	2AA	55	[BA]555	50								
	PPB Lock Bit Set	2	XX	A0	XX	00										
	PPB Lock Bit Status Read	1	BA	RD(0)												
	Command Set Exit (7)	2	XX	90	XX	00										
Volatile Sector Protection (DYB)	Command Set Entry (5)	3	555	AA	2AA	55	[BA]555	E0								
	DYB Set	2	XX	A0	SA	00										
	DYB Clear	2	XX	A0	SA	01										
	DYB Status Read	1	SA	RD(0)												
	Command Set Exit (7)	2	XX	90	XX	00										

Legend:

X = Don't care.

RA = Address of the memory location to be read.

PD(0) = SecSi Sector Lock Bit. PD(0), or bit[0].

PD(1) = Persistent Protection Mode Lock Bit. PD(1), or bit[1], must be set to '0' for protection while PD(2), bit[2] must be left as '1'.

PD(2) = Password Protection Mode Lock Bit. PD(2), or bit[2], must be set to '0' for protection while PD(1), bit[1] must be left as '1'.

PD(3) = Protection Mode OTP Bit. PD(3) or bit[3].

SA = Sector Address. WS256N = A23–A14; WS128N = A22–A14; WS064N = A21–A14.

BA = Bank Address. WS256N = A23–A20; WS128N = A22–A20; WS064N = A21–A18.

PWD3–PWD0 = Password Data. PD3–PD0 present four 16 bit combinations that represent the 64-bit Password

PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.

PWD = Password Data.

RD(0), RD(1), RD(2) = DQ0, DQ1, or DQ2 protection indicator bit. If protected, DQ0, DQ1, or DQ2 = 0. If unprotected, DQ0, DQ1, DQ2 = 1.

Notes:

1. *All values are in hexadecimal.*
2. *Shaded cells indicate read cycles.*
3. *Address and data bits not specified in table, legend, or notes are don't cares (each hex digit implies 4 bits of data).*
4. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
5. *Entry commands are required to enter a specific mode to enable instructions only available within that mode.*
6. *If both the Persistent Protection Mode Locking Bit and the Password Protection Mode Locking Bit are set at the same time, the command operation will abort and return the device to the default Persistent Sector Protection Mode during 2nd bus cycle. Note that on all future devices, addresses will equal 00h, but are currently 77h for WS256N, WS128N, and WS064N. See Table 14 for explanation of lock bits.*
7. *Exit command must be issued to reset the device into read mode; device may otherwise be placed in an unknown state.*
8. *Entire two bus-cycle sequence must be entered for each portion of the password.*
9. *Full address range is required for reading password.*
10. *See Figure 5 for details.*
11. *"All PPB Erase" command will pre-program all PPBs before erasure to prevent over-erasure.*

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ1, DQ2, DQ3, DQ5, DQ6, and DQ7. Table 32 and the following subsections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence. **Note that the Data# Polling is valid only for the last word being programmed in the write-buffer-page during Write Buffer Programming. Reading Data# Polling status on any word other than the last word to be programmed in the write-buffer-page will return false status information.**

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately t_{PSP}, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately t_{ASP}, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6-DQ0 may be still invalid. Valid data on DQ7-D00 will appear on successive read cycles.

Table 32 shows the outputs for Data# Polling on DQ7. Figure 6 shows the Data# Polling algorithm. Figure 24 in "AC Characteristics—Asynchronous" shows the Data# Polling timing diagram.

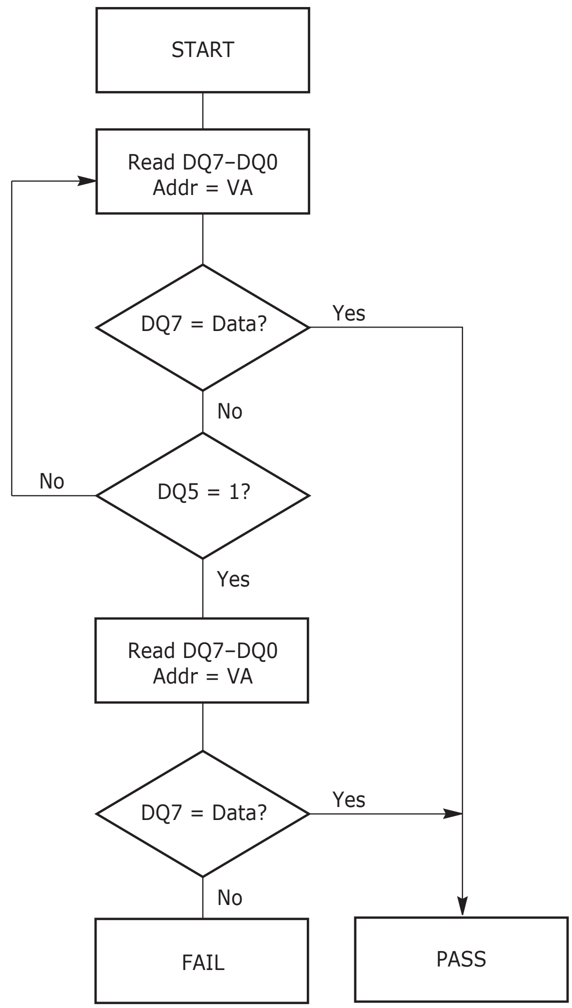


Figure 6. Data# Polling Algorithm

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately t_{ASP} (all sectors protected toggle time), then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

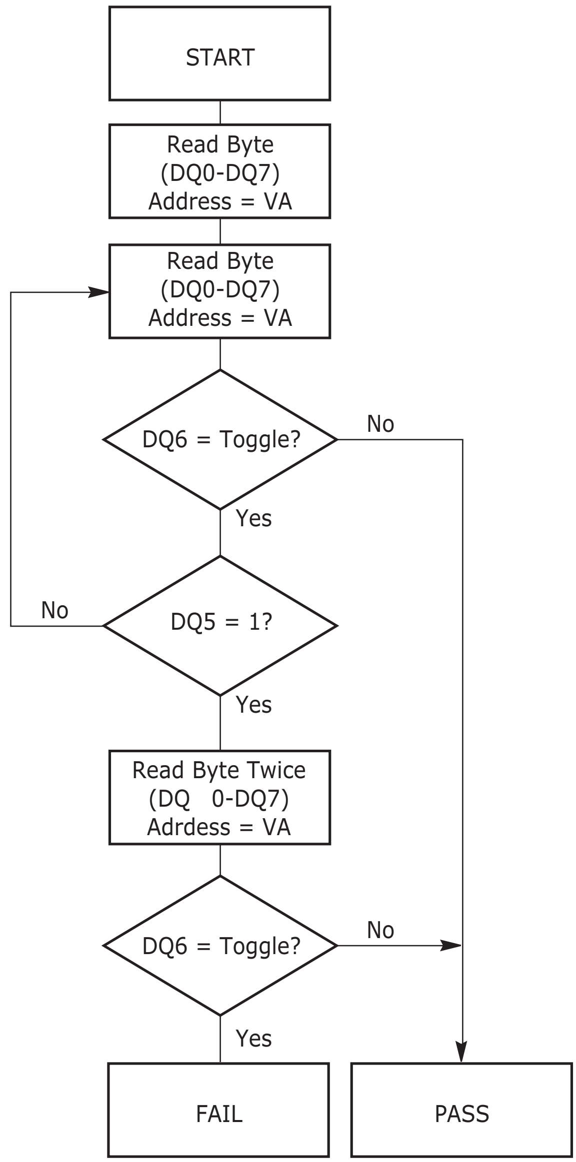
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately t_{PSP} after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: Figure 7, DQ6: Toggle Bit I, Figure 25 (toggle bit timing diagram), and Table 31.

Toggle Bit I on DQ6 requires either OE# or CE# to be deasserted and reasserted to show the change in state.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 7. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 31 to compare outputs for DQ2 and DQ6.

See the following for additional information: Figure 7; DQ6: Toggle Bit I; and Figure 25.

Table 31. DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. Refer to Figure 7 for more details.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, the system need not monitor DQ3. See Sector Erase Command Sequence for more details.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 32 shows the status of DQ3 relative to the other status bits.

DQ1: Write to Buffer Abort

DQ1 indicates whether a Write to Buffer operation was aborted. Under these conditions DQ1 produces a '1'. The system must issue the Write to Buffer Abort Reset command sequence to return the device to reading array data. See Write Buffer Programming Operation for more details.

Table 32. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1 (Note 4)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A
Program Suspend Mode (Note 3)	Reading within Program Suspended Sector		INVALID *(Not Allowed)*	INVALID *(Not Allowed)*	INVALID *(Not Allowed)*	INVALID *(Not Allowed)*	INVALID *(Not Allowed)*	INVALID *(Not Allowed)*
	Reading within Non-Program Suspended Sector		Data	Data	Data	Data	Data	Data
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	N/A
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	Data
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	N/A
Write to Buffer (Note 5)	BUSY State		DQ7#	Toggle	0	N/A	N/A	0
	Exceeded Timing Limits		DQ7#	Toggle	1	N/A	N/A	0
	ABORT State		DQ7#	Toggle	0	N/A	N/A	1

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *Data are invalid for addresses in a Program Suspended sector.*
4. *DQ1 indicates the Write to Buffer ABORT status during Write Buffer Programming operations.*
5. *The data-bar polling algorithm should be used for Write Buffer Programming operations. Note that DQ7# during Write Buffer Programming indicates the data-bar for DQ7 data* ***for the LAST LOADED WRITE-BUFFER ADDRESS location****.*

Absolute Maximum Ratings

Storage Temperature
Plastic Packages . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . –65°C to +125°C

Voltage with Respect to Ground:
All Inputs and I/Os except
as noted below (Note 1) . . . . –0.5 V to V_{IO} + 0.5 V

V_{CC} (Note 1). . . . . –0.5 V to +2.5 V

V_{IO} . . . . –0.5 V to +2.5 V

ACC (Note 2) . . . . –0.5 V to +9.5 V

Output Short Circuit Current (Note 3) . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 8. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 9.*
2. *Minimum DC input voltage on pin ACC is -0.5V. During voltage transitions, ACC may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 8. Maximum DC voltage on pin ACC is +9.5 V, which may overshoot to 10.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

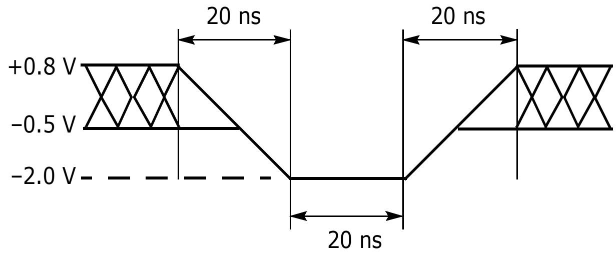


Figure 8. Maximum Negative Overshoot Waveform

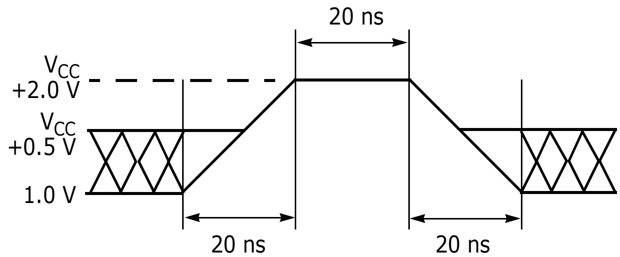


Figure 9. Maximum Positive Overshoot Waveform

Operating Ranges

Wireless (W) Devices

Ambient Temperature (T_A) . . . . –25°C to +85°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . –40°C to +85°C

Supply Voltages

V_{CC} Supply Voltages . . . . +1.70 V to +1.95 V

V_{IO} Supply Voltages: . . . . +1.70 V to +1.95 V
(Contact local sales office for V_{IO} = 1.35 to +1.70 V.)

Notes: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

DC Characteristics

CMOS Compatible

Parameter	Description (Notes)	Test Conditions (Notes l, 2, 9)		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}max$				±1	µA
I_{LO}	Output Leakage Current (3)	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}max$				±1	µA
I_{CCB}	V_{CC} Active burst Read Current	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 8	54 MHz		27	54	mA
			66 MHz		28	60	mA
			80 MHz		30	66	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 16	54 MHz		28	48	mA
			66 MHz		30	54	mA
			80 MHz		32	60	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 32	54 MHz		29	42	mA
			66 MHz		32	48	mA
			80 MHz		34	54	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = Continuous	54 MHz		32	36	mA
			66 MHz		35	42	mA
			80 MHz		38	48	mA
I_{IO1}	V_{IO} Non-active Output	OE# = V_{IH}			20	30	µA
I_{CC1}	V_{CC} Active Asynchronous Read Current (4)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}	10 MHz		27	36	mA
			5 MHz		13	18	mA
			1 MHz		3	4	mA
I_{CC2}	V_{CC} Active Write Current (5)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}	V_{ACC}		1	5	µA
			V_{CC}		19	52.5	mA
I_{CC3}	V_{CC} Standby Current (6, 7)	CE# = RESET# = V_{CC} ± 0.2 V	V_{ACC}		1	5	µA
			V_{CC}		20	40	µA
I_{CC4}	V_{CC} Reset Current (7)	RESET# = V_{IL}, CLK = V_{IL}			70	150	µA
I_{CC5}	V_{CC} Active Current (Read While Write) (7)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}			50	60	mA
I_{CC6}	V_{CC} Sleep Current (7)	CE# = V_{IL}, OE# = V_{IH}			2	40	µA
I_{ACC}	Accelerated Program Current (8)	CE# = V_{IL}, OE# = V_{IH}, V_{ACC} = 9.5 V	V_{ACC}		6	20	mA
			V_{CC}		14	20	mA
V_{IL}	Input Low Voltage	V_{IO} = 1.8 V		–0.5		0.4	V
V_{IH}	Input High Voltage	V_{IO} = 1.8 V		V_{IO} – 0.4		V_{IO} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$		V_{IO} – 0.1			V
V_{HH}	Voltage for Accelerated Program			8.5		9.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Notes:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}max$.*
2. *$V_{CC} = V_{IO}$.*
3. *CE# must be set high when measuring the RDY pin.*
4. *The I_{CC} current listed is typically less than 3 mA/MHz, with OE# at V_{IH}.*
5. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
6. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 20 ns. Typical sleep mode current is equal to I_{CC3}.*
7. *$V_{IH} = V_{CC}$ ± 0.2 V and V_{IL} > –0.1 V.*
8. *Total current during accelerated programming is the sum of V_{ACC} and V_{CC} currents.*
9. *$V_{ACC} = V_{HH}$ on ACC input.*

Test Conditions

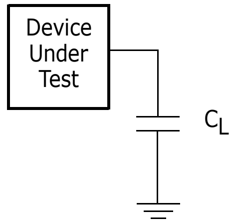
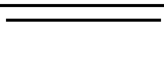
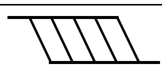
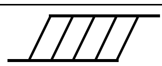
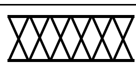
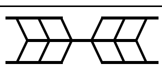


Figure 10. Test Setup

Table 33. Test Specifications

Test Condition	All Speed Options	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	3.0 @ 54, 66 MHz 2.5 @ 80 MHz	ns
Input Pulse Levels	0.0–V_{IO}	V
Input timing measurement reference levels	$V_{IO}/2$	V
Output timing measurement reference levels	$V_{IO}/2$	V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Switching Waveforms

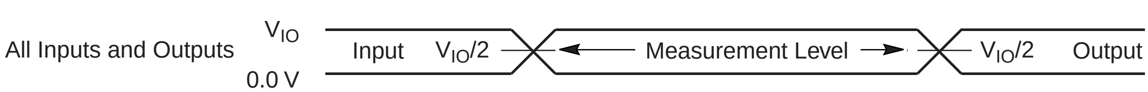


Figure 11. Input Waveforms and Measurement Levels

V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	1	ms

Note:

1. *V_{CC} >= V_{IO} - 100mV and V_{CC} ramp rate is > 1V / 100µs*
2. *V_{CC} ramp rate <1V / 100µs, a Hardware Reset will be required.*

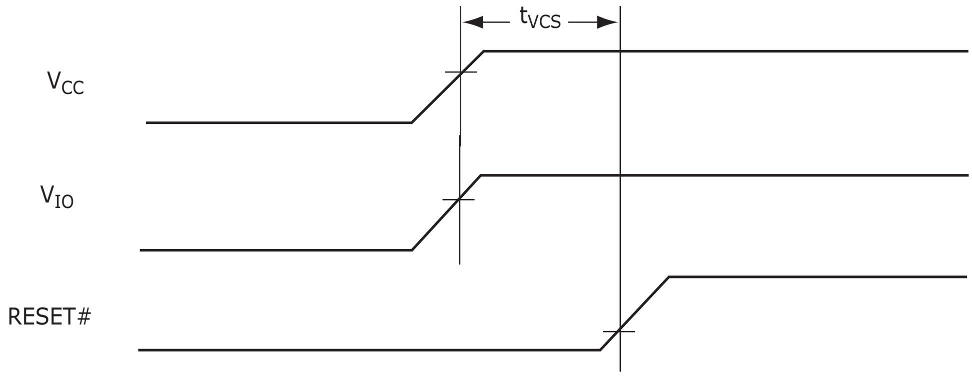


Figure 12. V_{CC} Power-up Diagram

AC Characteristics—Synchronous

CLK Characterization

Parameter	Description		54 MHz	66 MHz	80 MHz	Unit
f_{CLK}	CLK Frequency	Max	54	66	80	MHz
t_{CLK}	CLK Period	Min	18.5	15.1	12.5	ns
t_{CH}	CLK High Time	Min	7.4	6.1	5.0	ns
t_{CL}	CLK Low Time					
t_{CR}	CLK Rise Time	Max	3	3	2.5	ns
t_{CF}	CLK Fall Time					

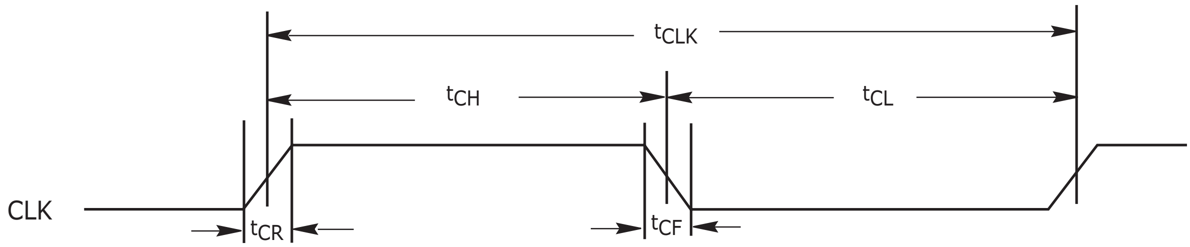


Figure 13. CLK Characterization

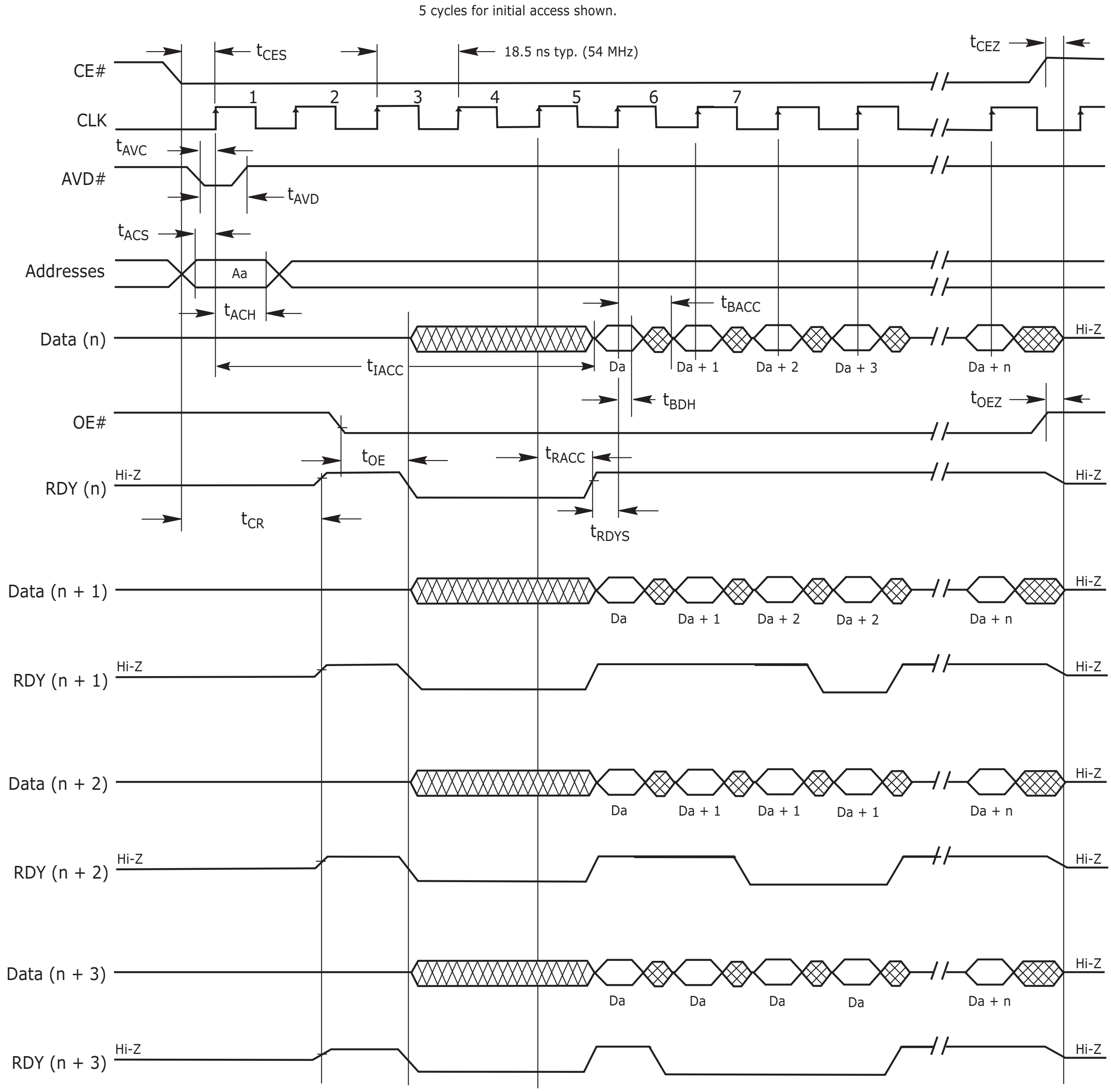
Synchronous/Burst Read

Parameter		Description		54 MHz	66 MHz	80 MHz	Unit
JEDEC	Standard						
	t_{IACC}	Latency	Max	69			ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	13.5	11.2	9	ns
	t_{ACS}	Address Setup Time to CLK (Note 1)	Min	5	4		ns
	t_{ACH}	Address Hold Time from CLK (Note 1)	Min	7	6		ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Min	4	3		ns
	t_{CR}	Chip Enable to RDY Valid	Max	13.5	11.2	9	ns
	t_{OE}	Output Enable to Output Valid	Max	13.5	11.2		ns
	t_{CEZ}	Chip Enable to High Z (Note 2)	Max	10			ns
	t_{OEZ}	Output Enable to High Z (Note 2)	Max	10			ns
	t_{CES}	CE# Setup Time to CLK	Min	4			ns
	t_{RDYS}	RDY Setup Time to CLK	Min	5	4	3.5	ns
	t_{RACC}	Ready Access Time from CLK	Max	13.5	11.2	9	ns
	t_{AAS}	Address Setup Time to AVD# (Note 1)	Min	5	4		ns
	t_{AAH}	Address Hold Time to AVD# (Note 1)	Min	7	6		ns
	t_{CAS}	CE# Setup Time to AVD#	Min	0			ns
	t_{AVC}	AVD# Low to CLK	Min	4			ns
	t_{AVD}	AVD# Pulse	Min	8			ns

Notes:

1. *Addresses are latched on the first of either the active edge of CLK or the rising edge of AVD#.*
2. *Not 100% tested.*

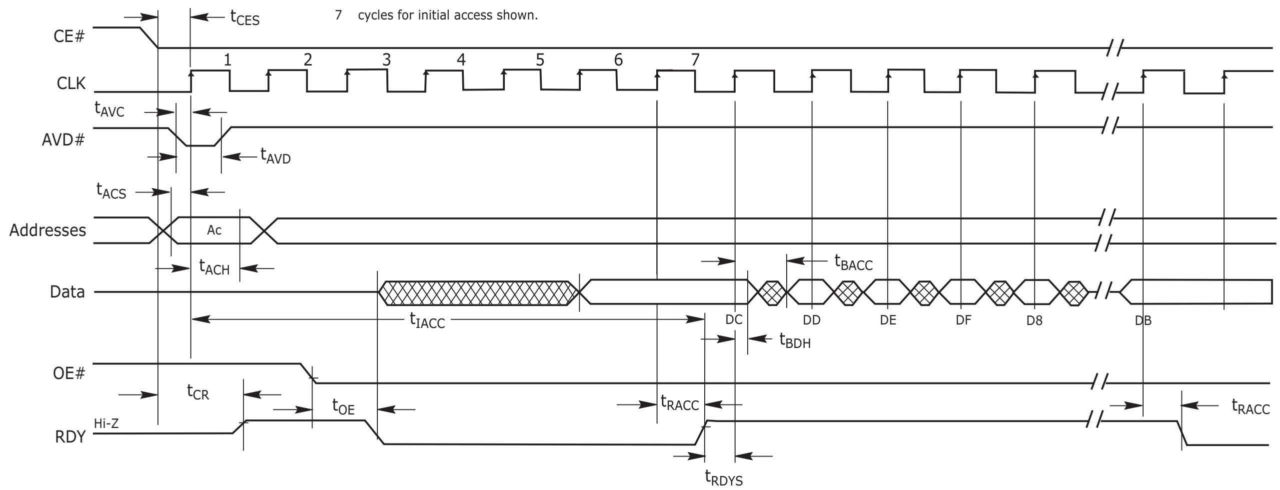
Timing Diagrams



Notes:

1. *Figure shows total number of wait states set to five cycles. The total number of wait states can be programmed from two cycles to seven cycles.*
2. *If any burst address occurs at "address + 1", "address + 2", or "address + 3", additional clock delay cycles are inserted, and are indicated by RDY.*
3. *The device is in synchronous mode.*

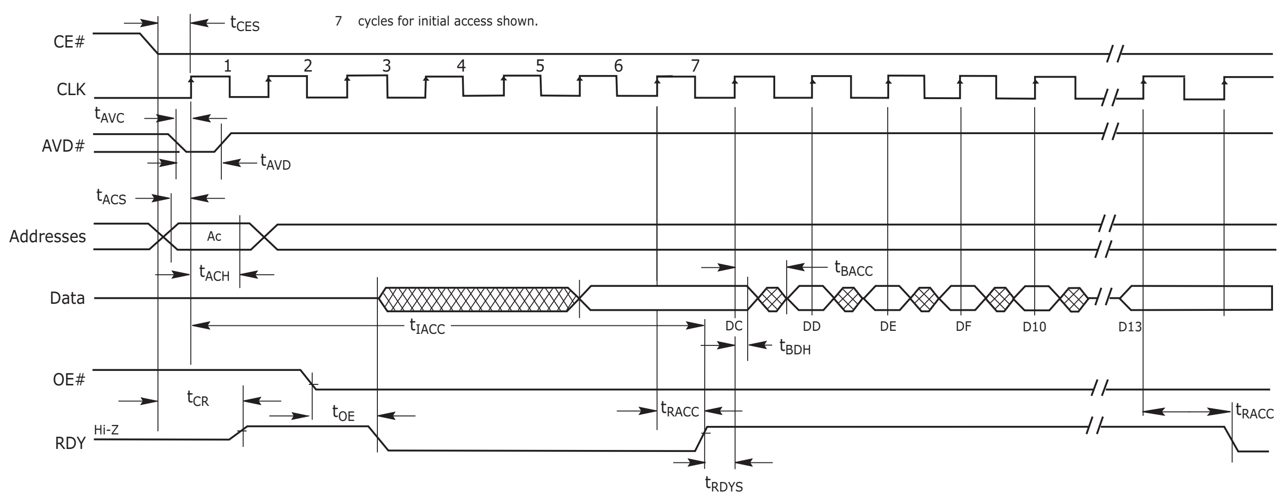
Figure 14. CLK Synchronous Burst Mode Read



Note:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at "address + 1", "address + 2", or "address + 3", additional clock delay cycles are inserted, and are indicated by RDY.*
3. *The device is in synchronous mode with wrap around.*
4. *D8–DF in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Starting address in figure is the 4th address in range (8-F).*

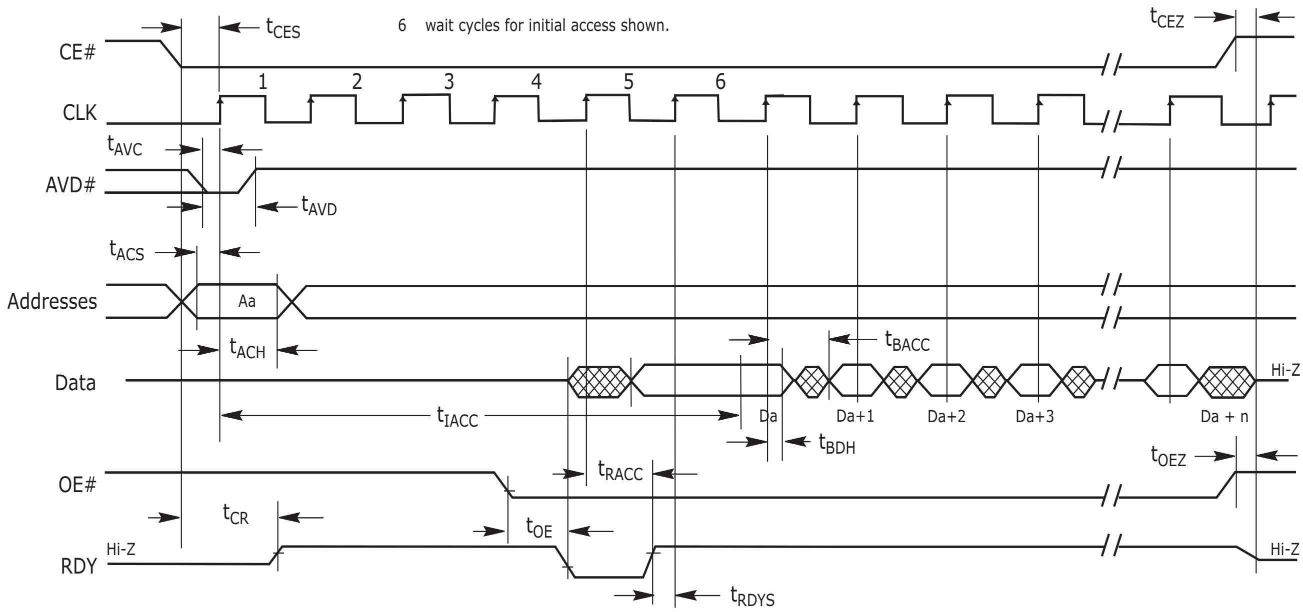
Figure 15. 8-word Linear Burst with Wrap Around



Note:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at "address + 1", "address + 2", or "address + 3", additional clock delay cycles are inserted, and are indicated by RDY.*
3. *The device is in asynchronous mode with out wrap around.*
4. *DC–D13 in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Starting address in figure is the 4th address in range (c-13).*

Figure 16. 8-word Linear Burst without Wrap Around



Note:

1. *Figure assumes 6 wait states for initial access and synchronous read.*
2. *The Set Configuration Register command sequence has been written with CR8=0; device will output RDY one cycle before valid data.*

Figure 17. Linear Burst with RDY Set One Cycle Before Data

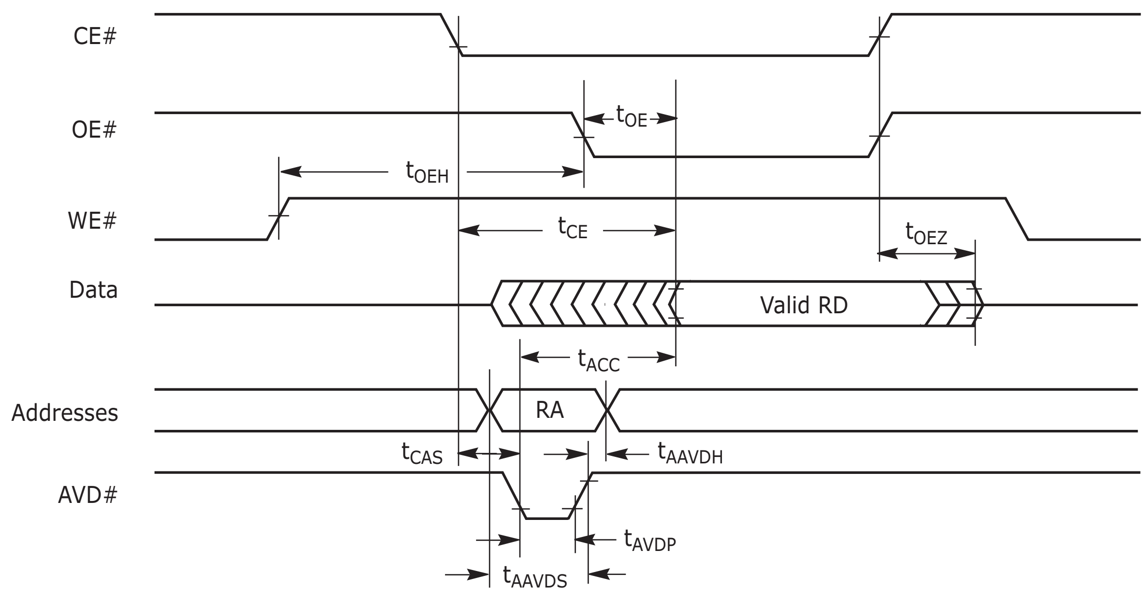
AC Characteristics—Asynchronous

Asynchronous Mode Read

Parameter								
JEDEC	Standard	Description			54 MHz	66 MHz	80 MHz	Unit
	t_{CE}	Access Time from CE# Low		Max	70			ns
	t_{ACC}	Asynchronous Access Time		Max	70			ns
	t_{AVDP}	AVD# Low Time		Min	8			ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD#		Min	4			ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD#		Min	7	6		ns
	t_{OE}	Output Enable to Output Valid		Max	13.5	11.2		ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0			ns
			Toggle and Data# Polling	Min	10			ns
	t_{OEZ}	Output Enable to High Z (see Note)		Max	10			ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0			ns

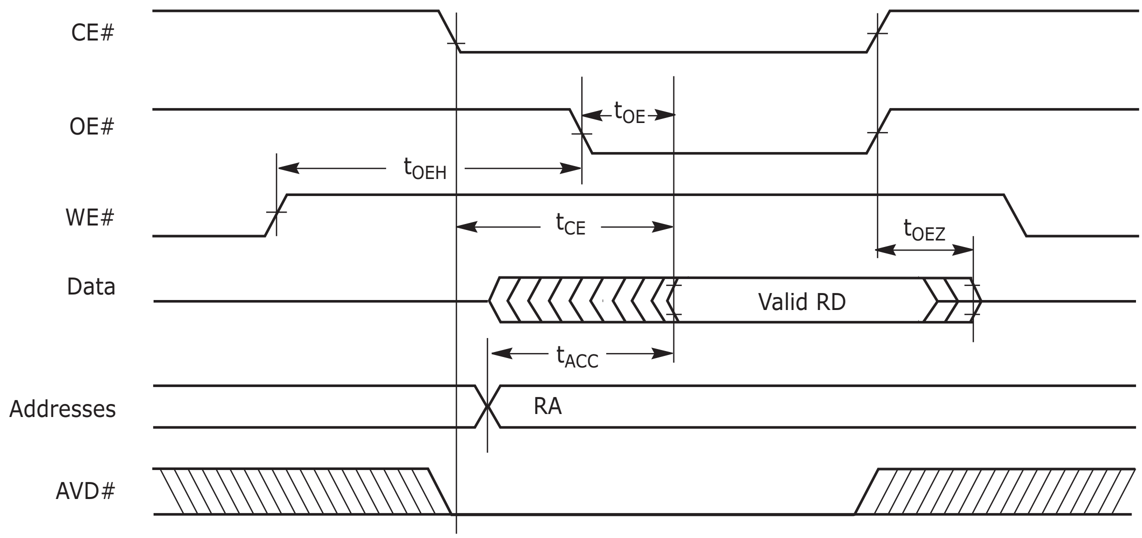
Note: *Not 100% tested.*

Timing Diagrams



Note: *RA = Read Address, RD = Read Data.*

Figure 18. Asynchronous Mode Read with Latched Addresses



Note: *RA = Read Address, RD = Read Data.*

Figure 19. Asynchronous Mode Read

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	**Std.**				
	t_{RP}	RESET# Pulse Width	Min	30	µs
	t_{RH}	Reset High Time Before Read (See Note)	Min	200	ns

Note: *Not 100% tested.*

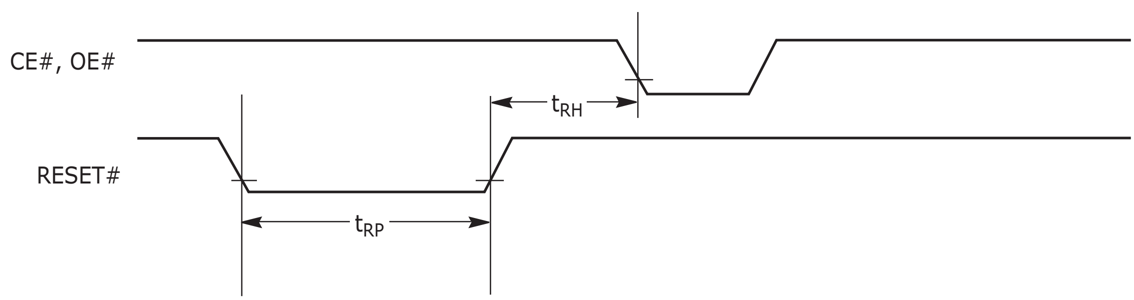


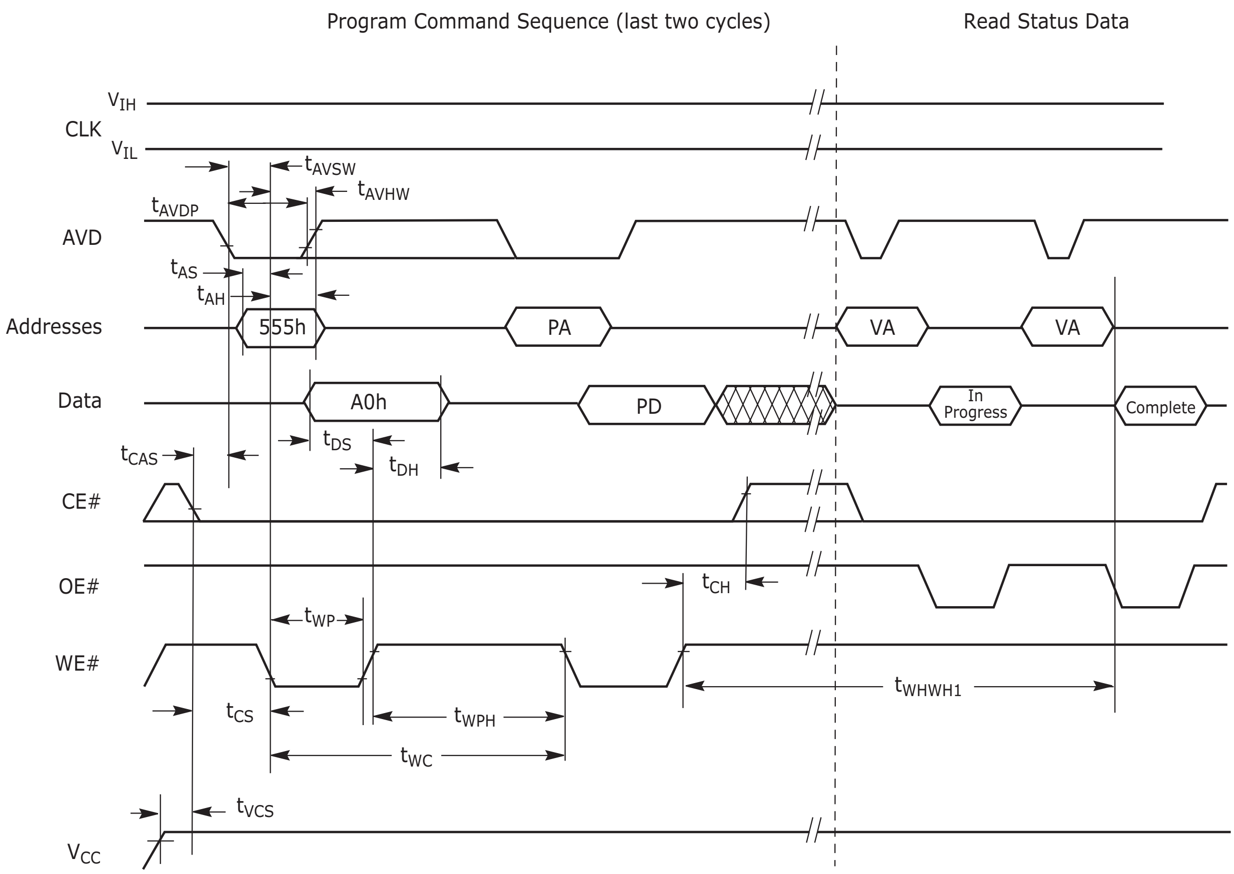
Figure 20. Reset Timings

Erase/Program Timing Operations

Parameter		Description			54 MHz	66 MHz	80 MHz	Unit
JEDEC	Standard							
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70			ns
t_{AVWL}	t_{AS}	Address Setup Time (Notes 2, 3)	Synchronous	Min	5			ns
			Asynchronous		0			ns
t_{WLAX}	t_{AH}	Address Hold Time (Notes 2, 3)	Synchronous	Min	9			ns
			Asynchronous		20			
	t_{AVDP}	AVD# Low Time		Min	8			ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45	20		ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0			ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0			ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	30			ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20			ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0			ns
	t_{VID}	V_{ACC} Rise and Fall Time		Min	500			ns
	t_{VIDS}	V_{ACC} Setup Time (During Accelerated Programming)		Min	1			µs
	t_{VCS}	V_{CC} Setup Time		Min	50			µs
t_{ELWL}	t_{CS}	CE# Setup Time to WE#		Min	5			ns
	t_{AVSW}	AVD# Setup Time to WE#		Min	5			ns
	t_{AVHW}	AVD# Hold Time to WE#		Min	5			ns
	t_{AVSC}	AVD# Setup Time to CLK		Min	5			ns
	t_{AVHC}	AVD# Hold Time to CLK		Min	5			ns
	t_{CSW}	Clock Setup Time to WE#		Min	5			ns
	t_{WEP}	Noise Pulse Margin on WE#		Max	3			ns
	t_{SEA}	Sector Erase Accept Time-out		Max	50			µs
	t_{ESL}	Erase Suspend Latency		Max	20			µs
	t_{PSL}	Program Suspend Latency		Max	20			µs
	t_{ASP}	Toggle Time During Sector Protection		Typ	100			µs
	t_{PSP}	Toggle Time During Programming Within a Protected Sector		Typ	1			µs

Notes:

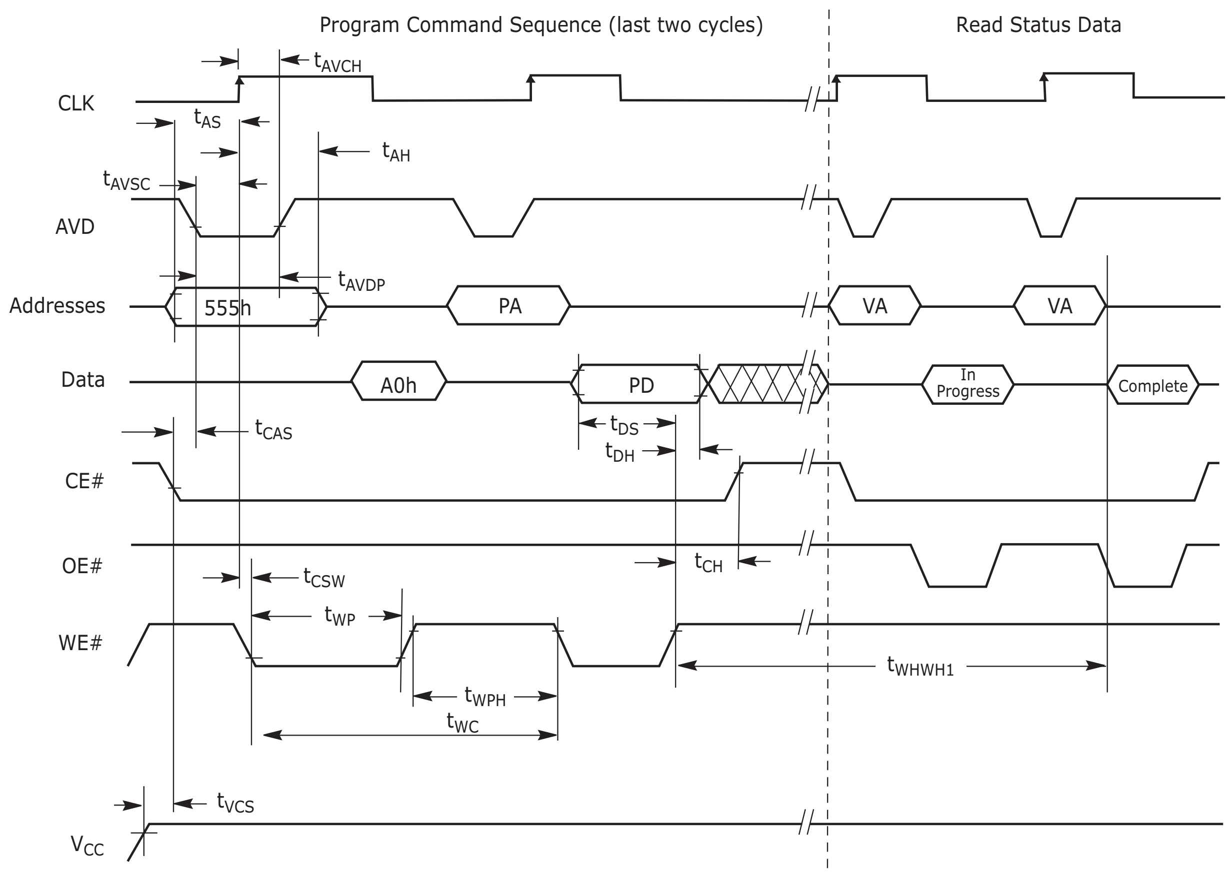
1. *Not 100% tested.*
2. *Asynchronous read mode allows Asynchronous program operation only. Synchronous read mode allows both Asynchronous and Synchronous program operation.*
3. *In asynchronous program operation timing, addresses are latched on the falling edge of WE#. In synchronous program operation timing, addresses are latched on the rising edge of CLK.*
4. *See the "Erase and Programming Performance" section for more information.*
5. *Does not include the preprogramming time.*



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A23–A14 for the WS256N (A22–A14 for the WS128N, A21–A14 for the WS064N) are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Configuration Register.*

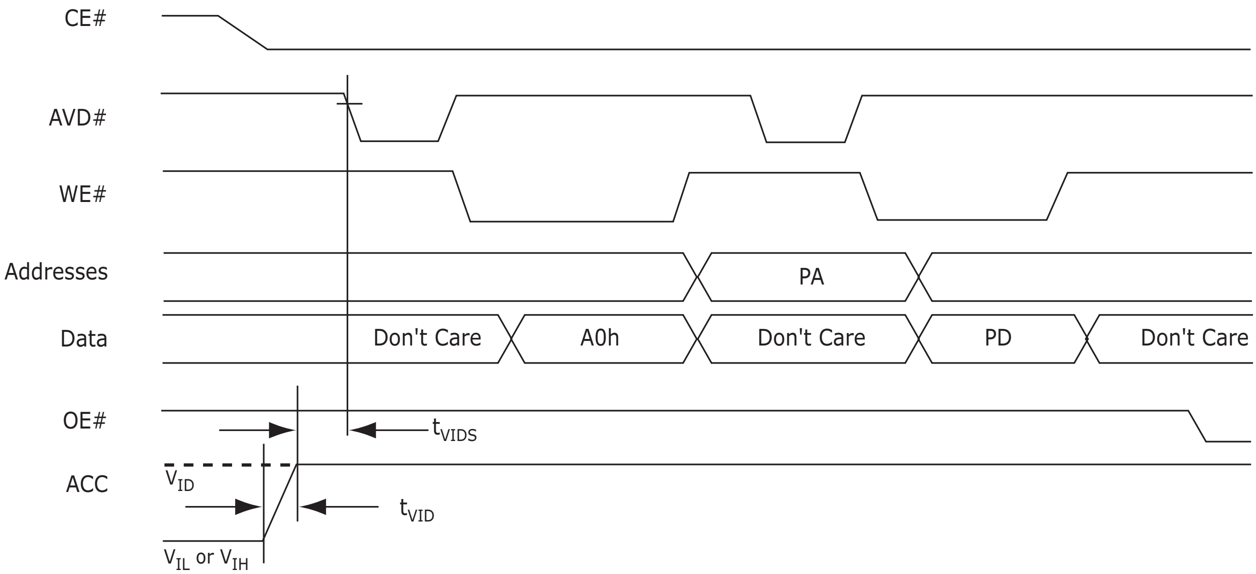
Figure 21. Asynchronous Program Operation Timings: WE# Latched Addresses



Notes:

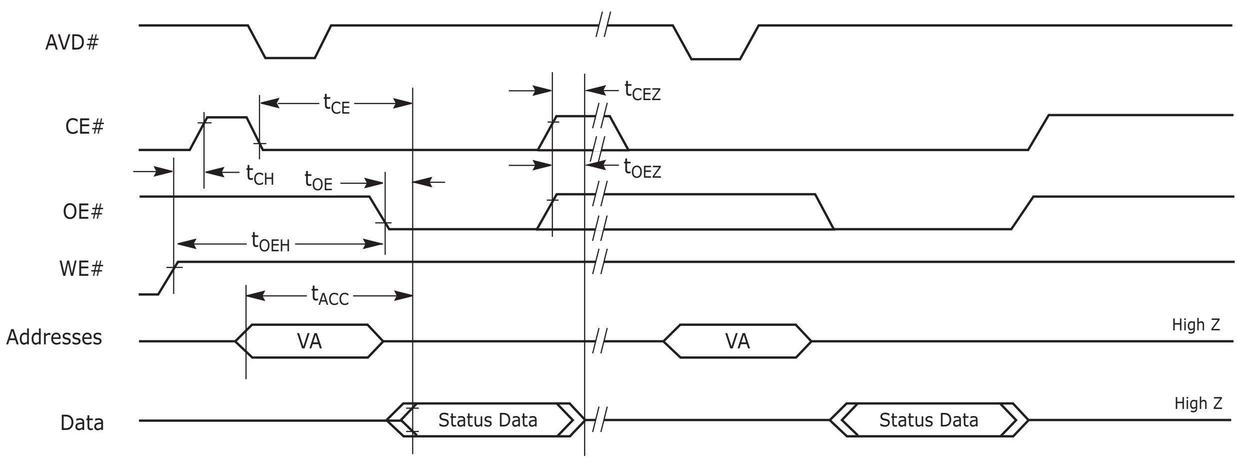
1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A23–A14 for the WS256N (A22–A14 for the WS128N, A21–A14 for the WS064N) are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
5. *Either CE# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is dependent of the Set Device Read Mode bit in the Configuration Register. The Configuration Register must be set to the Synchronous Read Mode.*

Figure 22. Synchronous Program Operation Timings: CLK Latched Addresses



Note: *Use setup and hold times from conventional program operation.*

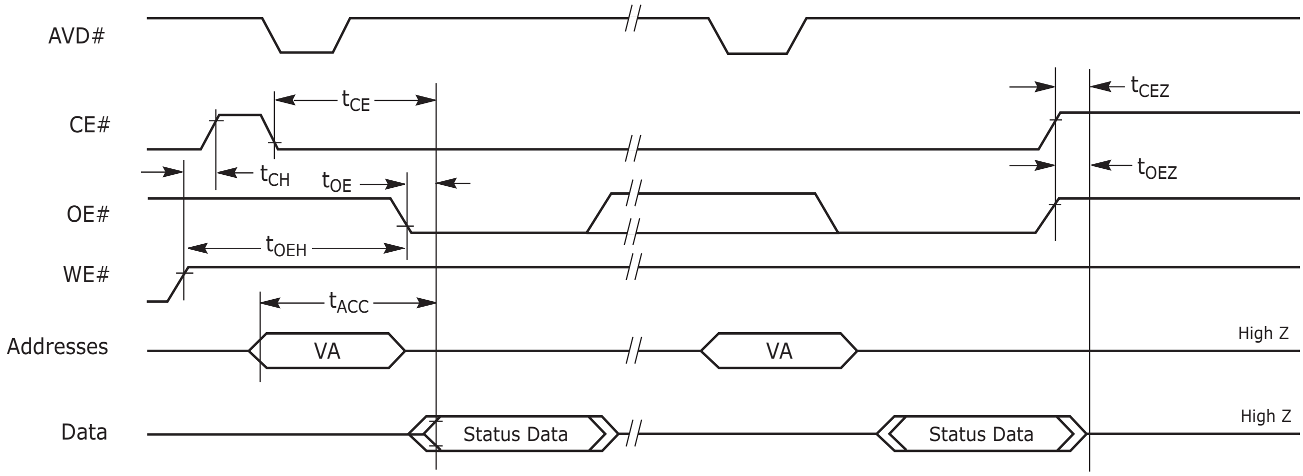
Figure 23. Accelerated Unlock Bypass Programming Timing



Notes:

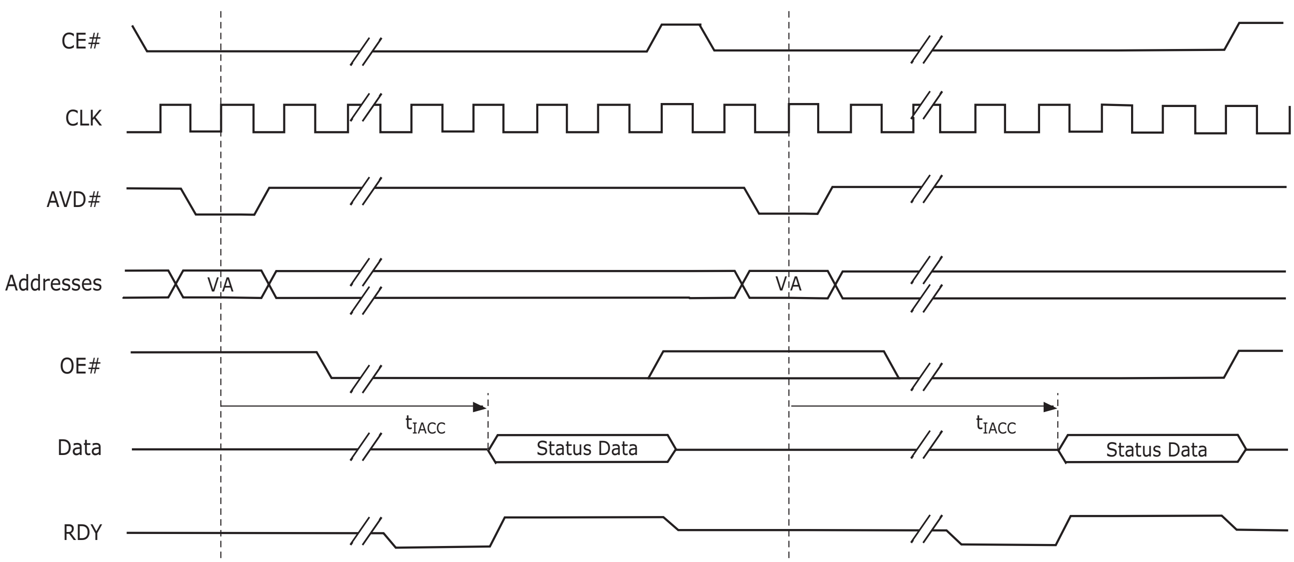
1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*

Figure 24. Data# Polling Timings (During Embedded Algorithm)



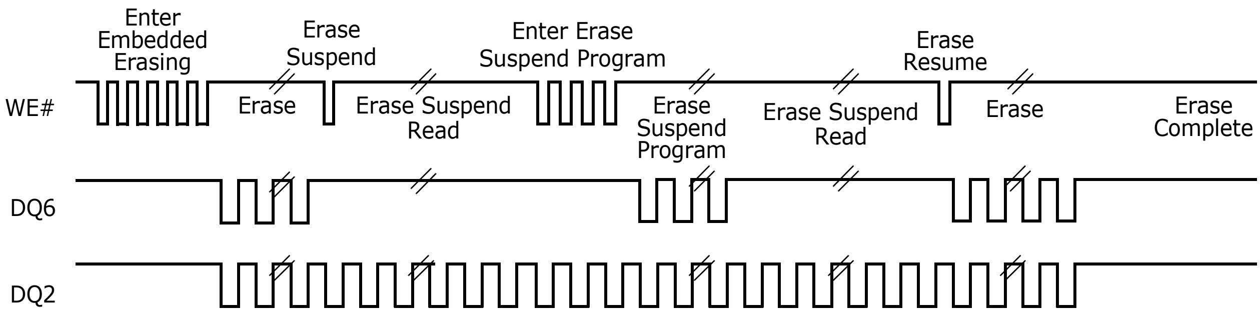
Notes:
1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*

Figure 25. Toggle Bit Timings (During Embedded Algorithm)



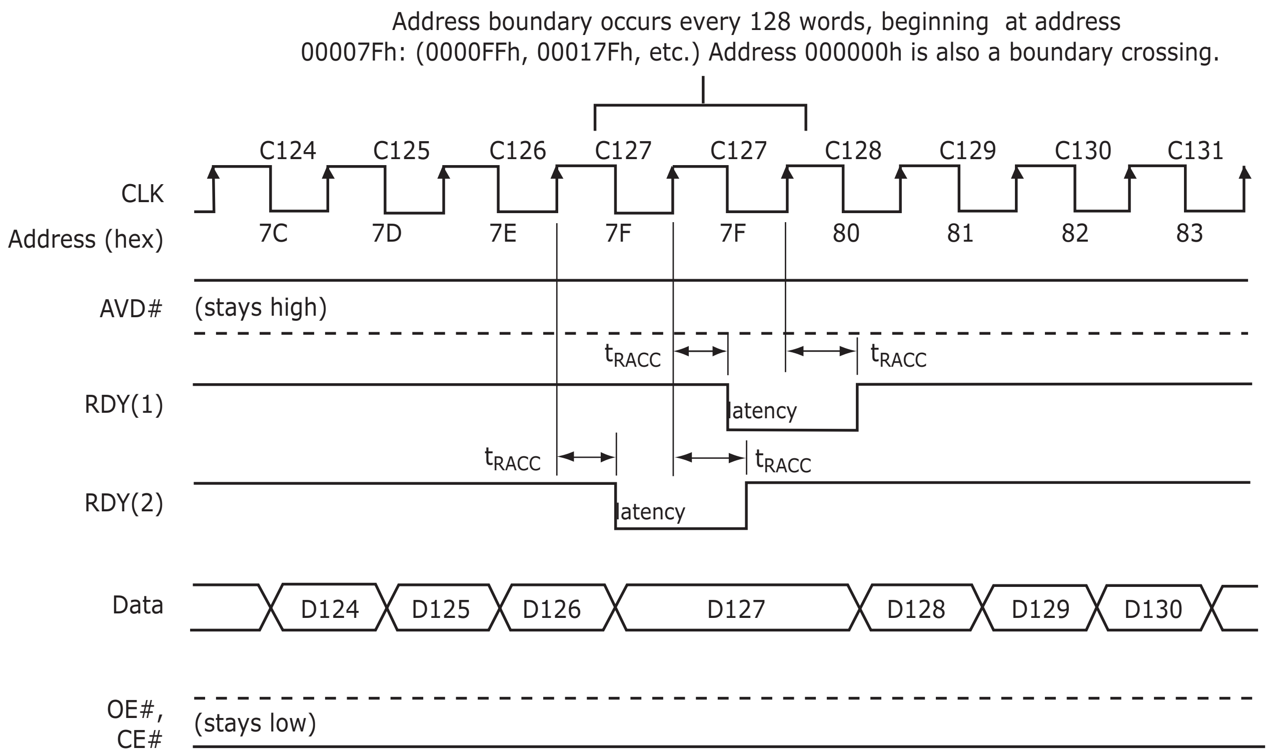
Notes:
1. *The timings are similar to synchronous read timings.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*
3. *RDY is active with data (D8 = 0 in the Configuration Register). When D8 = 1 in the Configuration Register, RDY is active one clock cycle before data.*

Figure 26. Synchronous Data Polling Timings/ Toggle Bit Timings



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

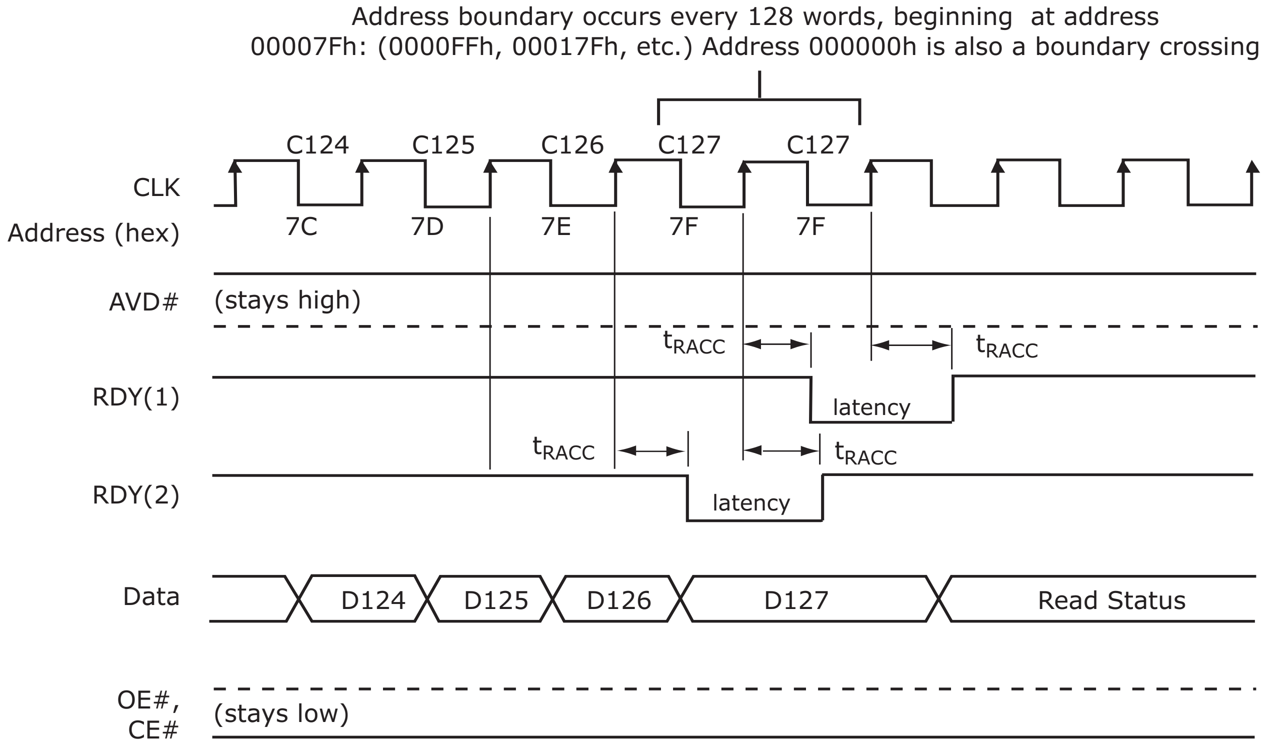
Figure 27. DQ2 vs. DQ6



Notes:

1. *RDY active with data (D8 = 0 in the Configuration Register).*
2. *RDY active one clock cycle before data (D8 = 1 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60.*
4. *Figure shows the device not crossing a bank in the process of performing an erase or program.*
5. *RDY will not go low and no additional wait states will be required if the Burst frequency is <=66 MHz and the Boundary Crossing bit (D14) in the Configuration Register is set to 0*

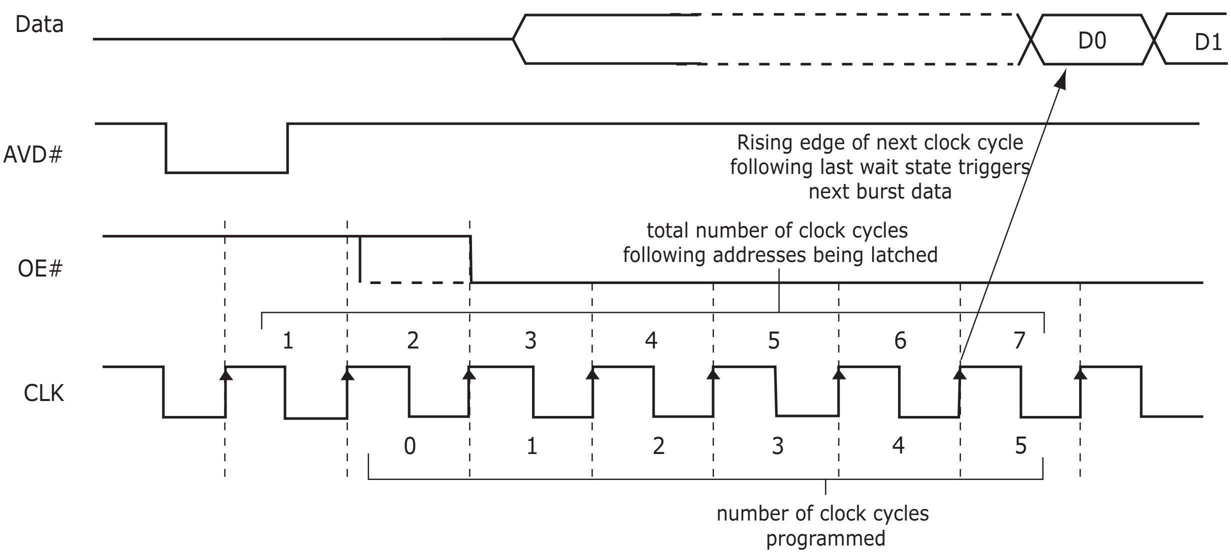
Figure 28. Latency with Boundary Crossing when Frequency > 66 MHz



Notes:

1. *RDY active with data (D8 = 0 in the Configuration Register).*
2. *RDY active one clock cycle before data (D8 = 1 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60.*
4. *Figure shows the device crossing a bank in the process of performing an erase or program.*
5. *RDY will not go low and no additional wait states will be required if the Burst frequency is <=66 MHz and the Boundary Crossing bit (D14) in the Configuration Register is set to 0*

Figure 29. Latency with Boundary Crossing into Program/Erase Bank

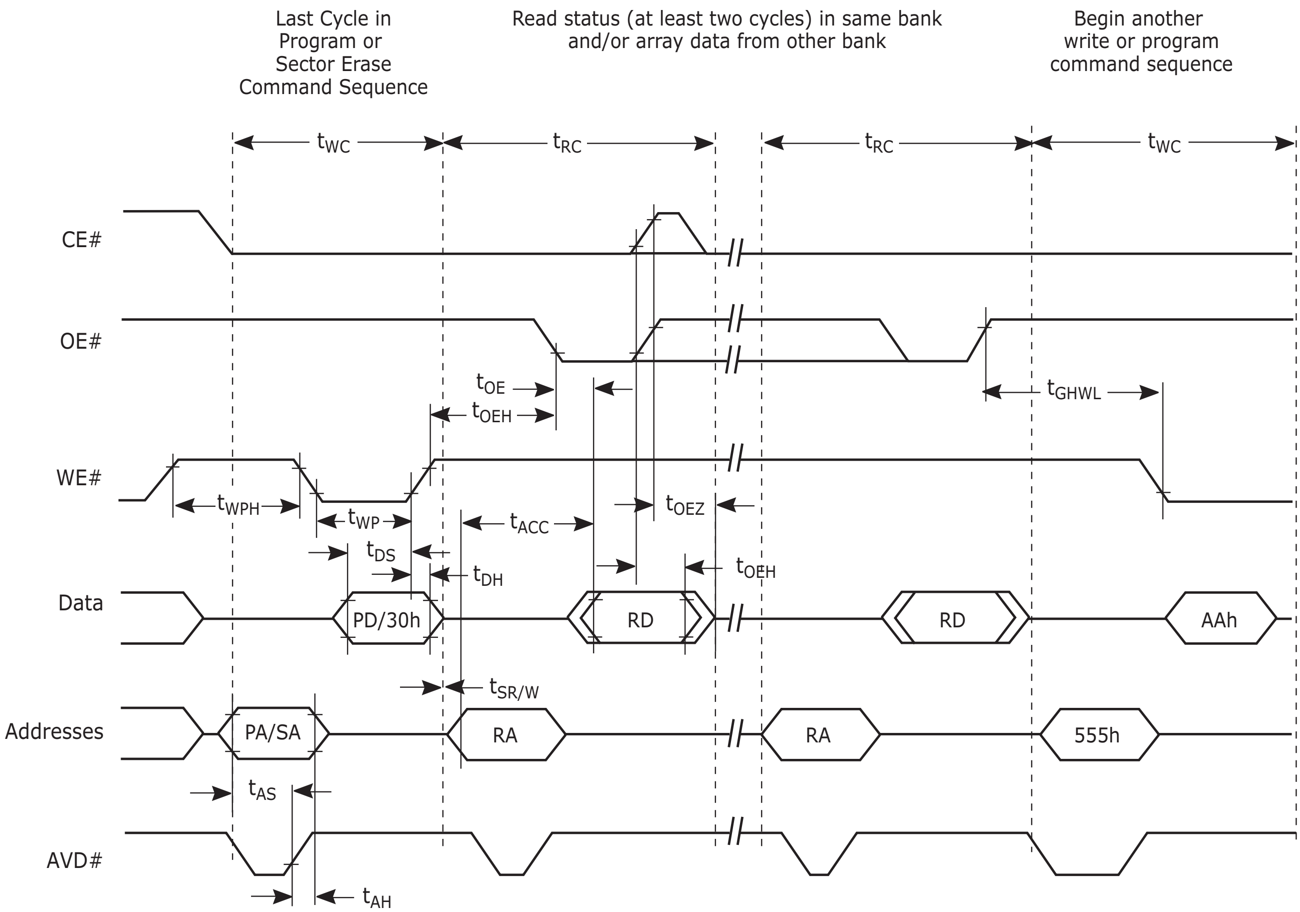


Wait State Configuration Register Setup:

D13, D12, D11 = "111" ⇒ Reserved
D13, D12, D11 = "110" ⇒ Reserved
D13, D12, D11 = "101" ⇒ 5 programmed, 7 total
D13, D12, D11 = "100" ⇒ 4 programmed, 6 total
D13, D12, D11 = "011" ⇒ 3 programmed, 5 total
D13, D12, D11 = "010" ⇒ 2 programmed, 4 total
D13, D12, D11 = "001" ⇒ 1 programmed, 3 total
D13, D12, D11 = "000" ⇒ 0 programmed, 2 total

Note: *Figure assumes address D0 is not at an address boundary, and wait state is set to "101".*

Figure 30. Example of Wait States Insertion



Note: *Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.*

Figure 31. Back-to-Back Read/Write Cycle Timings

Erase and Programming Performance

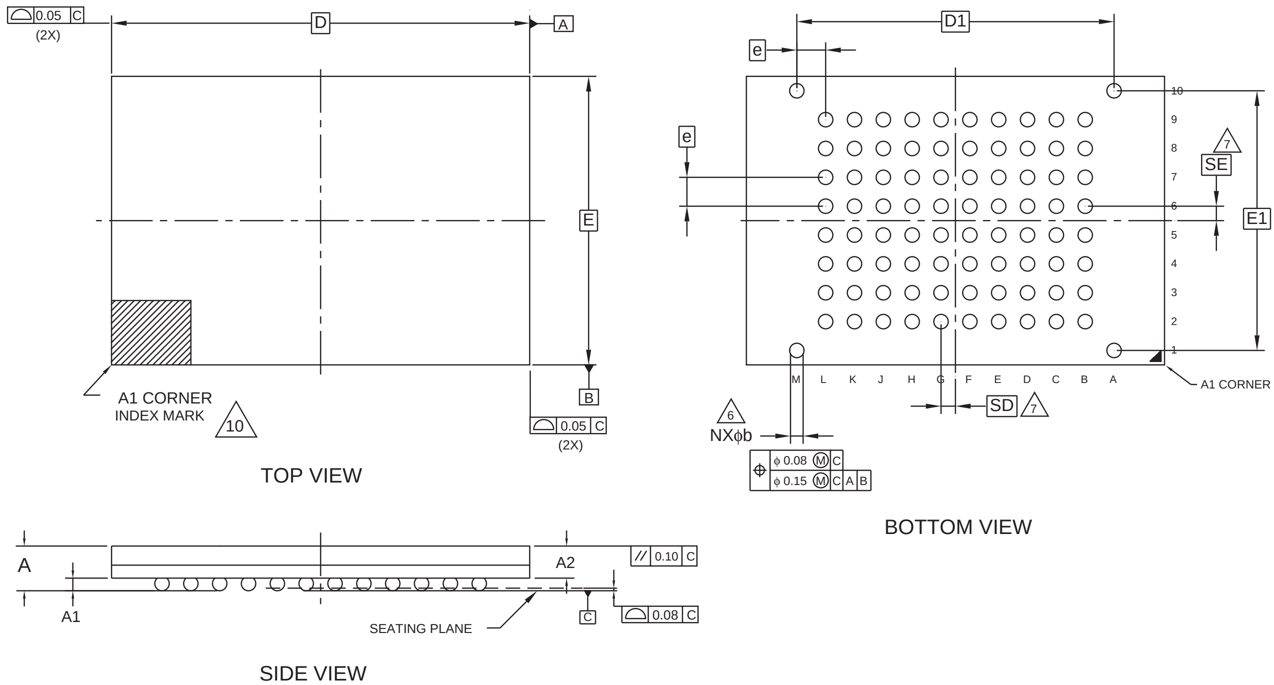
Parameter			Typ (Note l)	Max (Note 2)	Unit	Comments
Sector Erase Time	64 Kword	V_{CC}	0.6	3.5	s	Excludes 00h programming prior to erasure (Note 4)
	16 Kword	V_{CC}	<0.15	2		
Chip Erase Time		V_{CC}	154 (WS256N) 77 (WS128N) 39 (WS064N)	308 (WS256N) 154 (WS128N) 78 (WS064N)	s	
		ACC	131 (WS256N) 66 (WS128N) 33 (WS064N)	262 (WS256N) 132 (WS128N) 66 (WS064N)		
Single Word Programming Time (Note 8)		V_{CC}	40	400	µs	
		ACC	24	240		
Effective Word Programming Time utilizing Program Write Buffer		V_{CC}	9.4	94	µs	
		ACC	6	60		
Total 32-Word Buffer Programming Time		V_{CC}	300	3000	µs	
		ACC	192	1920		
Chip Programming Time (Note 3)		V_{CC}	157.3 (WS256N) 78.6 (WS128N) 39.3 (WS064N)	314.6 (WS256N) 157.3 (WS128N) 78.6 (WS064N)	s	Excludes system level overhead (Note 5)
		ACC	100.7 (WS256N) 50.3 (WS128N) 25.2 (WS064N)	201.3 (WS256N) 100.7 (WS128N) 50.3 (WS064N)		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 10,000 cycles; checkerboard data pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.70 V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed. Based upon single word programming, not page programming.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Command Definition Summary for further information on command definitions.*
6. *Contact the local sales office for minimum cycling endurance values in specific applications and operating conditions.*
7. *Refer to Application Note "Erase Suspend/Resume Timing" for more details.*
8. *Word programming specification is based upon a single word programming operation not utilizing the write buffer.*

Physical Dimensions (256 Mb and 128 Mb)

VBH084—84-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6 mm MCP Compatible Package



PACKAGE	VBH 084			
JEDEC	N/A			
	11.60 mm x 8.00 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.00	OVERALL THICKNESS
A1	0.18	---	---	BALL HEIGHT
A2	0.62	---	0.76	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			BALL FOOTPRINT
E1	7.20 BSC.			BALL FOOTPRINT
MD	12			ROW MATRIX SIZE D DIRECTION
ME	10			ROW MATRIX SIZE E DIRECTION
N	84			TOTAL BALL COUNT
ϕb	0.33	---	0.43	BALL DIAMETER
e	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	(A2-A9, B10-L10, M2-M9, B1-L1)			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3339 \ 16-038.25b

Note: *BSC is an ANSI standard for Basic Space Centering*

Physical Dimensions (64 Mb)

TBD—80-ball Fine-Pitch Ball Grid Array (FBGA) 7x9 mm MCP Compatible Package

TBD

Note: *BSC is an ANSI standard for Basic Space Centering*

Revision Summary

Revision A (February 2, 2004)

Initial release.

Revision A + 1 (March 12, 2004)

Performance Characteristics

Removed the Clock Divider section.

Security Features

Removed Burst Suspend/Resume section. Removed all document-wide references to this feature.

Ordering Information

Package type designations were corrected to show proper lead (Pb) characteristics.

Process Technology was corrected to 110nm.

Word Program Command Sequence

New information added. Section completely re-written.

Revision B (May 24, 2004)

Global

Changed document status to Preliminary. Deleted references to 1.5 V V_{IO} option.

Distinctive Characteristics

MCP-Compatible Packages: Changed ball count and dimensions for 128Mb BGA package to 84-ball, 8 x 11.6 mm.

High Performance: Changed typical word programming time to <6 µs.

General Description

Corrected maximum wireless temperature range maximum to +85°C. Deleted paragraph referring to clock polarity.

Connection Diagrams

Changed diagram for 128 Mb package to 84-ball layout, changed A23 input to RFU. Added note to 64 Mb connection diagram.

Ordering Information

Reformatted layout for easier reference. Changed valid combinations for 128 Mb density to match package change (80-ball to 84-ball; 8 x 10 mm to 8 x 11.6 mm).

Table 1, Device Bus Operations

Corrected symbols for AVD# during the Load Starting Burst Address and Terminate Current Burst Read Cycle and Start New Burst Read Cycle operations to active rising edge.

Write Buffer Programming Operation

Changed "Sector Address" to "starting address" in the first paragraph.

Table 17, System Interface String

Deleted note and references in table.

Read Configuration Register Command

Burst Active Clock Edge Configuration: Deleted reference to active falling edge settings.

Table 26, Configuration Register

Changed 01b setting definition for CR6 to reserved for future use.

Tables 29-30, Command Definitions Tables

Reformatted for easier reference. Added Notes 10 and 11 to Table 30. Corrected definition for SecSi Sector Program command sequence.

DC Characteristics Table

Added Note 9 to Test Conditions column heading. Added Note 7 reference to I_{CC4}, I_{CC5}, and I_{CC6} specifications. Changed maximum specifications for I_{CC3} at V_{CC}, I_{CC4}, and I_{CC6}. Added Notes 7 and 8.

V_{CC} Power-up Table and Figure 12, V_{CC} Power-up Diagram

Deleted t_{VIOS} from table and diagram. Moved beginning of t_{VCS} period from V_{CC} low to V_{CC} high.

Figure 13, CLK Characterization

Deleted CLK Divider waveform from figure.

Synchronous Burst Read Operations table

Deleted t_{RCC} from table. Changed Note 1 to indicate only rising edge of CLK.

Synchronous Burst Mode Read figure.

Deleted figure.

Hardware Reset (RESET#) table

Deleted references to Embedded Algorithms. Deleted alternate definition of t_{RH} (not during Embedded Algorithms).

Erase/Program Operations table

Changed specifications for t_{AH} at 54 and 80 MHz speed options.

Changed specification for t_{WHWH1}. Modified Note 3 to indicate rising edge of CLK only.

Erase and Programming Performance Table

Changed cycles in Note 1 and V_{CC} voltage in Note 2. Added Note 7. Changed typical and maximum values for Effective Word Programming Time utilizing Program Write Buffer (at ACC), Total 32-Word Buffer Programming Time (at ACC), Chip Programming Time (at ACC and V_{CC}).

Physical Dimensions

Deleted 80-ball, 8 x 10 mm package drawing.

Revision C (June 14, 2004)

Global

Changed all 1.65 V V_{CC} and V_{IO} specifications to 1.70 V. Deleted references to 1.8 V V_{IO}.

Distinctive Characteristics

SecSi Sector region: Added "non-erasable region" subbullet.

MCP-compatible packages: Deleted "recommended for all new designs".

Read access times: Changed specifications for synchronous initial latency and asynchronous random access times for 80 MHz speed option.

Program and Erase Performance: Changed heading text. Deleted "less than" symbols in front of specification values. Changed typical sector erase time for 64 Kword sectors.

Power dissipation: Deleted C_L condition. Deleted "less than" symbols in front of specification values. Changed all specifications listed to new values.

Deleted *Hardware Reset input* and *CMOS compatible input* bullets.

ACC input: Added "erase" to bullet text.

General Description

Modified description in third sentence of first paragraph. Changed initial latency specification for 80 MHz speed option.

Modified description of Write Buffer Programming, Program Suspend/Program Resume, Erase Suspend/Erase Resume paragraphs. In 15th paragraph, added "memory array' to first sentence, and changed description of DQ3. In last paragraph, deleted reference to Fowler-Nordheim tunneling.

Product Selector Guide

Changed specifications for 80 MHz speed option.

Block Diagram

Deleted V_{SSIO} input.

Connection Diagrams

Deleted note below diagrams. *Multi-Chip Compatible Packages:* Deleted references to Am29BDS products. *MCP Look-Ahead Connection Diagram:* Added section.

Input/Output Descriptions

Deleted V_{IO} and V_{SSIO}. Corrected CE#f1 name. Deleted voltage range for V_{CC}. Added description for RFU.

Ordering Information

Changed reel size for packing types 2, 3. Corrected model numbers for 64 Mb device. Added Note 3 to all ordering information charts. Deleted BAI and added BFW to package & temperature valid combinations. Modified DYB power-up state description.

Table 1, Device Bus Operations

Deleted note. Changed active edge symbol in AVD# column for all operations. Changed active edge symbol in CLK column for synchronous write operation.

Requirements for Asynchronous (Non-Burst) Read Operation

Deleted last sentence of first paragraph. Deleted reference to addresses in second sentence of second paragraph.

Requirements for Synchronous (Burst) Read Operation

Modified first sentence of second paragraph. Deleted third paragraph. Modified Tables 2–11 and rearranged table sequence. *8-, 16-, and 32-Word Linear Burst with Wrap Around:* Clarified first sentence in first paragraph. Modified first and second sentences in second paragraph. *8-, 16-, and 32-Word Linear Burst without Wrap Around:* Added last sentence to first paragraph. Deleted second paragraph.

Configuration Register

Deleted "active clock edge" from paragraph.

Accelerated Program/Chip Erase Operations

Clarified heading title. Modified first sentence of second paragraph.

Write Buffer Programming Operation

Modified note from first paragraph. Moved partial text from last paragraph to previous paragraph, deleted ramaining text.

Password Sector Protection

Replaced OTP reference in last paragraph with "non-erasable".

Lock Register

Modified first paragraph.

Hardware Data Protection Mode

Modified second, third, and last paragraphs.

Write Pulse "Glitch" Protection

Modified description.

Standby Mode

Modified second paragraph.

RESET#: Hardware Reset Input

Modified second paragraph. Deleted fourth paragraph.

SecSi™ (Secured Silicon) Sector Flash Memory Region

Modified second paragraph.

SecSi Sector Protection Bit

Deleted section.

Common Flash Memory Interface (CFI)

Added table reference to second paragraph. Deleted third paragraph.

Table 16, CFI Query Identification String: Changed data for addresses 1Fh, 21h, and 25h.

Table 17, System Interface String: Changed data for addresses 2Ah.

Table 18, Device Geometry Definition: Changed data and description for addresses 45h.

Table 21, WS128N Sector & Memory Address Map: Corrected address range and sector address bit range for SA66.

Set Configuration Register Command Sequence

Deleted reference to active clock edge.

Programmable Wait State

Modified paragraph.

Set Internal Clock Frequency, Burst Sequence, Burst Active Clock Edge Configuration

Deleted sections.

Table 23, Programmable Wait State Settings

Added 80 MHz column.

RDY Configuration

Deleted last sentence of paragraph.

Table 25, Burst Length Configuration

Changed function and settings descriptions for CR9, CR7, CR6. Added CR5, CR4 to table.

Table 26, Configuration Register

Changed read data for DA15-DQ0 and DQ2 indicator bits (BA) + 03h. Added row for Sector Block Lock/Unlock codes.

Word Program Command Sequence

Modified first sentence of third paragraph. Modified fourth sentence of last paragraph. Moved Figure 2 to this section.

Figure 3, Write Buffer Programming Operation

Deleted WS=31 from second box in figure.

Unlock Bypass Command Sequence

Deleted next to last sentence in first paragraph. Modified first sentence in second paragraph. Deleted third and fourth paragraphs.

Chip Erase Command Sequence

Modified first sentence in first paragraph. Deleted fourth paragraph.

Sector Erase Command Sequence

Modified first sentence in first paragraph. Modified third paragraph: added t_{SEA}, description, deleted sixth and seventh and ninth (last) sentences. Deleted seventh paragraph.

Erase Suspend/Erase Resume Commands

Added t_{SEA} to first paragraph. Added t_{ESL} to second paragraph.

Program Suspend/Program Resume Commands

Added t_{PSL} to first paragraph.

Lock Register Command Set Definitions

Modified third paragraph; combined with fifth paragraph. Deleted fourth paragraph.

Password Protection Command Set Definitions

Clarified fifth and sixth paragraphs.

Non-Volatile Sector Protection Command Set Definitions

Modified third paragraph. Added Figure 5 to section.

Volatile Sector Protection Command Set

Clarified statement after bulleted list.

Table 29, Memory Array Commands

Added Note 18 to table. Deleted sector erase and erase rows from Unlock Bypass section of table. Added note reference to Set Configuration Register command.

Table 30, Sector Protection Commands

Deleted "Non" from Global Non-Volatile Sector Protection Freeze Command heading in table. Modified Note 10.

Write Operation Status

Added t_{PSP} to second paragraph and t_{ASP} to fourth paragraph.

RDY: Ready

Moved subsection to Device Bus Operations section. Modified first sentence, and deleted last sentence in first paragraph. Deleted second paragraph.

DQ6: Toggle Bit I

Added t_{ASP} to third paragraph. Added t_{PAP} to fifth paragraph.

DQ3: Sector Erase Timer

Added t_{SEA} to first paragraph.

Operating Ranges

Changed V_{CC} and V_{IO} supply voltage range specifications.

DC Characteristics

Changed Note 7. Changed specifications for I_{CCB}, I_{CC1}, I_{CC2}, I_{CC3}, I_{CC4}, I_{CC6}. Removed "less than" symbol from I_{CC5} and I_{ACC}.

Synchronous/Burst Read

Changed specifications for t_{IACC}, t_{OE}, t_{CEZ}, t_{OEZ}, t_{CES}, t_{AVC}, t_{AVD}. Deleted t_{CKA}, t_{CKZ}, t_{OES}. Changed Note 2.

Figure 14, CLK Synchronous Burst Mode Read and Figure 15, 8-word Linear Burst with Wrap Around

Modified Addresses waveform. Changed Note 4.

Hardware Reset (RESET#) table

Changed specifications for t_{RP} and t_{RH}.

Asynchronous Mode Read table

Changed specifications for t_{CE}, t_{ACC}, t_{AVDP}, t_{AAVDS}, tOE, t_{OEH}, t_{OEZ}. Added note.

Erase/Program Timing Operations table

Changed specifications for t_{WC}, t_{AS}, t_{AH}, t_{AVDP}, t_{WP}, t_{CS}, t_{ASW}, t_{AVHW}, t_{AVSC}, t_{AVHC}. Added t_{WEP}, t_{SEA}, t_{ESL}, t_{PS}L, t_{ASP}, t_{PSP}. Deleted t_{WHWH1} and t_{WHWH2}.

Figure 22, Synchronous Program Operation Timings: CLK Latched Addresses

Modified AVD waveform.

Figure 23, Accelerated Unlock Bypass Programming Timing

Deleted t_{VIDS} value from OE# waveform.

Figure 29, Latency with Boundary Crossing into Program/Erase Bank

Modified note.

Erase and Programming Performance

Deleted Erase Suspend/Erase Resume Latency, and Program Suspend/Program Resume Latency specifications from table. Changed specifications for all except Chip Programming Time. Removed "less than" symbol for Chip Programming Times. Added Single Word Programming Time specifications. Added Note 8.

Colophon

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