Bi-Directional P-Channel Battery Disconnect Switch

TrenchFET® Power MOSFETs
1.8-V Rated

PRODUCT SUMMARY		
V_{SS} (V)	$r_{(on)}$ (Ω)	I_S (A)
–8	0.140 @ V_{GS} = –4.5 V	±3
	0.190 @ V_{GS} = –2.5 V	±2.6
	0.310 @ V_{GS} = –1.8 V	±2.0

FEATURES

- Low $r_{SS(on)}$ Symmetrical P-Channel MOSFET
- Rated for 1.8- to 8-V Operation
- Symmetrical 8-V Blocking (off) Voltage
- Solution for High-Side Battery Disconnect Switching (BDS)
- Supports Multiple Battery Applications
- Low Profile, Small Footprint TSOP-6 Package

DESCRIPTION

The Si3803DV is a low on-resistance p-channel power MOSFET providing 8-V bi-directional blocking and low-resistance bi-directional conduction. The Si3803DV was realized by integrating two rugged, p-channel, high density Trench process, vertical MOSFETs in a common drain area. This yields exactly the same “reverse blocking” results as externally connecting the drains of a dual MOSFET, but without the wasted separation between two die and the area lost to drain connections that can be avoided by connecting them internally. Additional space is saved by tying the two gates common. This allows the Si3803DV to replace a larger dual MOSFET package with a single smaller footprint, lower profile, TSOP-6 package.

APPLICATION CIRCUITS

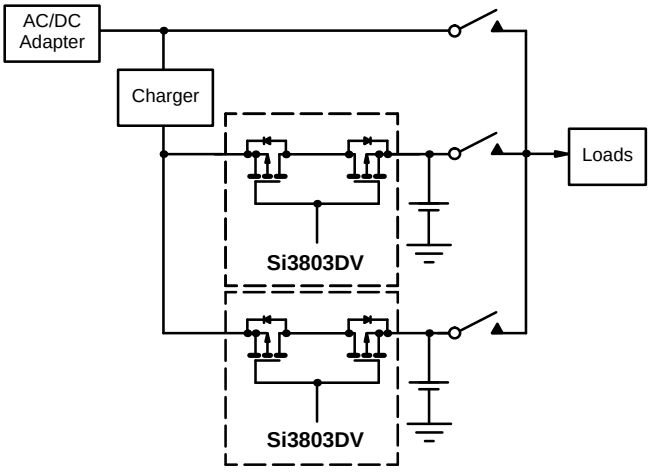


FIGURE 1. Charger Demultiplexing

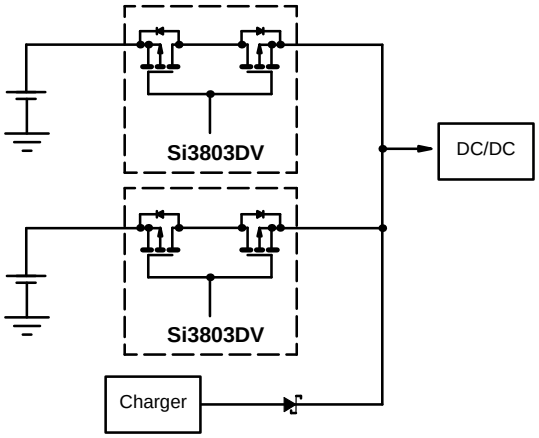


FIGURE 2. Battery Multiplexing (High-Side Switch)

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

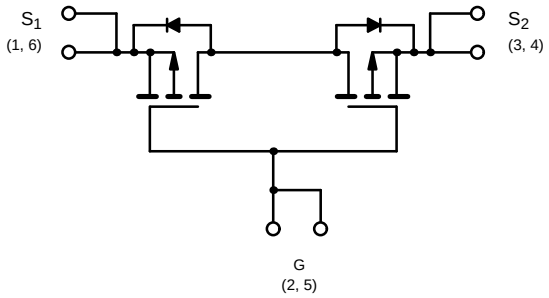


FIGURE 3.

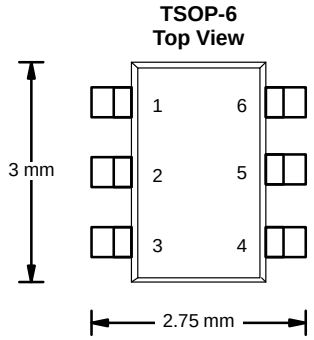


FIGURE 4.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Unit
Source-Source Voltage		V_{SS}	±8	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Current (T_J = 150°C)[a, b]	T_A = 25°C	I_S	±3	A
	T_A = 70°C		±2.5	
Pulsed Drain Current		I_{SM}	±10	
Maximum Power Dissipation[a, b]	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}		62.5	°C/W
	Steady State		106		

Notes
a. Surface Mounted on FR4 Board.
b. t ≤5 sec.

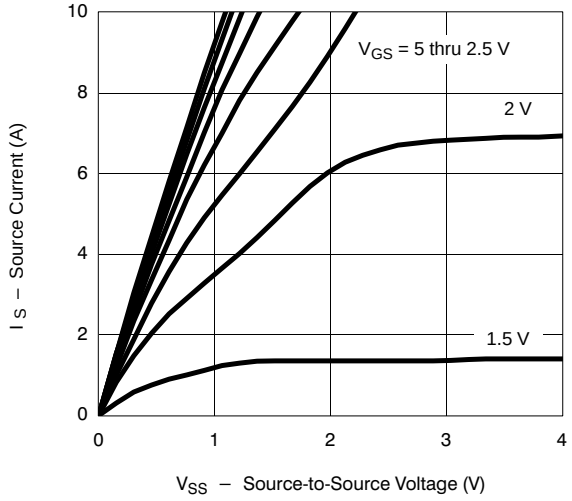
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{SS} = V_{GS}, I_D = 250 μA	–0.45			V
Gate-Body Leakage	I_{GSS}	V_{SS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Source Current	I_{SSS}	V_{SS} = –8 V, V_{GS} = 0 V			–1	μA
		V_{SS} = –8 V, V_{GS} = 0 V, T_J = 70°C			–5	
On-State Source Current[a]	$I_{S(on)}$	V_{SS} = –5 V, V_{GS} = –4.5 V	–10			A
Source-Source On-State Resistance[a]	$r_{(on)}$	V_{GS} = –4.5 V, I_S = –3 A		0.115	0.140	Ω
		V_{GS} = –2.5 V, I_S = –1.0 A		0.160	0.190	
		V_{GS} = –1.8 V, I_S = –1.0 A		0.260	0.310	
Forward Transconductance[a]	g_{fs}	V_{SS} = –10 V, I_S = –3 A		9		S
Dynamic[b]						
Total Gate Charge	Q_g	V_{SS} = –6 V, V_{GS} = –4.5 V, I_S = –3 A		30	60	nC
Miller Charge	Q_{Miller}			6		
Gate-Source Charge	Q_{gs}			12		
Turn-On Delay Time	$t_{d(on)}$	V_{SS} = –6 V, R_L = 6 Ω I_S ≅ –1.0 A, V_{GEN} = –4.5 V, R_G = 6 Ω		45	90	ns
Rise Time	t_r			50	100	
Turn-Off Delay Time	$t_{d(off)}$			75	150	
Fall Time	t_f			105	200	

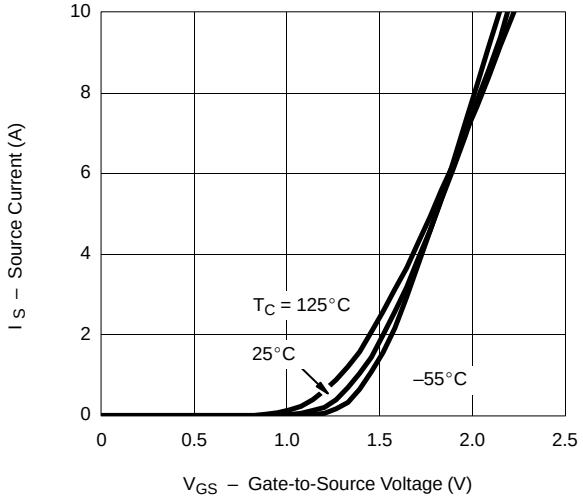
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

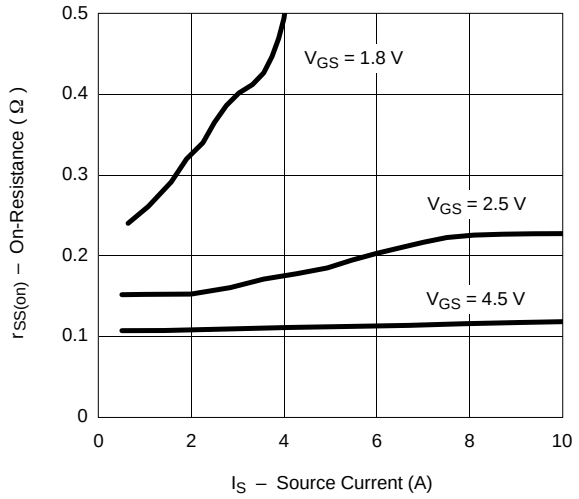
Output Characteristics



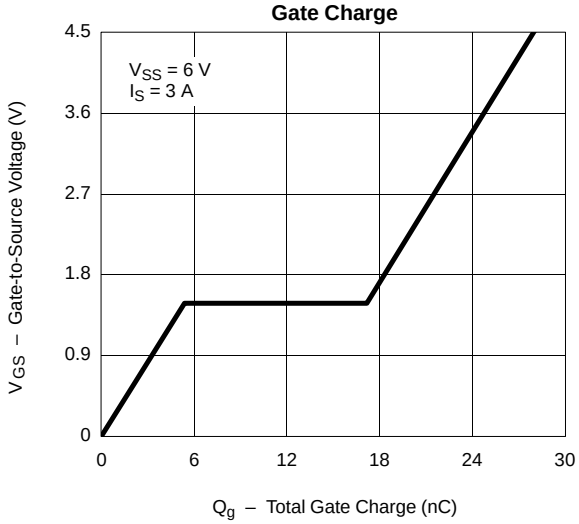
Transfer Characteristics



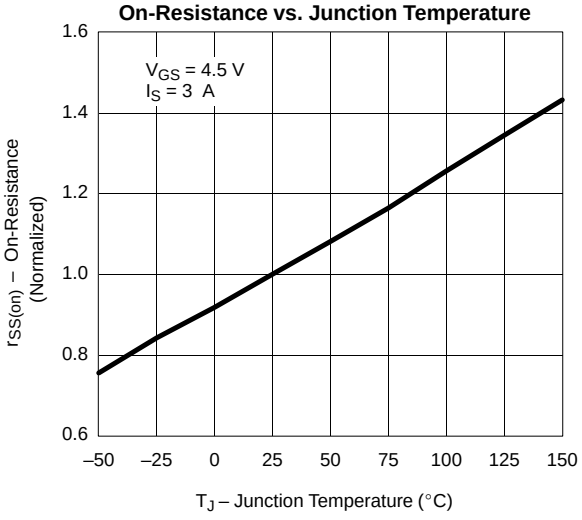
On-Resistance vs. Source Current



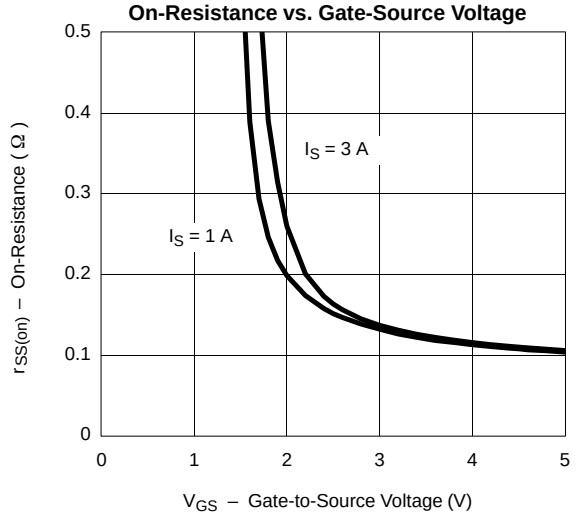
Gate Charge



On-Resistance vs. Junction Temperature

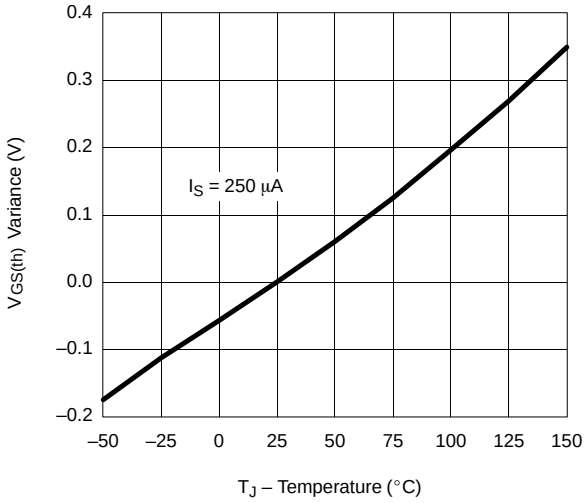


On-Resistance vs. Gate-Source Voltage

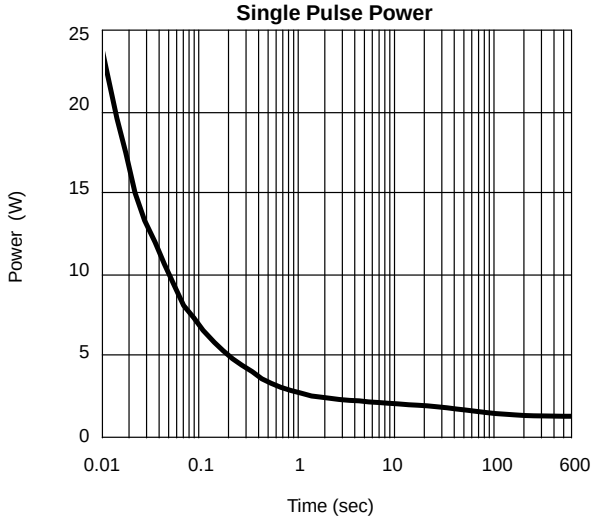


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient