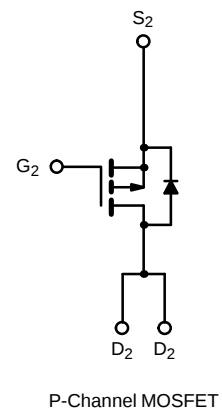
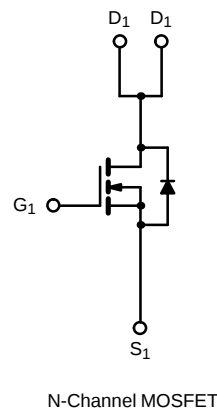
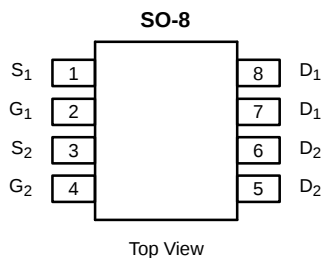




N- and P-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.025 @ $V_{GS} = 4.5$ V	± 7.1
		0.035 @ $V_{GS} = 2.5$ V	± 6.0
P-Channel	-20	0.033 @ $V_{GS} = -4.5$ V	± 6.2
		0.050 @ $V_{GS} = -2.5$ V	± 5.0

TrenchFET®
Power MOSFETs
2.5-V Rated



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	−20	V
Gate-Source Voltage		V _{GS}	± 12	± 12	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	± 7.1	± 6.2	A
	T _A = 70 °C		± 5.7	± 4.9	
Pulsed Drain Current		I _{DM}	± 40	± 40	
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	−1.7	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	2.0	2.0	W
	T _A = 70 °C		1.3	1.3	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition		Min	Typ ^a	Max	Unit	
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6			V	
		V _{DS} = V _{GS} , I _D = −250 μA	P-Ch	−0.6				
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	N-Ch P-Ch			± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = −20 V, V _{GS} = 0 V	P-Ch			−1		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55°C	N-Ch			5		
		V _{DS} = −20 V, V _{GS} = 0 V, T _J = 55°C	P-Ch			−5		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	20			A	
		V _{DS} ≤ −5 V, V _{GS} = −4.5 V	P-Ch	−20				
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 7.1 A	N-Ch		0.019	0.025	Ω	
		V _{GS} = −4.5 V, I _D = −6.2 A	P-Ch		0.027	0.033		
		V _{GS} = 2.5 V, I _D = 6.0 A	N-Ch		0.025	0.035		
		V _{GS} = −2.5 V, I _D = −5.0 A	P-Ch		0.040	0.050		
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 7.1 A	N-Ch		27		S	
		V _{DS} = −10 V, I _D = −6.2 A	P-Ch		20			
Diode Forward Voltage ^b	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch			1.2	V	
		I _S = −1.7 A, V _{GS} = 0 V	P-Ch			−1.2		
Dynamic ^a								
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 7.1 A P-Channel V _{DS} = −10 V, V _{GS} = −4.5 V, I _D = −6.2 A	N-Ch P-Ch		25 22	50 35	nC	
Gate-Source Charge	Q _{gs}		N-Ch P-Ch		6.5 7			
Gate-Drain Charge	Q _{gd}		N-Ch P-Ch		4 3.5			
Turn-On Delay Time	t _{d(on)}		N-Ch P-Ch		40 27	60 50		
Rise Time	t _r	N-Channel V _{DD} = 10 V, R _L =10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω P-Channel V _{DD} = −10 V, R _L = 10 Ω I _D ≅ −1 A, V _{GEN} = −4.5 V, R _G = 6 Ω	N-Ch P-Ch		40 32	60 50	ns	
Turn-Off Delay Time	t _{d(off)}		N-Ch P-Ch		90 95	150 150		
Fall Time	t _f		N-Ch P-Ch		40 45	60 70		
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.7 A, di/dt = 100 A/μs	N-Ch		40		80
			I _F = −1.7 A, di/dt = 100 A/μs	P-Ch		40		80

Notes

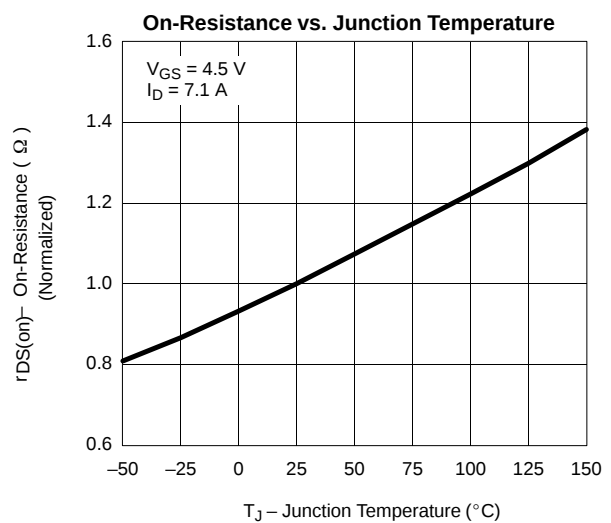
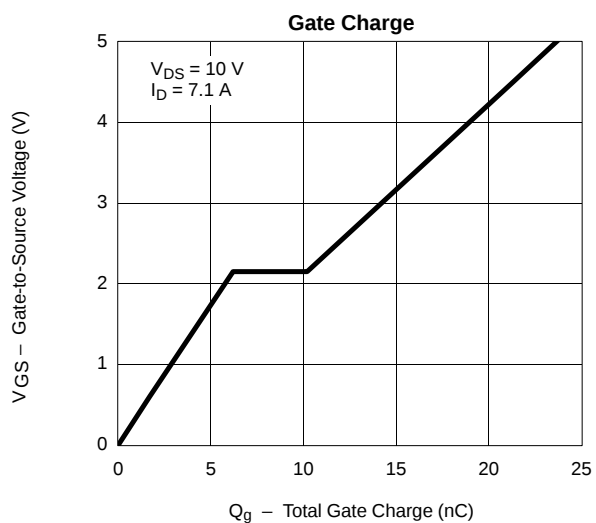
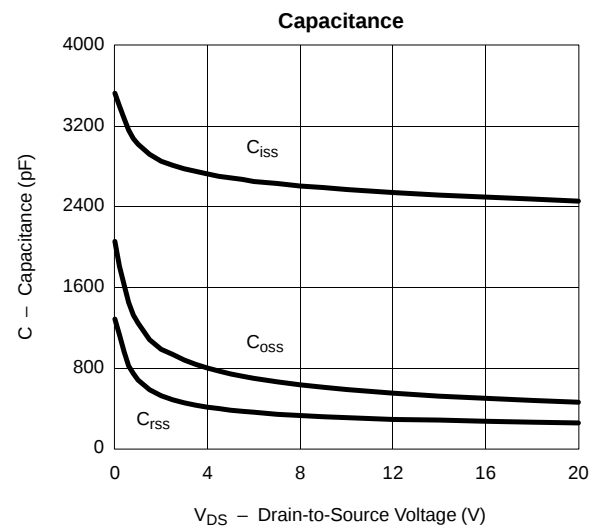
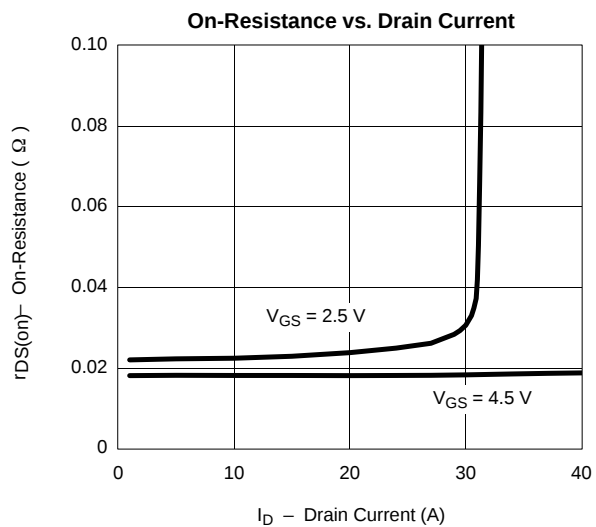
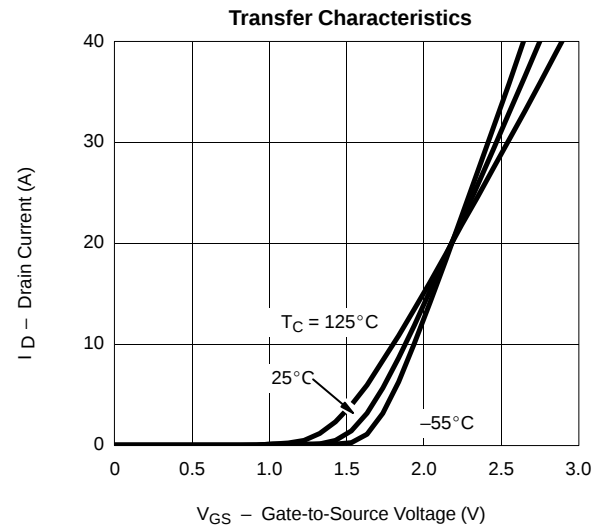
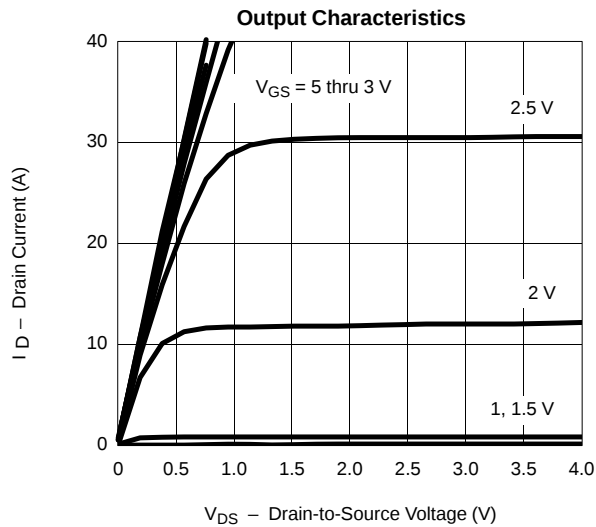
a. For design aid only; not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.



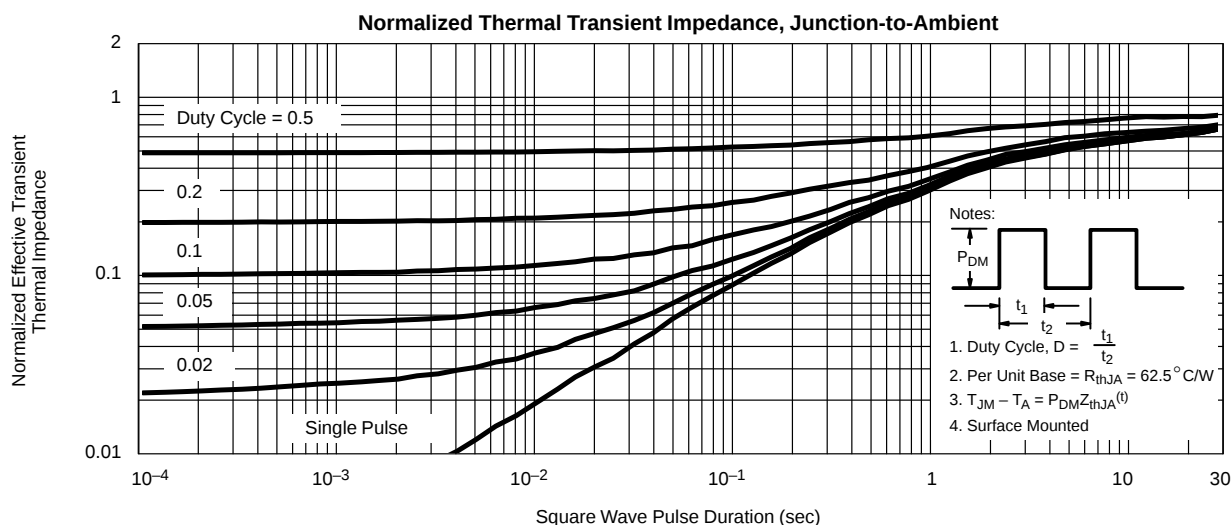
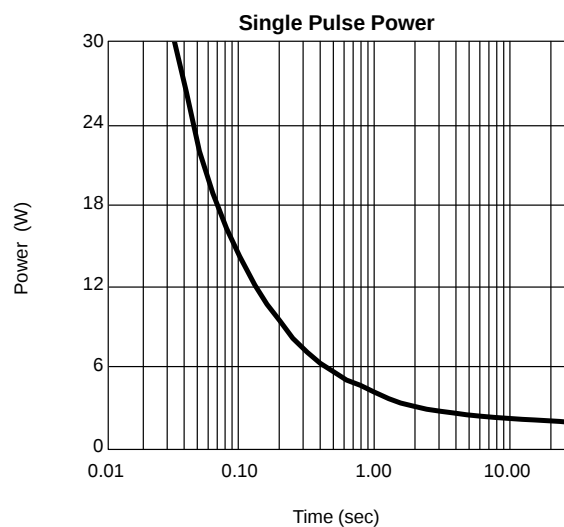
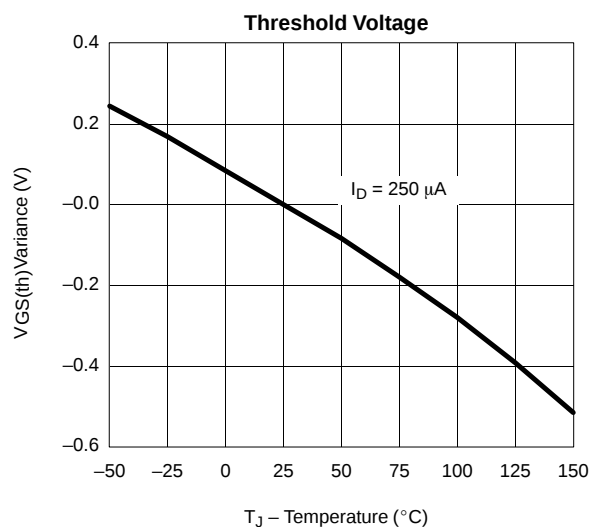
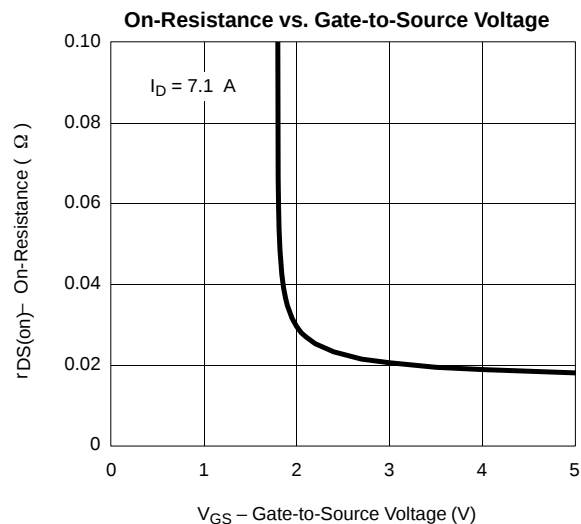
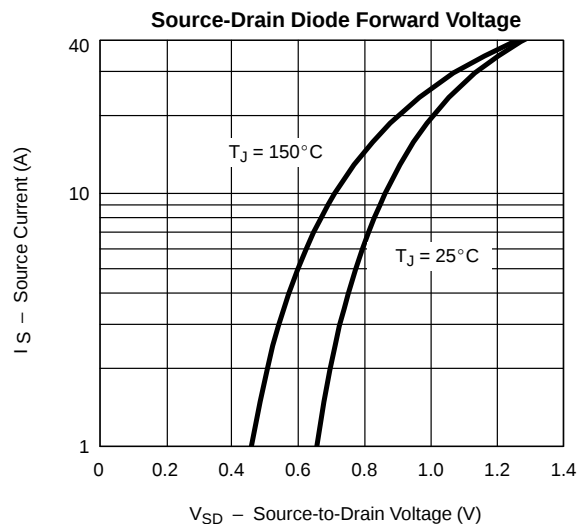
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

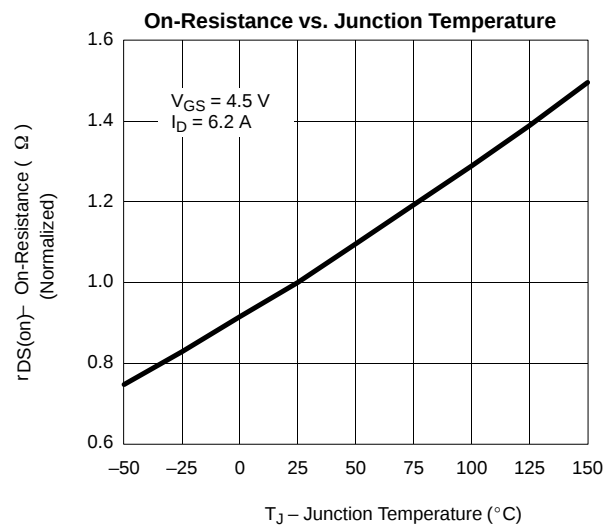
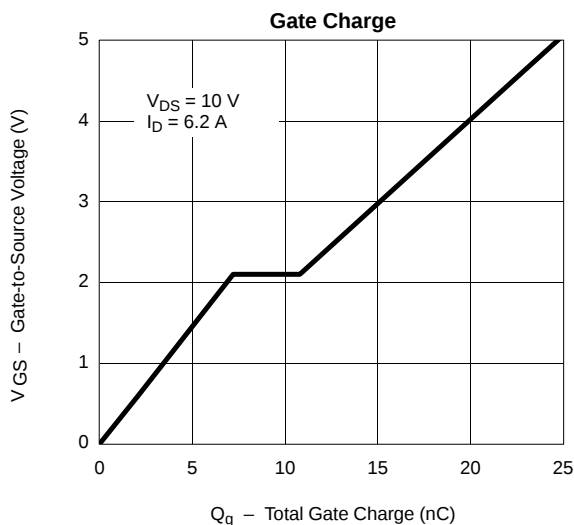
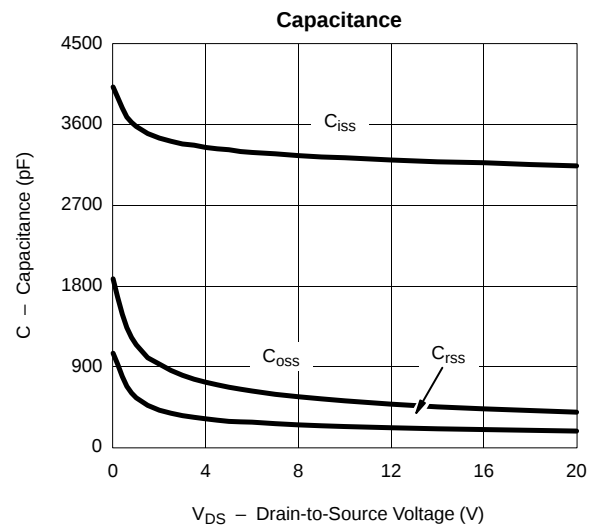
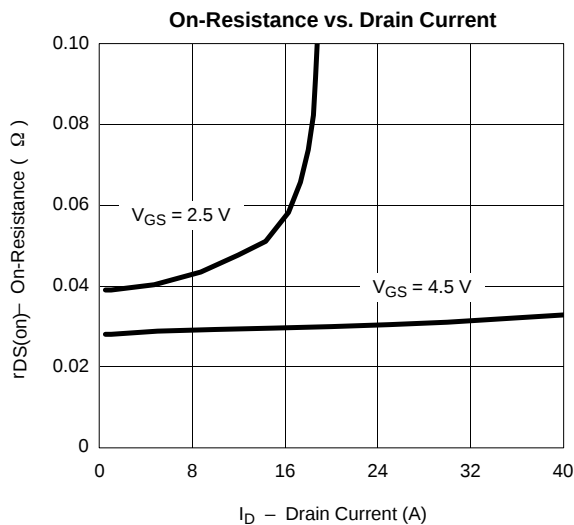
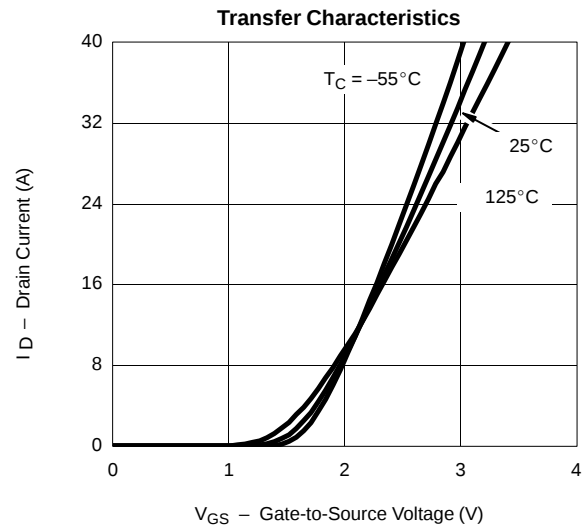
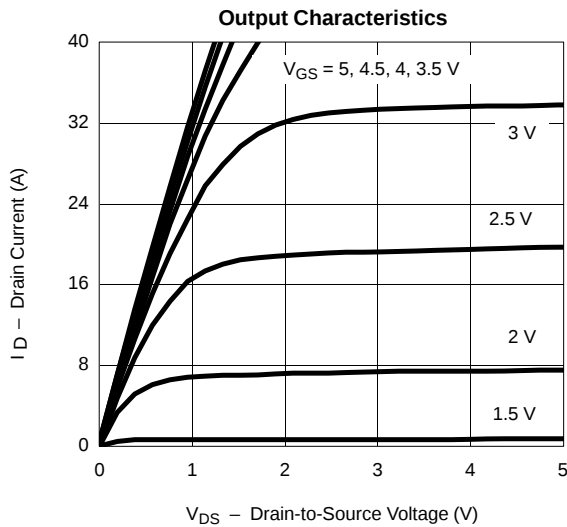
N-CHANNEL





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL

