



N-Channel Lateral DMOS FETs (Available Only In Extended Hi-Rel Flow)

PRODUCT SUMMARY				
$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
20	1.5	70 @ $V_{GS} = 5\text{ V}$	0.5	2

FEATURES

- Quad SPST Switch with Zener Input Protection
- Low Interelectrode Capacitance and Leakage
- Ultra-High Speed Switching— t_{ON} : 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @ 5 V
- Low Turn-On Threshold Voltage

BENEFITS

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

APPLICATIONS

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- Video Switch
- Multiplexer
- DAC Deglitchers
- High-Speed Driver

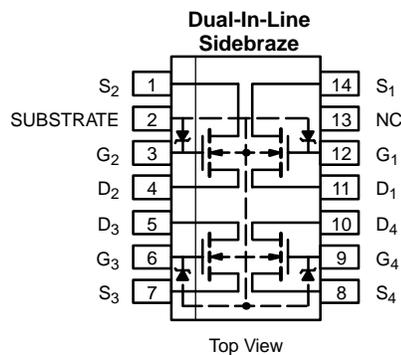
DESCRIPTION

The SD5000I-2 monolithic switch features four individual double-diffused enhancement-mode MOSFETs built on a common substrate. This bidirectional device provides low on-resistance and low interelectrode capacitances to minimize insertion loss and crosstalk.

SD5000I-2 utilizes lateral construction to achieve low capacitance and ultra-fast switching speeds. For manufacturing reliability, these devices feature poly-silicon gates protected by Zener diodes.

Built on Vishay Siliconix' proprietary DMOS process, the

The SD5000I is available only in the “-2” extended hi-rel flow. The Vishay Siliconix “-2” flow complies with the requirements of MIL-PRF-19500 for JANTX discrete devices.



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)

Gate-Drain, Gate-Source Voltage	+30 V/-25 V	Storage Temperature	-65 to 150 °C
Gate-Substrate Voltage	+30 V/-0.3 V	Operating Junction Temperature	-55 to 150 °C
Drain-Source Voltage	20 V	Power Dissipation ^{a, b} : (Package)	500 mW
Drain-Source-Substrate Voltage	25 V	(Each Device)	300 mW
Drain Current	50 mA	Notes:	
Lead Temperature (1/16" from case for 10 seconds)	300 °C	a. Derate 4 mW/°C above 25 °C	

SPECIFICATIONS^a						
Parameter	Symbol ^b	Test Conditions ^b	Limits			Unit
			Min	Typ ^c	Max	
Static						
Drain-Source Breakdown Voltage	V _{(BR)DS}	V _{GS} = V _{BS} = -5 V, I _D = 10 nA	20	30		V
Source-Drain Breakdown Voltage	V _{(BR)SD}	V _{GD} = V _{BD} = -5 V, I _S = 10 nA	20	22		
Drain-Substrate Breakdown Voltage	V _{(BR)DBO}	V _{GB} = 0 V, I _D = 10 nA, Source Open	25	35		
Source-Substrate Breakdown Voltage	V _{(BR)SBO}	V _{GB} = 0 V, I _S = 10 μA, Drain Open	25	35		
Drain-Source Leakage	I _{DS(off)}	V _{GS} = V _{BS} = -5 V	V _{DS} = 10 V	0.4		nA
			V _{DS} = 15 V	0.7		
			V _{DS} = 20 V	0.9	10	
Source-Drain Leakage	I _{SD(off)}	V _{GD} = V _{BD} = -5 V	V _{SD} = 10 V	0.5		
			V _{SD} = 15 V	0.8		
			V _{SD} = 20 V	1	10	
Gate Leakage	I _{GBS}	V _{DB} = V _{SB} = 0 V, V _{GB} = 30V		0.01	100	
Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 μA, V _{SB} = 0 V	0.1	0.8	1.5	V
Drain-Source On-Resistance	r _{DS(on)}	V _{SB} = 0 V I _D = 1 mA	V _{GS} = 5 V	58	70	Ω
			V _{GS} = 10 V	38		
			V _{GS} = 15 V	30		
			V _{GS} = 20 V	26		
Resistance Match	Δr _{DS(on)}		V _{GS} = 5 V	1	5	
Dynamic						
Forward Transconductance	g _{fs}	V _{DS} = 10 V, V _{SB} = 0 V, I _D = 20 mA, f = 1 kHz	10	12		mS
Gate-Node Capacitance	C _(GS+GD+GB)	V _{DS} = 10 V, f = 1 MHz V _{GS} = V _{BS} = -15 V		2.5	3.5	pF
Drain-Node Capacitance	C _(GD+DB)			2.0	3	
Source-Node Capacitance	C _(GS+SB)			3.7	5	
Reverse Transfer Capacitance	C _{rSS}			0.2	0.5	
Crosstalk		f = 3 kHz		-107		dB
Switching						
Turn-On Time	t _{d(on)}	V _{SB} = 5 V, V _{IN} 0 to 5 V, R _G = 25 Ω V _{DD} = 5 V, R _L = 680 Ω		0.5	1	ns
	t _r			0.6	1	
Turn-Off Time	t _{d(off)}			2		
	t _f			6		

Notes:

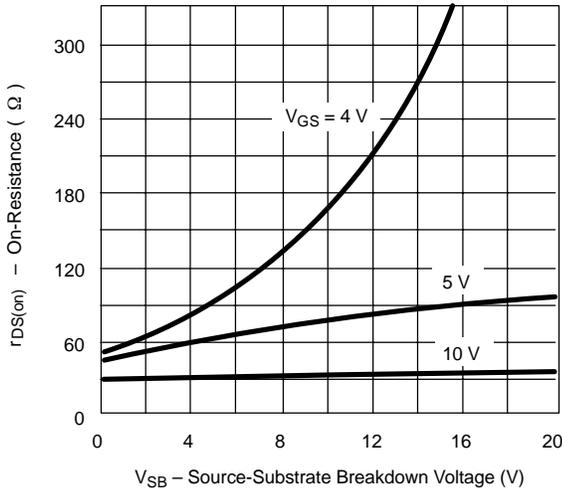
- T_A = 25 °C unless otherwise noted.
- B is the body (substrate) and V_(BR) is breakdown.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

DMCA

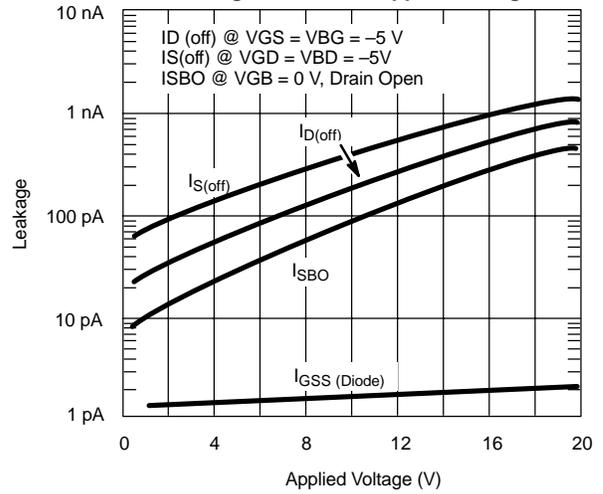


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

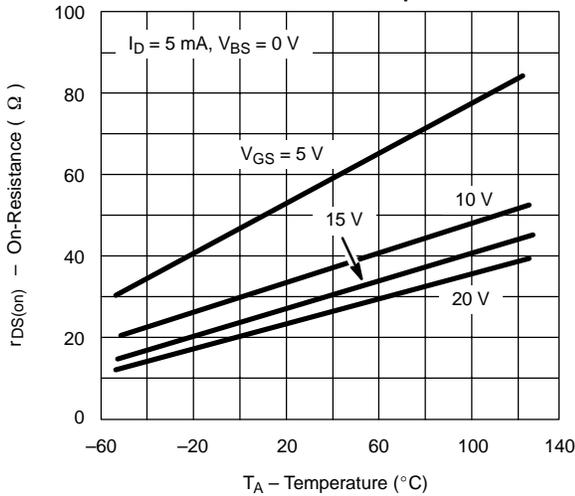
On-Resistance vs. Gate-Source Voltage



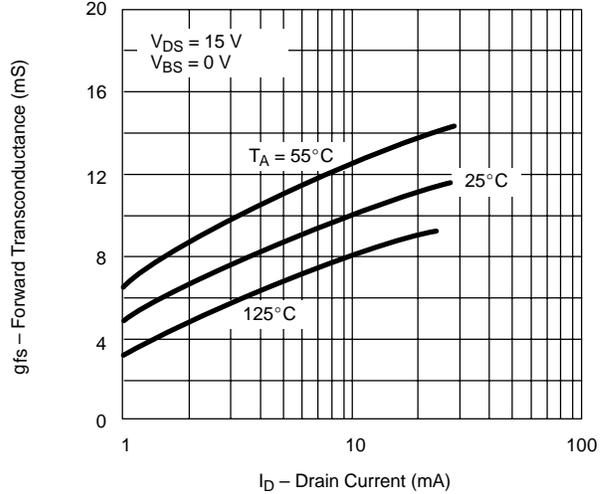
Leakage Current vs. Applied Voltage



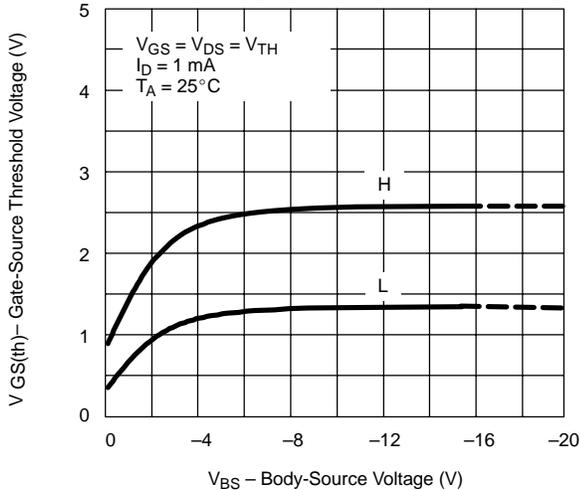
On-Resistance vs. Temperature



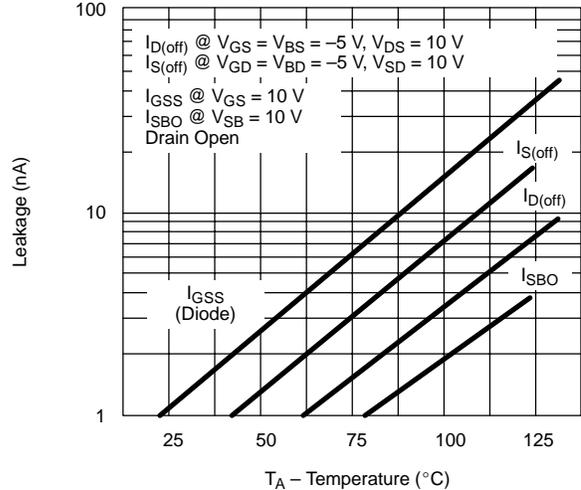
Common-Source Forward Transconductance vs. Drain Current



Threshold Voltage vs. Substrate-Source Voltage

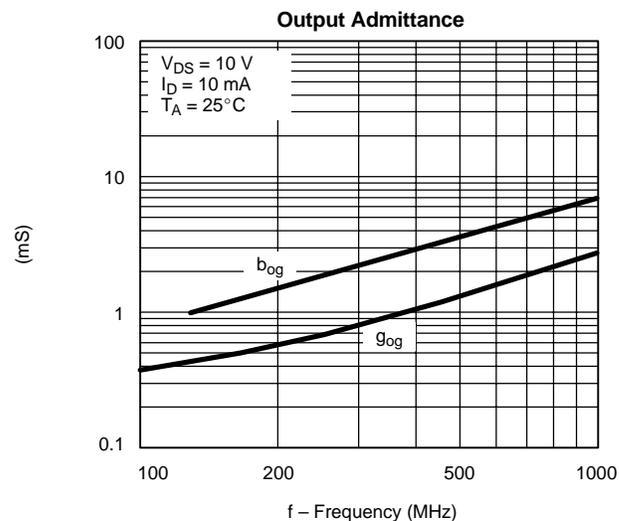
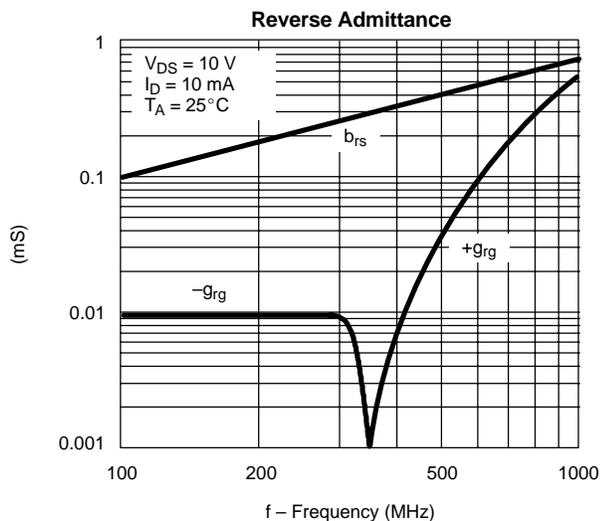
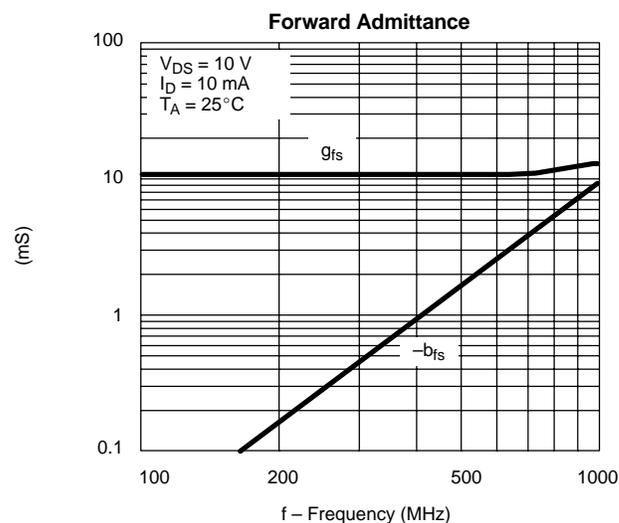
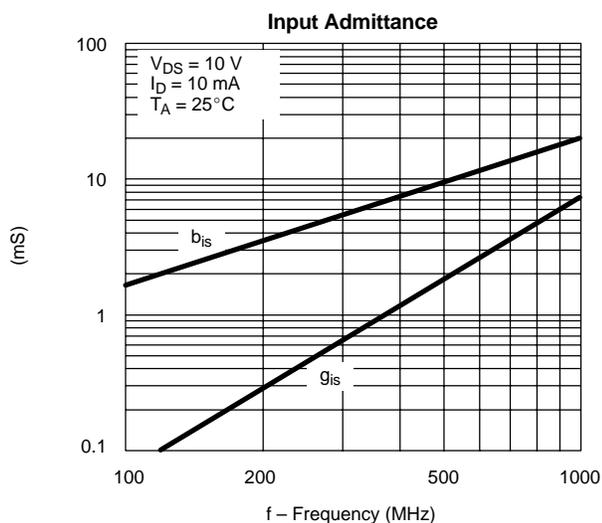
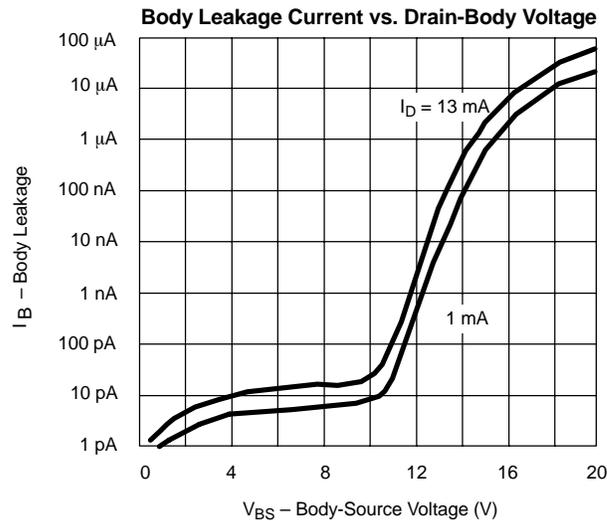
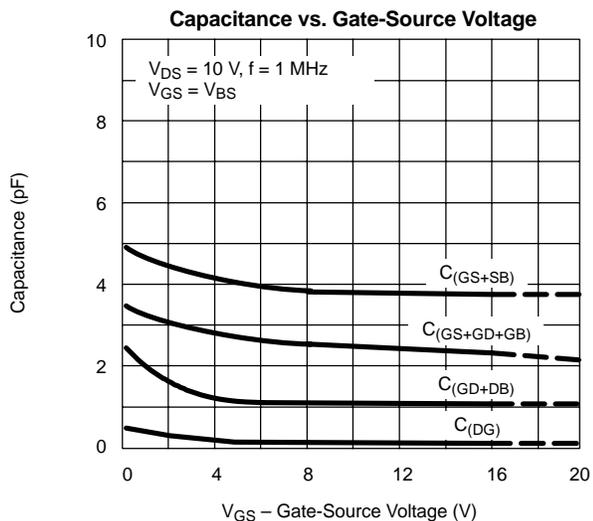


Leakage Current vs. Temperature

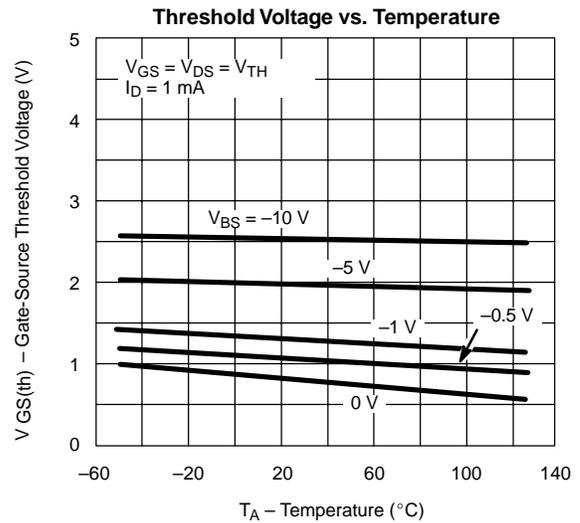
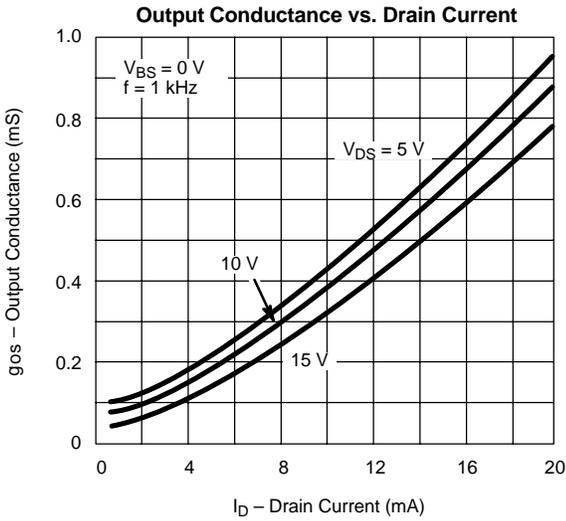
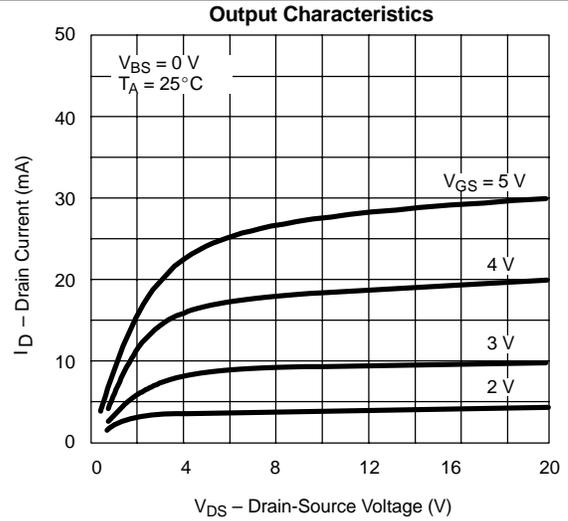
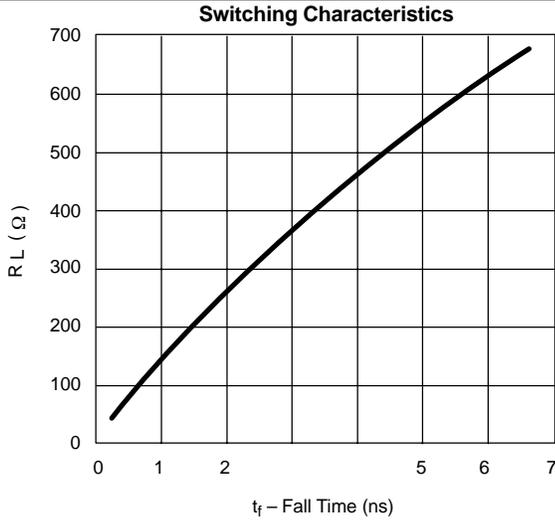




TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



SWITCHING TIME TEST CIRCUIT

