N-Channel Lateral DMOS FETs

(Available Only In Extended Hi-Rel Flow)

PRODUCT SUMMARY					
Part Number	**$V_{(BR)DS}$ Min (V)**	**$V_{GS(th)}$ Max (V)**	**$r_{DS(on)}$ Max (Ω)**	**C_{rss} Max (pF)**	**t_{ON} Max (ns)**
SD211DE-2	30	1.5	45 @ V_{GS} = 10 V	0.5	2
SD213DE-2	10	1.5	45 @ V_{GS} = 10 V	0.5	2
SD215DE-2	20	1.5	45 @ V_{GS} = 10 V	0.5	2

FEATURES

- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @ 5 V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

BENEFITS

- High Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

APPLICATIONS

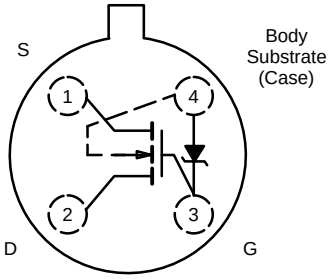
- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

DESCRIPTION

The SD211DE-2 series consists of enhancement- mode MOSFETs designed for high speed low-glitch switching in audio, video, and high-frequency applications. The SD211DE-2 may be used for ±5-V analog switching or as a high speed driver of the SD214DE-2. The SD214DE-2 is normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. An integrated Zener diode provides ESD protection. These devices feature a poly-silicon gate for manufacturing reliability.

The SD211DE/213DE/215DE are available only in the "–2" extended hi-rel flow. The Vishay Siliconix "–2" flow complies with the requirements of MIL-PRF-19500 for JANTX discrete devices.

TO-206AF (TO-72)



Top View

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Gate-Drain, Gate-Source Voltage
(SD211DE-2) . . . . . –30/25 V
(SD213DE-2) . . . . . –15/25 V
(SD215DE-2) . . . . . –25/30 V

Gate-Substrate Voltage (Derate 3 mW/°C above 25°C)
(SD211DE-2) . . . . . –0.3/25 V
(SD213DE-2) . . . . . –0.3/25 V
(SD215DE-2) . . . . . –0.3/30 V

Drain-Source Voltage
(SD211DE-2) . . . . . 30 V
(SD213DE-2) . . . . . 10 V
(SD215DE-2) . . . . . 20 V

Source-Drain Voltage
(SD211DE-2) . . . . . 10 V
(SD213DE-2) . . . . . 10 V
(SD215DE-2) . . . . . 20 V

Drain-Substrate Voltage
(SD211DE-2) . . . . . 30 V
(SD213DE-2) . . . . . 15 V
(SD215DE-2) . . . . . 25 V

Source-Substrate Voltage
(SD211DE-2) . . . . . 15 V
(SD213DE-2) . . . . . 15 V
(SD215DE-2) . . . . . 25 V

Drain Current . . . . . 50 mA

Lead Temperature ($^1/_{16}$" from case for 10 seconds) . . . . . 300°C

Storage Temperature . . . . . –65 to 150°C

Operating Junction Temperature . . . . . –55 to 125°C

Power Dissipation (Derate 3 mW/°C above 25°C) . . . . . 300 mW

Applications Information—See Applications Note AN502

SPECIFICATIONS[a]

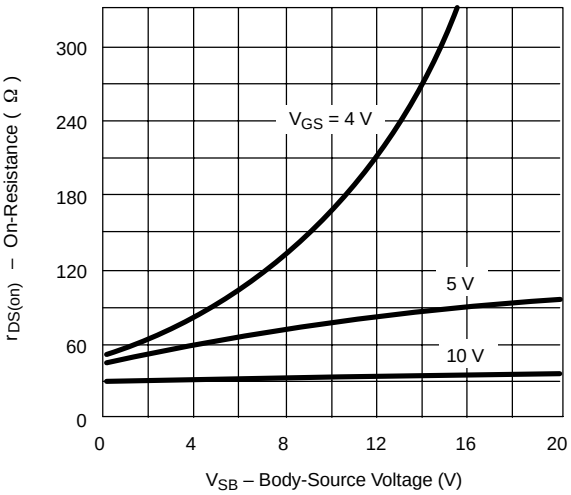
Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits 211DE-2 Min	211DE-2 Max	213 DE-2 Min	213 DE-2 Max	215 DE-2 Min	215 DE-2 Max	Unit
Static											
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DBO}$	$V_{GB} = 0$ V, $I_D = 10$ nA Source Open		35	15		15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SBO}$	$V_{GB} = 0$ V, $I_S = 10$ µA Drain Open		35	15		15		25		
Drain-Source Leakage	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
Source-Drain Leakage	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			
			$V_{SD} = 20$ V	1						10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$V		0.01		100		100		100	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ µA, $V_{SB} = 0$ V		0.8	0.5	1.5	0.1	1.5	0.1	1.5	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58		70		70		70	Ω
			$V_{GS} = 10$ V	38		45		45		45	
			$V_{GS} = 15$ V	30							
			$V_{GS} = 20$ V	26							
			$V_{GS} = 25$ V	24							
Dynamic											
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, f = 1 kHz		11	10		10		10		mS
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, f = 1 MHz $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5		0.5	
Switching											
Turn-On Time	$t_{d(on)}$	$V_{SB} = 0$ V, V_{IN} 0 to 5 V, $R_G = 25$ Ω $V_{DD} = 5$ V, $R_L = 680$ Ω		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-Off Time	$t_{d(off)}$			2							
	t_f			6							

Notes:
a. $T_A = 25°C$ unless otherwise noted.
b. B is the body (substrate), and (BR) is breakdown.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

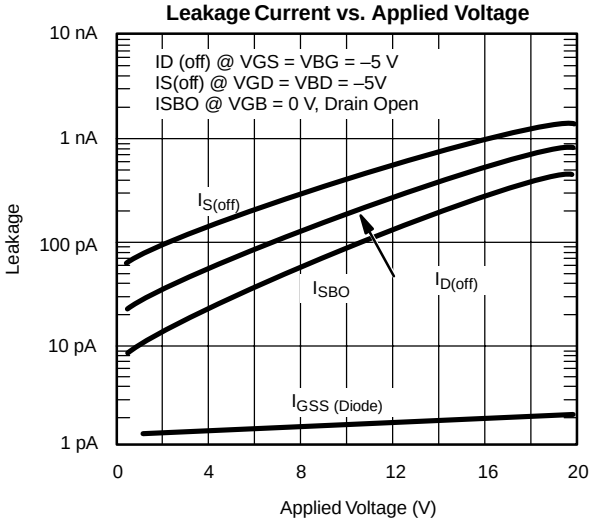
DMCBA

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

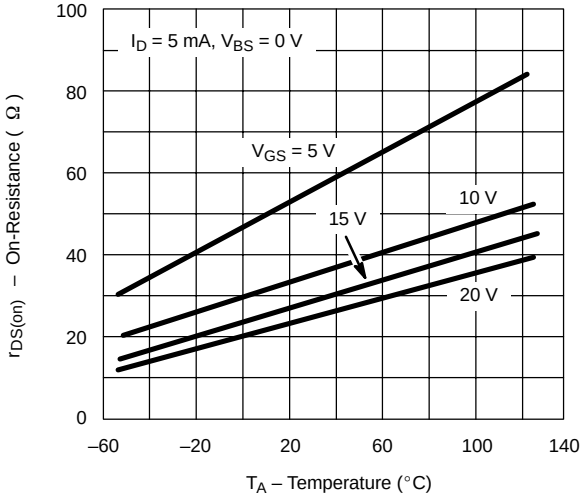
On-Resistance vs. Gate-Source Voltage



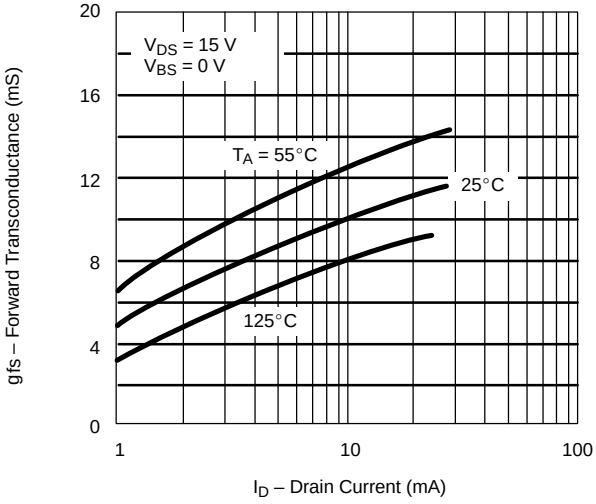
Leakage Current vs. Applied Voltage



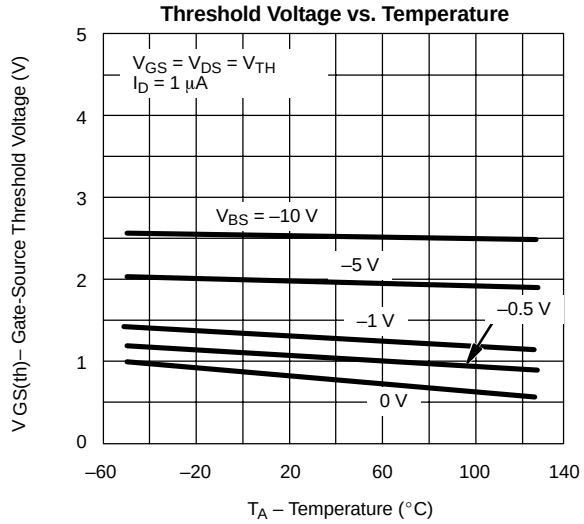
On-Resistance vs. Temperature



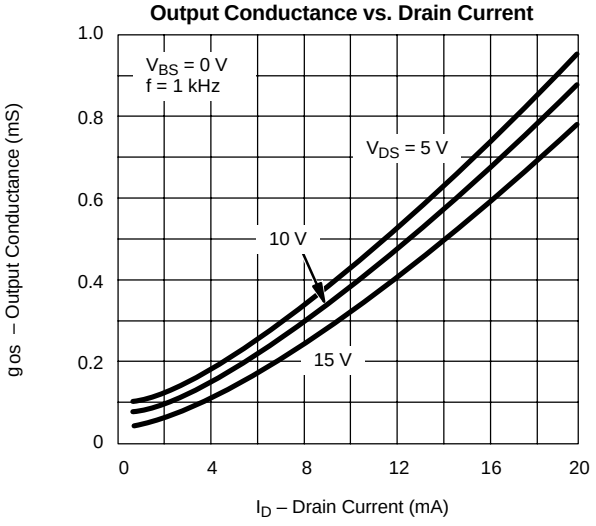
Common-Source Forward Transconductance vs. Drain Current



Threshold Voltage vs. Temperature

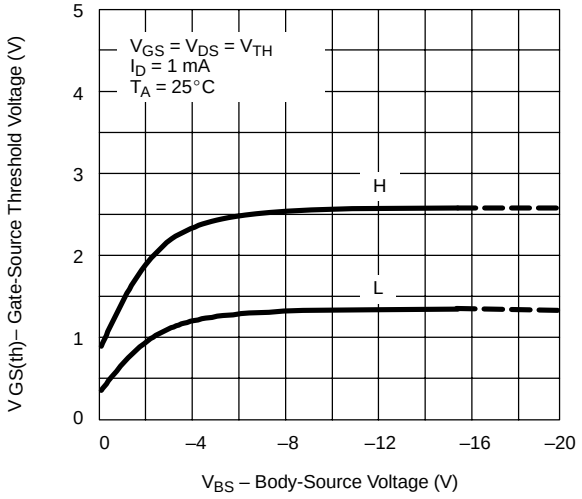


Output Conductance vs. Drain Current

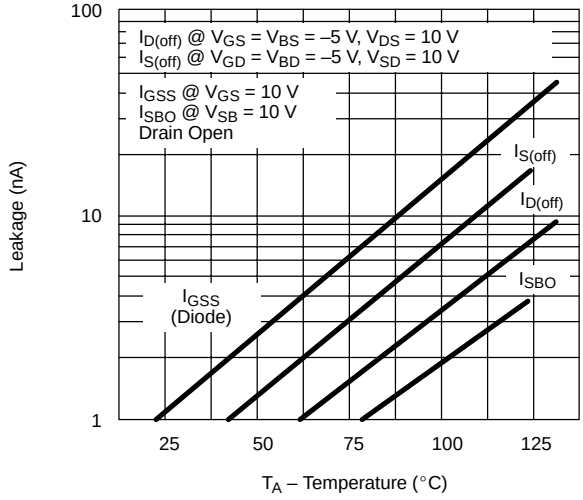


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

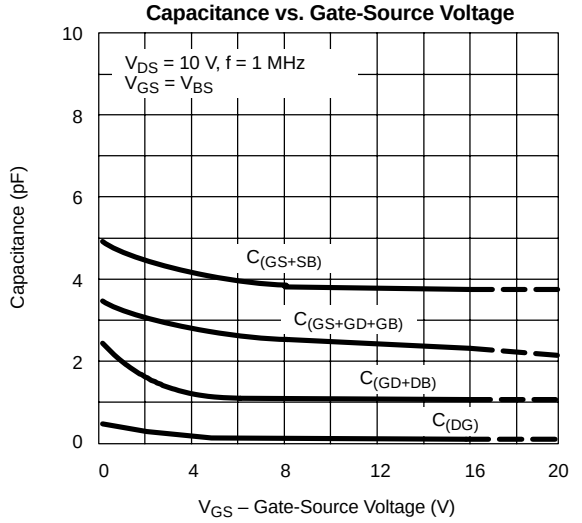
Threshold Voltage vs. Substrate-Source Voltage



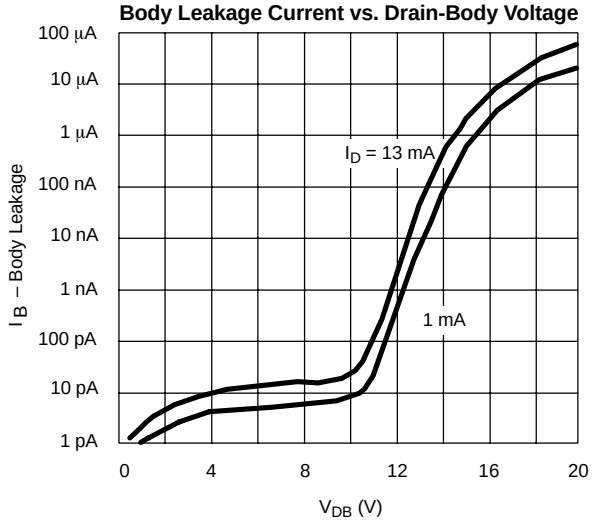
Leakage Current vs. Temperature



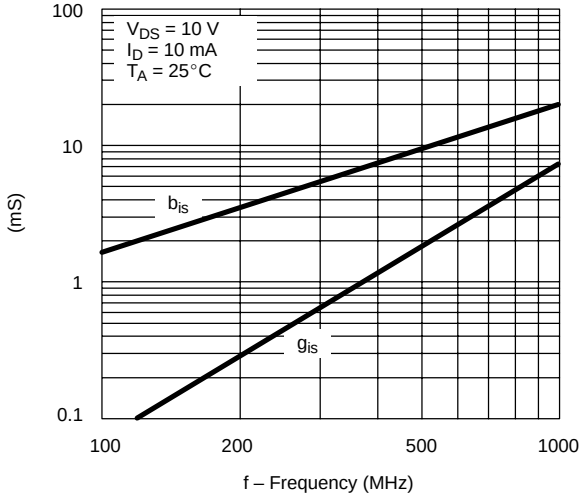
Capacitance vs. Gate-Source Voltage



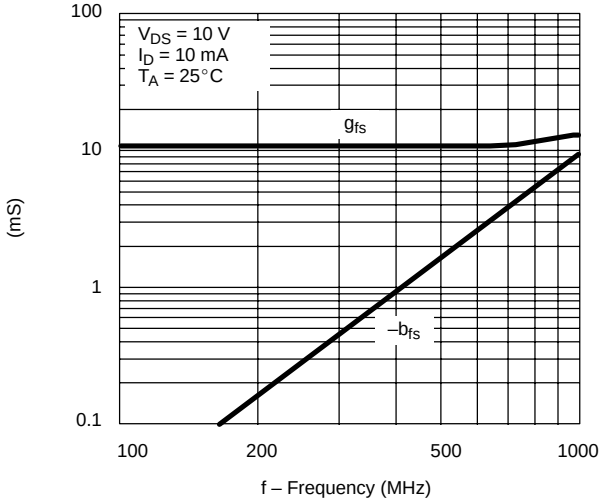
Body Leakage Current vs. Drain-Body Voltage



Input Admittance

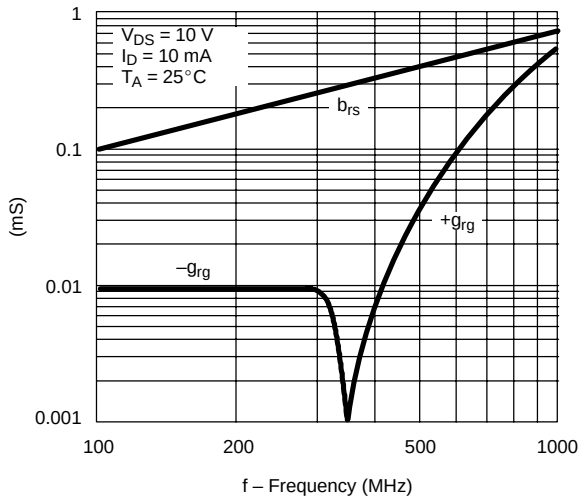


Forward Admittance

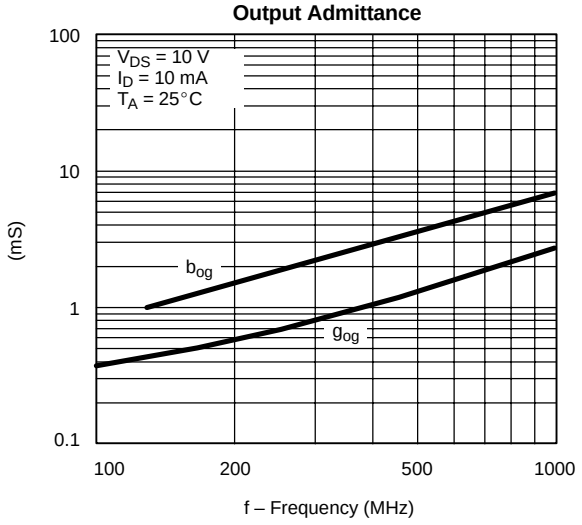


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

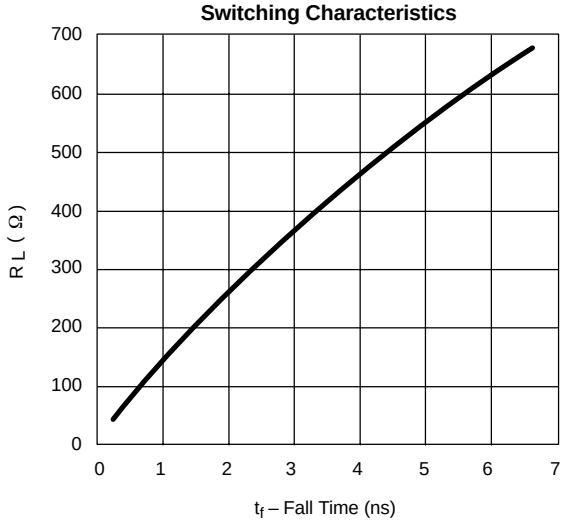
Reverse Admittance



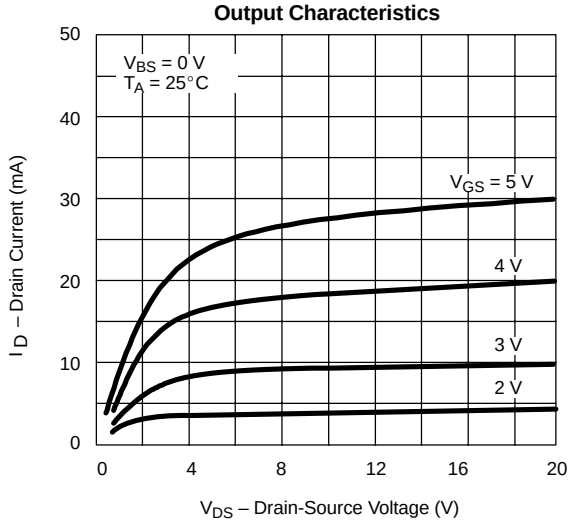
Output Admittance



Switching Characteristics



Output Characteristics



SWITCHING TIME TEST CIRCUIT