



1-W High-Voltage Switchmode Regulator

FEATURES

- CCITT Compatible
- Current-Mode Control
- Low Power Consumption (less than 5 mW)
- 10- to 120-V Input Range
- 200-V, 250-mA MOSFET
- Internal Start-Up Circuit
- Current-Mode Control
- SHUTDOWN and RESET

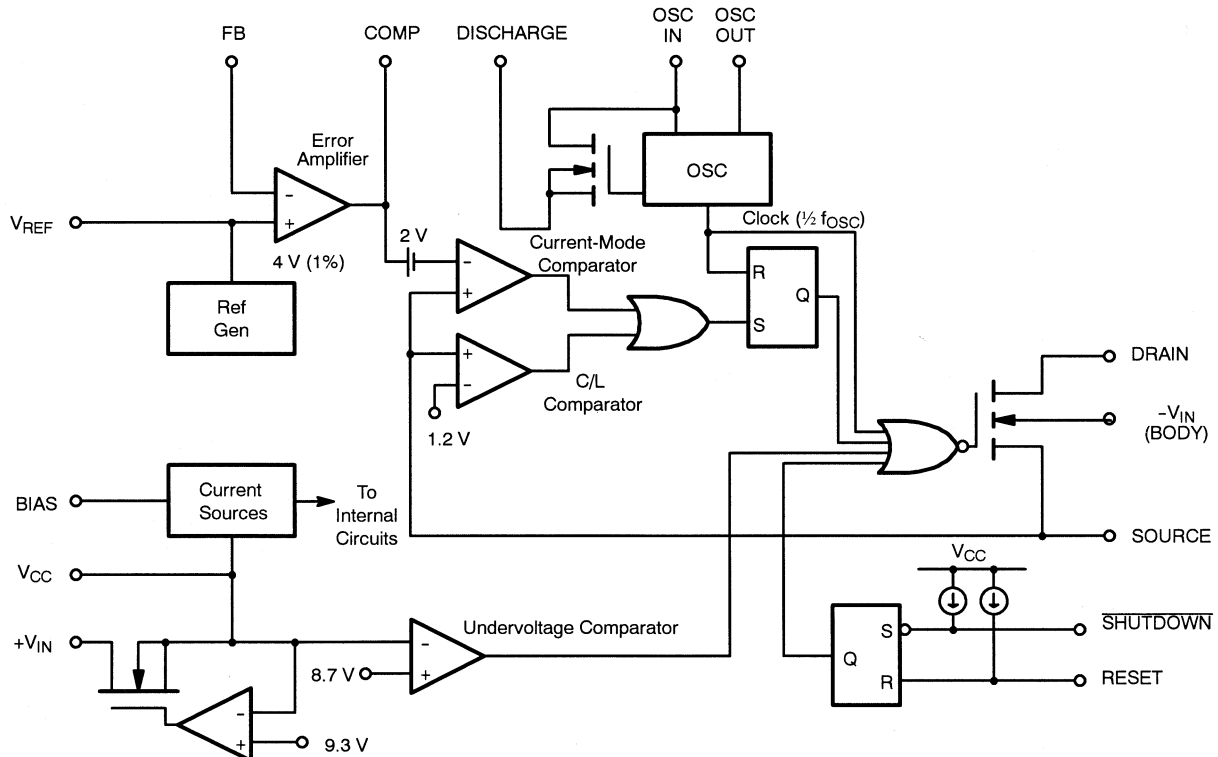
DESCRIPTION

The Si9105 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc/dc converter in ISDN terminals up to 3 watts. A 0.5-mA max supply current makes possible the design of a dc/dc converter with 60% efficiency at 25 mW, therefore meeting the recommended performance under the CCITT I.430 specifications.

This device may be used with an appropriate transformer to implement isolated flyback power converter topologies to provide single or multiple regulated dc outputs (i.e., ± 5 V).

The Si9105 is available in 16-pin wide-body SOIC, 14-pin plastic DIP, and 20-pin PLCC packages, and is specified over the industrial, D suffix (-40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)

V_{CC}	15 V
$+V_{IN}$	120 V
V_{DS}	200 V
I_D (Peak) (300 μ s pulse, 2% duty cycle)	2 A
I_D (rms)	250 mA
Logic Inputs (RESET, SHUTDOWN, OSC IN) ..	-0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SOURCE)	-0.3 V to 7 V
HV Pre-Regulator Input Current (continuous)	5 mA
Storage Temperature	-65 to 125°C
Operating Temperature	-40 to 85°C
Junction Temperature (T_J)	150°C

Power Dissipation (Package)^a

14-Pin Plastic DIP (J Suffix) ^b	750 mW
16-Pin Plastic Wide-Body SOIC (W Suffix) ^c	900 mW
20-Pin PLCC (N Suffix) ^d	1400 mW
Thermal Impedance (Θ_{JA})	
14-Pin Plastic DIP	167°C/W
16-Pin Plastic Wide-Body SOIC	140°C/W
20-Pin PLCC	90°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 6 mW/°C above 25°C

c. Derate 7.2 mW/°C above 25°C

d. Derate 11.2 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$

V_{CC}	10 V to 13.5 V
$+V_{IN}$	10 V to 120 V
f_{OSC}	40 kHz to 1 MHz

 R_{OSC}

Linear Inputs

Digital Inputs

SPECIFICATIONS^a

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN} = 0$ V $V_{CC} = 10$ V, $+V_{IN} = 48$ V $R_{BIAS} = 820$ k Ω , $R_{OSC} = 910$ k Ω	Temp ^b	Limits D Suffix -40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Reference							
Output Voltage	V_R	OSC IN = V_{IN} (OSC Disabled), $R_L = 10$ M Ω	Room	3.92	4.00	4.08	V
Output Impedance ^e	Z_{OUT}	OSC IN = $-V_{IN}$	Room	15	300	45	k Ω
Short Circuit Current	I_{SREF}	OSC IN = $-V_{IN}$, $V_{REF} = -V_{IN}$	Room	70	100	130	μ A
Temperature Stability ^e	T_{REF}	OSC IN = $-V_{IN}$	Full		0.25	1.0	mV/°C
Long Term Stability ^e		t = 1000 hrs, $T_A = 125^\circ$ C	Room		5.00	25.00	mV
Oscillator							
Maximum Frequency ^e	f_{MAX}	$R_{OSC} = 0$	Room	1	3		MHz
Initial Accuracy	f_{OSC}	See Note e	Room	32	40	48	kHz
Voltage Stability	$\Delta f/f$	$\Delta f/f = f(13.5 \text{ V}) - f(9.5 \text{ V})/f(9.5 \text{ V})$	Room		10	15	%
Temperature Coefficient ^e	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.96	4	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, $V_{FB} = 4$ V	Room		25	500	nA
Open Loop Voltage Gain ^e	A_{VOL}	OSC IN = $-V_{IN}$ (OSC Disabled)	Room	60	80		dB
Input Offset Voltage	V_{OS}	OSC IN = $-V_{IN}$	Room		± 15	± 40	mV
Unity Gain Bandwidth ^e	BW		Room	0.5	0.8		MHz
Dynamic Output Impedance	Z_{OUT}		Room		1		k Ω
Output Current	I_{OUT}	Source ($V_{FB} = 3.4$ V)	Room		-1.2	-0.32	mA
		Sink ($V_{FB} = 4.5$ V)	Room	0.05	0.08		

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SPECIFICATIONS ^a							
Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = -V _{IN} = 0 V V _{CC} = 10 V, +V _{IN} = 48 V R _{BIAS} = 820 kΩ, R _{OSC} = 910 kΩ	Temp ^b	Limits D Suffix -40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Power Supply Rejection	PSRR	10 V ≤ V _{CC} ≤ 13.5 V	Room		70		dB
Current Limit							
Threshold Voltage	V _{SOURCE}	R _L = 100 Ω from DRAIN to V _{CC} V _{FB} = 0 V	Room	0.8	1.0	1.2	V
Delay to Output ^e	t _d	R _L = 100 Ω from DRAIN to V _{CC} V _{SOURCE} = 1.5 V, See Figure 1.	Room		200	300	ns
Input Voltage	+V _{IN}	I _{IN} = 10 μA	Room	120			V
Input Leakage Current	+I _{IN}	V _{CC} ≥ 10 V	Room			10	μA
Pre-Regulator Start-Up Current	I _{START}	Pulse Width ≤ 300 μs, V _{CC} = 7 V	Room	8	15		mA
V _{CC} Pre-Regulator Turn-Off Threshold Voltage	V _{REG}	I _{PRE-REGULATOR} = 10 μA	Room	7.5	9.3	9.7	V
Undervoltage Lockout	V _{UVLO}	R _L = 100 Ω from DRAIN to V _{CC} See Detailed Description	Room	7.0	8.7	9.2	
V _{REG} - V _{UVLO}	V _{DELTA}		Room	0.25	0.5		
Supply							
Supply Current	I _{CC}		Room		0.35	0.5	mA
Bias Current	I _{BIAS}		Room		7.5		μA
SHUTDOWN Delay	t _{SD}	V _{SOURCE} = -V _{IN} , See Figure 2.	Room		50	100	ns
SHUTDOWN Pulse Width	t _{SW}	See Figure 3.	Room	50			
RESET Pulse Width	t _{RW}		Room	50			
Latching Pulse Width SHUTDOWN and RESET Low	t _{LW}		Room	25			
Input Low Voltage	V _{IL}		Room			2.0	V
Input High Voltage	V _{IH}		Room	8.0			
Input Current Input Voltage High	I _{IH}	V _{IN} = 10 V	Room		1	5	μA
Input Current Input Voltage Low	I _{IL}	V _{IN} = 0 V	Room	-35	-25		
MOSFET Switch							
Breakdown Voltage	V _{(BR)DSS}	I _{DRAIN} = 100 μA	Full	200	220		V
Drain-Source On Resistance ^g	r _{DS(on)}	I _{DRAIN} = 100 mA	Room		5	7	Ω
Drain Off Leakage Current	I _{DSS}	V _{DRAIN} = 100 V	Room			10	μA
Drain Capacitance	C _{DS}		Room		35		pF

Notes

- Refer to PROCESS OPTION FLOWCHART for additional information.
- Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- C_{STRAY} Pin 8 = $\leq 5\text{ pF}$
- Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

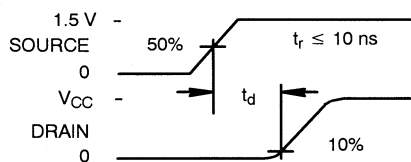


FIGURE 1.

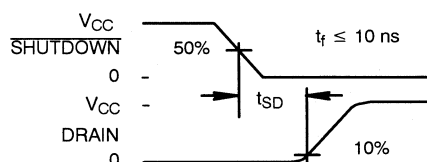


FIGURE 2.

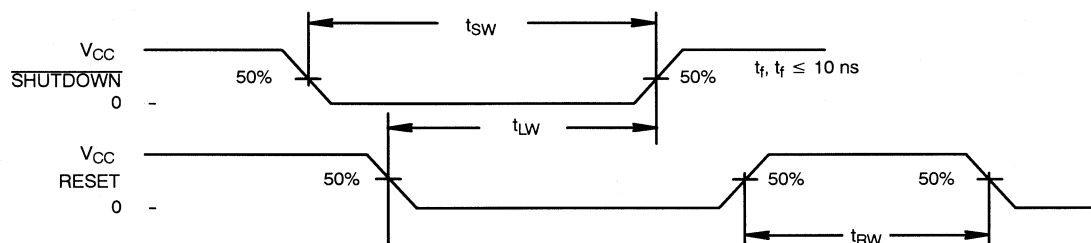


FIGURE 3.

TYPICAL CHARACTERISTICS

Output Switching Frequency vs. Oscillator Resistance

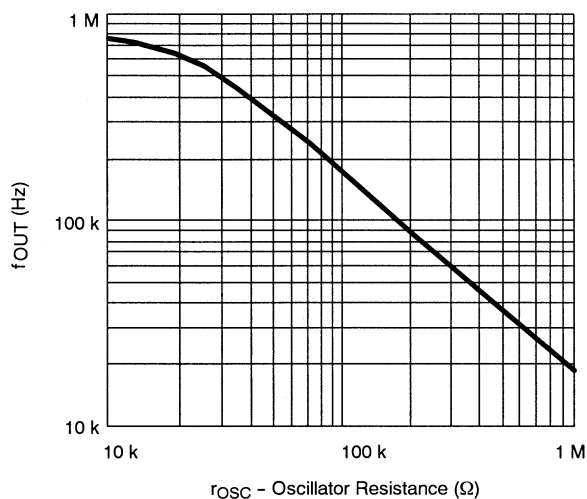
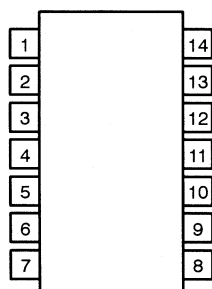


FIGURE 4.



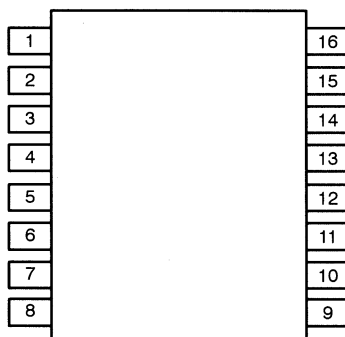
PIN CONFIGURATIONS

PDIP-14



Top View

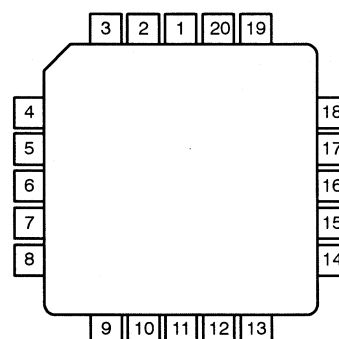
Order Number: Si9105DJ02

SO-16
(Wide-Body)

Top View

Order Number: Si9105DW

PLCC-20



Top View

Order Number: Si9105DN02

PIN DESCRIPTION			
Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
-V _{IN}	5	2	8
V _{CC}	6	4	9
OSC _{OUT}	7	5	10
OSC _{IN}	8	6	11
DISCHARGE	9	7	12
V _{REF}	10	8	14
SHUTDOWN	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
+V _{IN}	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19

DETAILED DESCRIPTION

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9105 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary “bootstrap” winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} . This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.3 V. If V_{CC} is not forced to exceed the 9.3-V threshold, then V_{CC} will be regulated to a nominal value of 9.3 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.7 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

BIAS

To properly set the bias for the Si9105, a 820-k Ω resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 7.5 μA .

Reference Section

The reference section of the Si9105 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9105 brings the output of the error amplifier (which is configured for unity gain during trimming) to within $\pm 1\%$ of 4 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, whose 1-k Ω dynamic output impedance enables it to be used

with feedback compensation (unlike transconductance amplifiers). A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Typical Characteristics graph of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to a maximum of 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5- μs pulse width, typical values would be 100 pF in series with 3 k Ω to OSC IN.

SHUTDOWN and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ pin to provide variable shutdown time.

Output Switch

The output switch is a 7- Ω , 200-V lateral DMOS transistor. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9105 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

TABLE 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H		Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
	L	Off (Latched, No Change)

APPLICATIONS

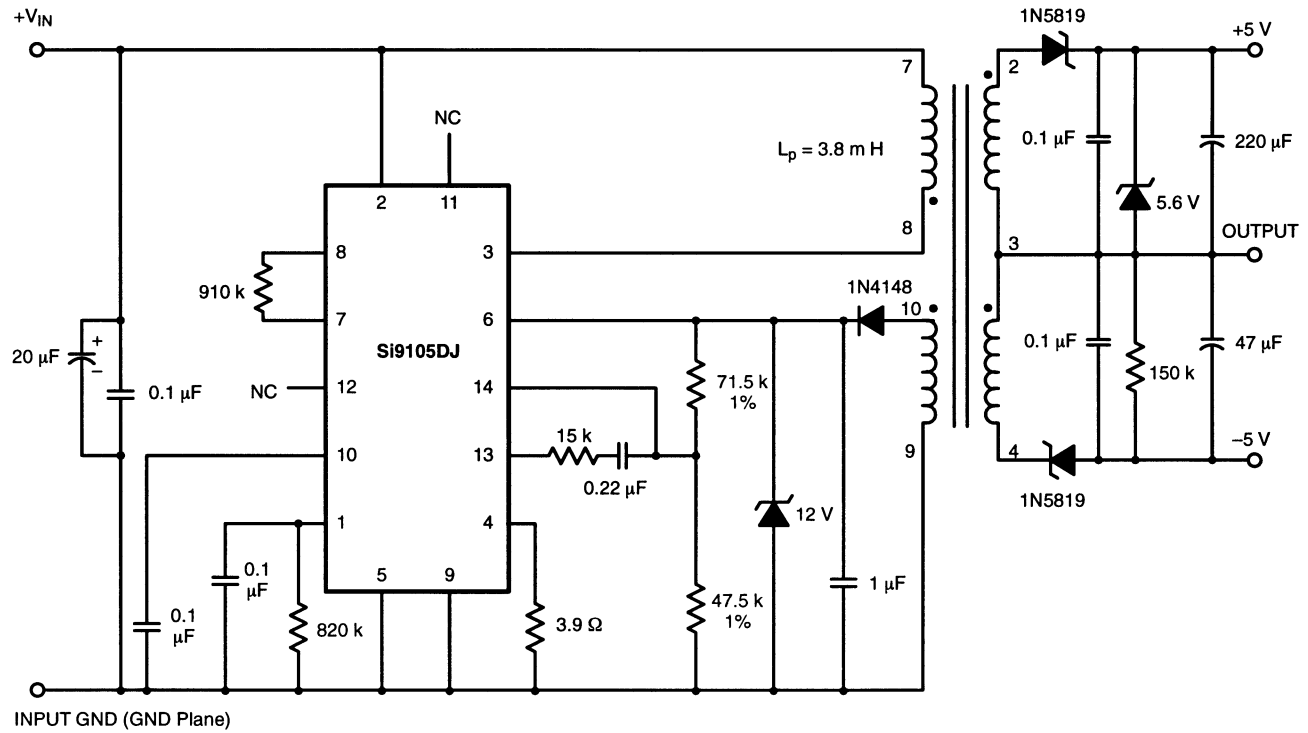


FIGURE 5. CCITT Compatible ISDN Terminal Power Supply