



High-Voltage Switchmode Regulator

FEATURES

- 10- to 120-V Input Range
- Current-Mode Control
- On-Chip 200-V, 5- Ω MOSFET Switch
- SHUTDOWN and RESET
- High Efficiency Operation (>80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

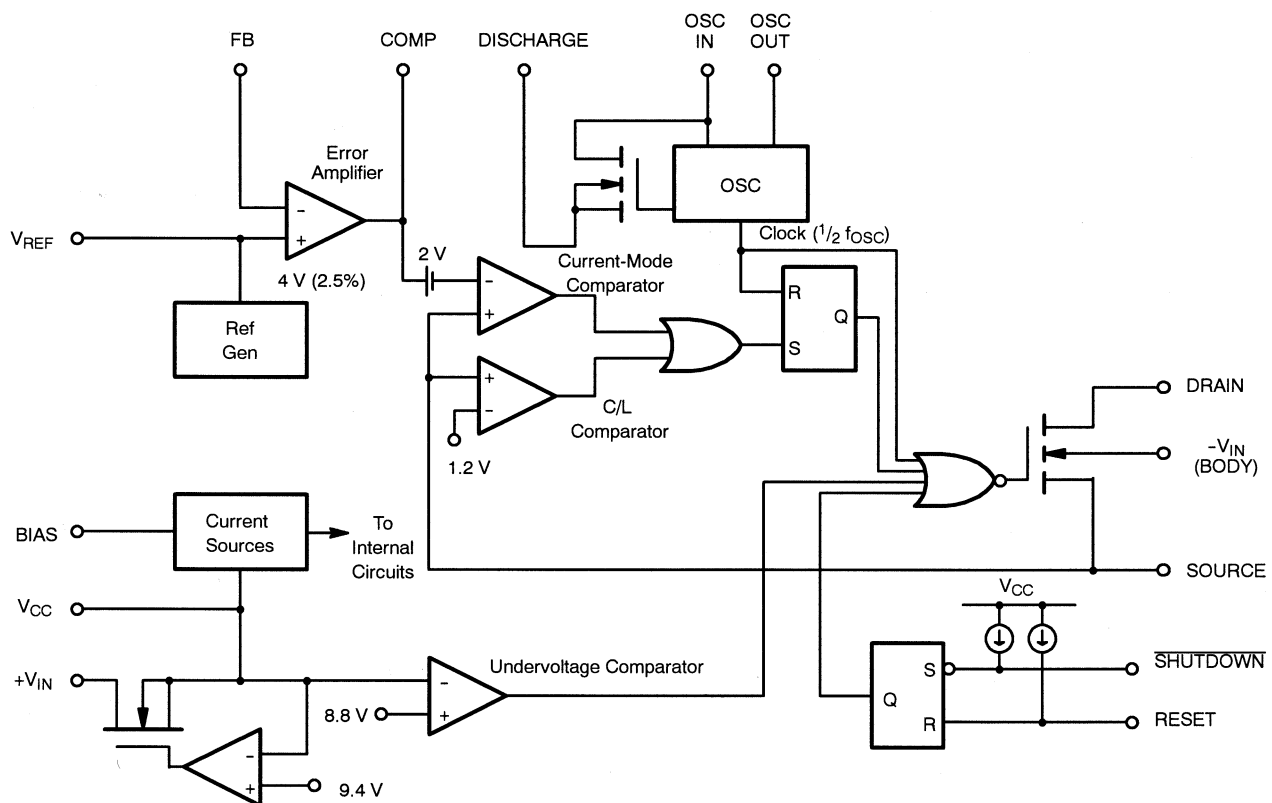
DESCRIPTION

The Si9104 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10- to 120-V unregulated dc power source.

This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9104 is available in a 16-pin wide-body SOIC and is specified over the D suffix (-40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)

V_{CC}	15 V
$+V_{IN}$	120 V
V_{DS}	200 V
I_D (Peak) (300 μ s pulse, 2% duty cycle)	2 A
I_D (rms)	250 mA
Logic Inputs (RESET, SHUTDOWN, OSC IN) ..	-0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SOURCE)	-0.3 V to 7 V
HV Pre-Regulator Input Current (continuous)	3 mA
Storage Temperature	-65 to 125°C

Operating Temperature

Junction Temperature (T_J)

Power Dissipation (Package)^a

16-Pin Plastic Wide-Body SOIC^b

Thermal Impedance (θ_{JA})

16-Pin Plastic Wide-Body SOIC

Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 7.2 mW/°C above 25°C.

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$

V_{CC}	10 V to 13.5 V
$+V_{IN}$	10 V to 120 V
f_{OSC}	40 kHz to 1 MHz

R_{OSC}

Linear Inputs

Digital Inputs

SPECIFICATIONS^a

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN} = 0$ V, $V_{CC} = 10$ V $+V_{IN} = 48$ V, $R_{BIAS} = 390$ k Ω $R_{OSC} = 330$ k Ω	Limits D Suffix -40 to 85°C				Unit
			Temp ^b	Min ^d	Typ ^c	Max ^d	
Reference							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) $R_L = 10$ M Ω	Room Full	3.92 3.85	4.0	4.08 4.15	V
Output Impedance ^e	Z_{OUT}		Room	15	30	45	k Ω
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	μ A
Temperature Stability ^e	T_{REF}		Full		0.25	1.0	mV/°C
Long Term Stability ^e		t = 1000 hrs., $T_A = 125^\circ\text{C}$	Room		5	25	mV
Oscillator							
Maximum Frequency ^e	f_{MAX}	$R_{OSC} = 0$	Room	1	3		MHz
Initial Accuracy	f_{OSC}	$R_{OSC} = 330$ k Ω ^f	Room	80	100	120	kHz
		$R_{OSC} = 150$ k Ω ^f	Room	160	200	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f = f(13.5 \text{ V}) - f(10 \text{ V}) / f(10 \text{ V})$	Room	4	10	15	%
Temperature Coefficient ^e	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, $V_{FB} = 4$ V	Room		25	500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$ (OSC Disabled)	Room		± 15	± 40	mV
Open Loop Voltage Gain ^e	A_{VOL}		Room	60	80		dB
Unity Gain Bandwidth ^e	BW		Room	0.7	1		MHz
Dynamic Output Impedance ^e	Z_{OUT}		Room		1000	2000	Ω
Output Current	I_{OUT}	Source ($V_{FB} = 3.4$ V)	Room		-2.0	-1.4	mA
		Sink ($V_{FB} = 4.5$ V)	Room	0.12	0.15		
Power Supply Rejection	PSRR	$10 \text{ V} \leq V_{CC} \leq 13.5 \text{ V}$	Room	50	70		dB

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			Temp ^b	Min ^d	Typ ^c	Max ^d	
Current Limit							
Threshold Voltage	V _{SOURCE}	R _L = 100 Ω from DRAIN to V _{CC} , V _{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output	t _d	R _L = 100 Ω from DRAIN to V _{CC} V _{SOURCE} = 1.5 V, See Figure 1.	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	+V _{IN}	I _{IN} = 10 μA	Room	120			V
Input Leakage Current	+I _{IN}	V _{CC} ≥ 10 V	Room			10	μA
Pre-Regulator Start-Up Current	I _{START}	Pulse Width ≤ 300 μs, V _{CC} = 7 V	Room	8	15		mA
V _{CC} Pre-Regulator Turn-Off Threshold Voltage	V _{REG}	I _{PRE-REGULATOR} = 10 μA	Room	7.8	9.4	9.8	V
Undervoltage Lockout	V _{UVLO}	R _L = 100 Ω from DRAIN to V _{CC} See Detailed Description	Room	7.0	8.8	9.3	
V _{REG} - V _{UVLO}	V _{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I _{CC}		Room	0.45	0.6	1.0	mA
Bias Current	I _{BIAS}		Room	10	15	20	μA
Logic							
SHUTDOWN Delay ^e	t _{SD}	V _{SOURCE} = -V _{IN} , See Figure 2.	Room		50	100	ns
SHUTDOWN Pulse Width ^e	t _{SW}	See Figure 3.	Room	50			
RESET Pulse Width ^e	t _{RW}		Room	50			
Latching Pulse Width ^e SHUTDOWN and RESET Low	t _{LW}		Room	25			
Input Low Voltage	V _{IL}		Room			2.0	V
Input High Voltage	V _{IH}		Room	8.0			
Input Current Input Voltage High	I _{IH}	V _{IN} = V _{CC}	Room		1	5	μA
Input Current Input Voltage Low	I _{IL}	V _{IN} = 0 V	Room	-35	-25		
MOSFET Switch							
Breakdown Voltage	V _{BR(DSS)}	I _{DRAIN} = 100 μA	Full	200	220		V
Drain-Source On-Resistance ^g	r _{DS(on)}	I _{DRAIN} = 100 mA	Room		3	5	Ω
Drain Off Leakage Current	I _{DSS}	V _{DRAIN} = 150 V	Room		5	10	μA
Drain Capacitance ^e	C _{DS}		Room		35		pF

Notes

- Refer to PROCESS OPTION FLOWCHART for additional information.
- Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- C_{STRAY} @ OSC IN $\leq 5\text{ pF}$.
- Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

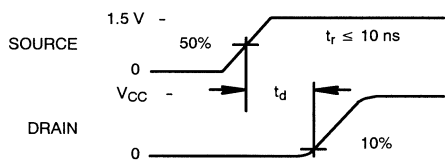


FIGURE 1.

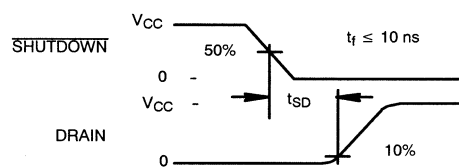


FIGURE 2.

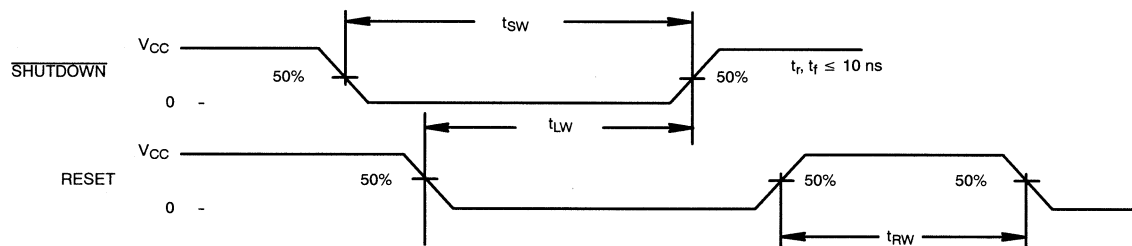


FIGURE 3.

TYPICAL CHARACTERISTICS

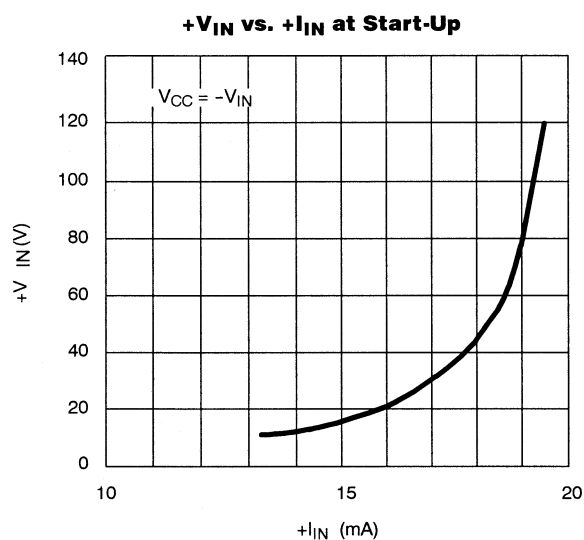


FIGURE 4.

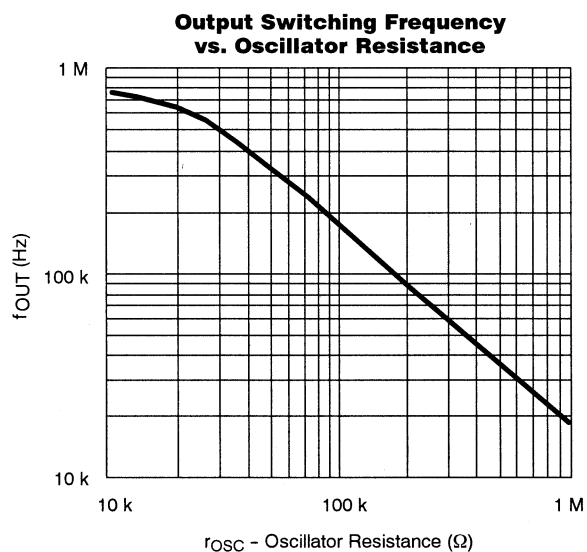
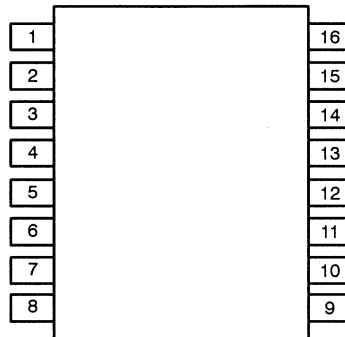


FIGURE 5.



PIN CONFIGURATIONS

SO-16
(Wide-Body)Top View
Order Number: Si9104DW

PIN DESCRIPTION			
Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
-V _{IN}	5	2	8
V _{CC}	6	4	9
OSC _{OUT}	7	5	10
OSC _{IN}	8	6	11
DISCHARGE	9	7	12
V _{REF}	10	8	14
SHUTDOWN	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
+V _{IN}	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19

