

## Features

- **Single-chip Sound Studio with Typical Applications including:**
  - Wavetable Synthesis, Serial MIDI In & Out, MPU-401 (UART)
  - Game-compatible Synthesis with Adlib Interface
  - Effects: Reverb and Chorus
  - Directsound™, Direct3Dsound™ Accelerator with Static Buffer Support
  - Interactive 3-D Positioning
  - Four-channel Surround
  - Four-band Equalizer
  - Mixer
- **High-quality Wavetable Synthesis**
  - 16-bit Samples with up to 48 kHz Sampling Rate
  - Internal Computations on 28 Bits, DAC Support up to 20 Bits
  - Alternate Loop, 24 dB Digital Filter for Each Voice
- **Professional Effects**
  - 13 Delay Lines for Resonance-free Stereo Reverb
- **Four-band Final Equalizer Allows Dramatic Sound presence Improvement**
- **Expandable**
  - Minimum System: SAM9707 + 512K Bytes of ROM + 32K x 8 RAM + DAC
  - Maximum System: SAM9707 + 64M Bytes of DRAM + Codec + DAC
- **High Performance**
  - RISC Structure for Sound Synthesis/Processing
  - CISC Structure for Host Communication and Housekeeping
  - Audio Transfer at Maximum 16-bit ISA Bus Speed
  - Audio Transfer in Burst Mode: Removes DMA-controlled Transfer Burden
- **Fully Programmable**
  - Firmware Downloaded to Memory at Power-up. Easy Software Upgrade.
  - Chip Programming Open to Third-party Software Companies
  - Powerful Programming and Debugging Tools: Algorithm Compiler, Sound Editor, Assembler and Source Debugger. Direct Development from PC Environment, No Special Emulator Required
- **Top Technology**
  - Single Low-frequency Crystal Operation and Built-in PLL Minimize RFI
  - 144-lead TQFP Space-saving Package
- **Pin and Function Compatible with SAM9407 with Additional Features for Professional Use:**
  - Up to Eight Channels of Audio-in
  - Improved Digital Mix Levels and Digital Overflow Handling
  - Improved Tuning Accuracy
  - Additional DSP Micro-instructions and Datapath for More Efficient Audio Processing Algorithm Coding

Note: Pin-to-pin replacement for SAM9407 requires 3.3V core supply  $V_{C3}$ .

## Description

The SAM9707 is a highly integrated sound processor studio that combines a specialized high-performance RISC-based digital signal processor (synthesis/DSP) and a general-purpose 16-bit CISC-based control processor on a single chip. An on-chip memory management unit (MMU) allows the synthesis/DSP and the control processor to share external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the ISA PC bus, the on-chip MIDI UART and the codec control interface, with minimum intervention from the control processor.



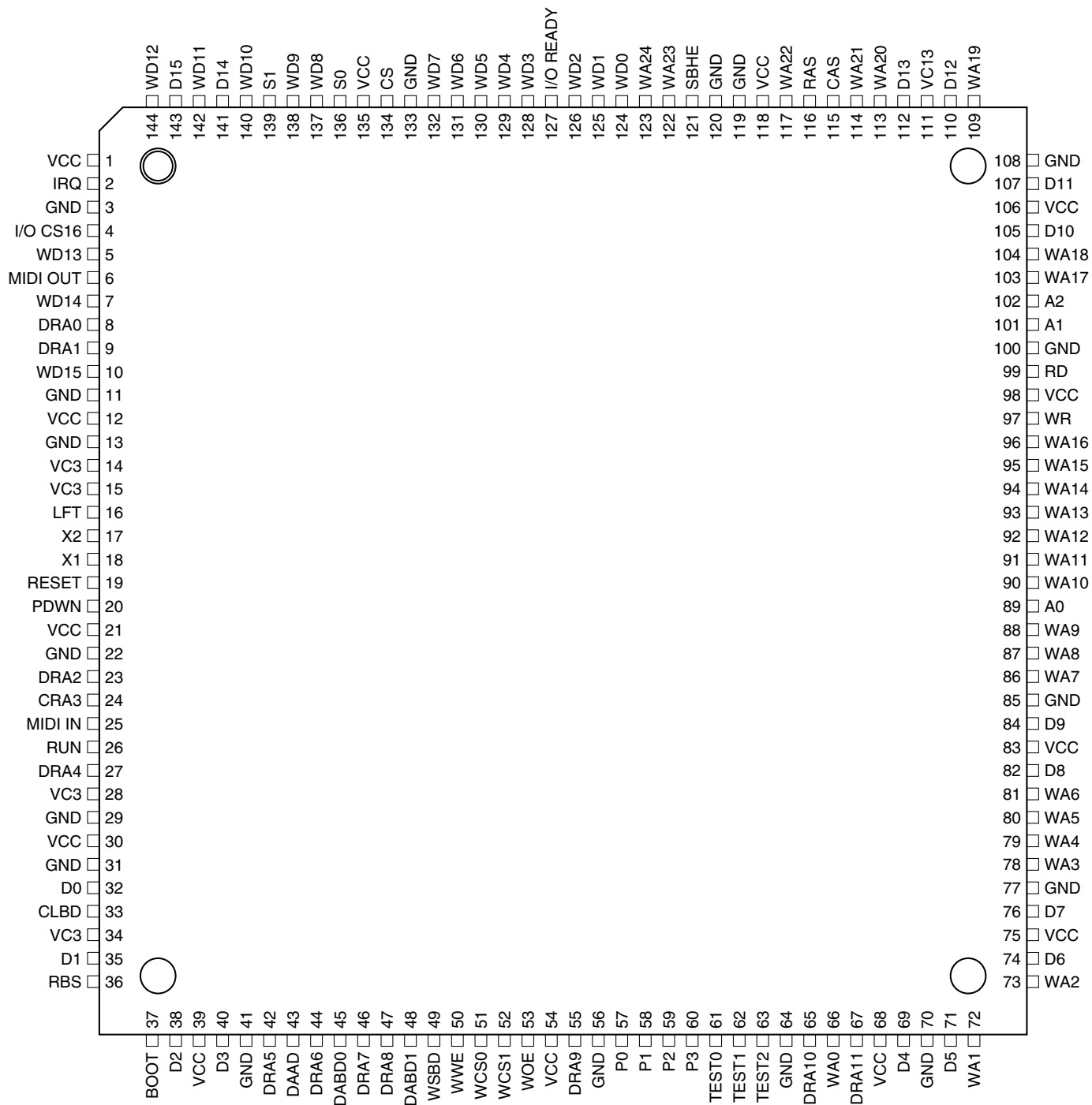
## Integrated Sound Studio

## SAM9707



## Pinout

Figure 1. SAM9707 in 144-lead TQFP Package



## Pin Description

Table 1. Pins by Function

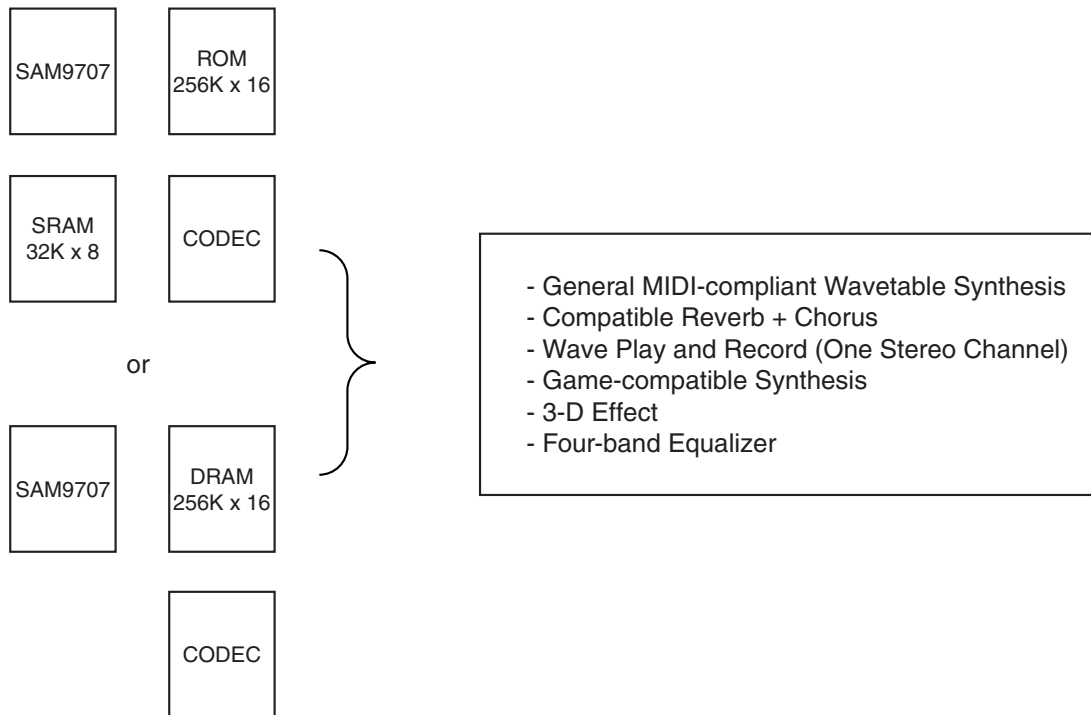
| Pin Name              | Pin Count | Type  | Function                                                                                                                                                                                                                                                                                                                                               |
|-----------------------|-----------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND                   | 17        | PWR   | Power ground – All GND pins should be returned to digital ground.                                                                                                                                                                                                                                                                                      |
| V <sub>C3</sub>       | 3         | PWR   | Core power +3.3V nominal (3V to 4.5V). All V <sub>C3</sub> pins should be returned to +3.3V.                                                                                                                                                                                                                                                           |
| V <sub>CC</sub>       | 15        | PWR   | Power +3V to +5.5V – All V <sub>CC</sub> pins should be returned to +5V (or 3.3V in case of single 3.3V supply).                                                                                                                                                                                                                                       |
| D0 - D15              | 16        | I/O   | 16-bit data bus to host processor. Has enough driving power to drive ISA PC bus directly (24 mA buffer).<br>Information on these pins is:<br>- parallel MIDI (MPU-401 type applications)<br>- Adlib control (game sound-type emulation)<br>- Down-/upload of PCM data or application programs<br>Direct ISA PC bus drive requires 5V V <sub>CC</sub> . |
| $\overline{CS}$       | 1         | IN    | Chip select from host, active low                                                                                                                                                                                                                                                                                                                      |
| $\overline{WR}$       | 1         | IN    | Write from host, active low                                                                                                                                                                                                                                                                                                                            |
| $\overline{RD}$       | 1         | IN    | Read from host, active low                                                                                                                                                                                                                                                                                                                             |
| A0 - A1               | 3         | IN    | Selects one of eight internal registers<br>- 0, 1: MPU-401 registers<br>- 2, 3: 16-bit data (burst DMA mode)<br>- 4-7: game sound registers                                                                                                                                                                                                            |
| IRQ                   | 1         | TSout | Tri-state output pin. Can be connected directly to host IRQ line (24 mA).                                                                                                                                                                                                                                                                              |
| $\overline{SBHE}$     | 1         | IN    | Bus high enable signal, active low. Normally connected to GND.                                                                                                                                                                                                                                                                                         |
| I/O READY             | 1         | OUT   | Open drain output buffer (24 mA); driven low during 16-bit burst mode transfers to synchronize PC to the SAM9707 memory.                                                                                                                                                                                                                               |
| $\overline{I/O CS16}$ | 1         | OUT   | Open drain output buffer (24 mA); driven low during 16-bit burst mode transfers.<br>Indicates to host that a 16-bit I/O is in progress.                                                                                                                                                                                                                |
| $\overline{RESET}$    | 1         | IN    | Master reset input, active low. Schmitt trigger input.                                                                                                                                                                                                                                                                                                 |
| X1, X2                | 2         |       | Crystal connection. Crystal frequency should be $f_s \times 256$ (typ 11.2896 MHz). Crystal frequency is internally multiplied by four to provide the IC master clock.<br>X1 can also be used as external clock input (3.3V input).<br>X2 CANNOT BE USED TO DRIVE EXTERNAL CIRCUITRY.                                                                  |
| DABD0 - 1             | 2         | OUT   | Two stereo serial audio data outputs (four audio channels). Each output holds 64 bits (2 x 32) of serial data per frame. Audio data has precision of up to 20 bits. DABD0 can hold additional control data (mute, A/D gain, D/A gain, etc.).                                                                                                           |
| CLBD                  | 1         | OUT   | Audio data bit clock; provides timing to DABD061.                                                                                                                                                                                                                                                                                                      |
| WSBD                  | 1         | OUT   | Audio data word select. The timing of WSBD can be selected to be I2S or Japanese compatible.                                                                                                                                                                                                                                                           |
| DAAD                  | 1         | IN    | Stereo serial audio data input                                                                                                                                                                                                                                                                                                                         |
| MIDI IN               | 1         | IN    | Serial MIDI IN input                                                                                                                                                                                                                                                                                                                                   |
| MIDI OUT              | 1         | OUT   | Serial MIDI OUT output                                                                                                                                                                                                                                                                                                                                 |

**Table 1.** Pins by Function (Continued)

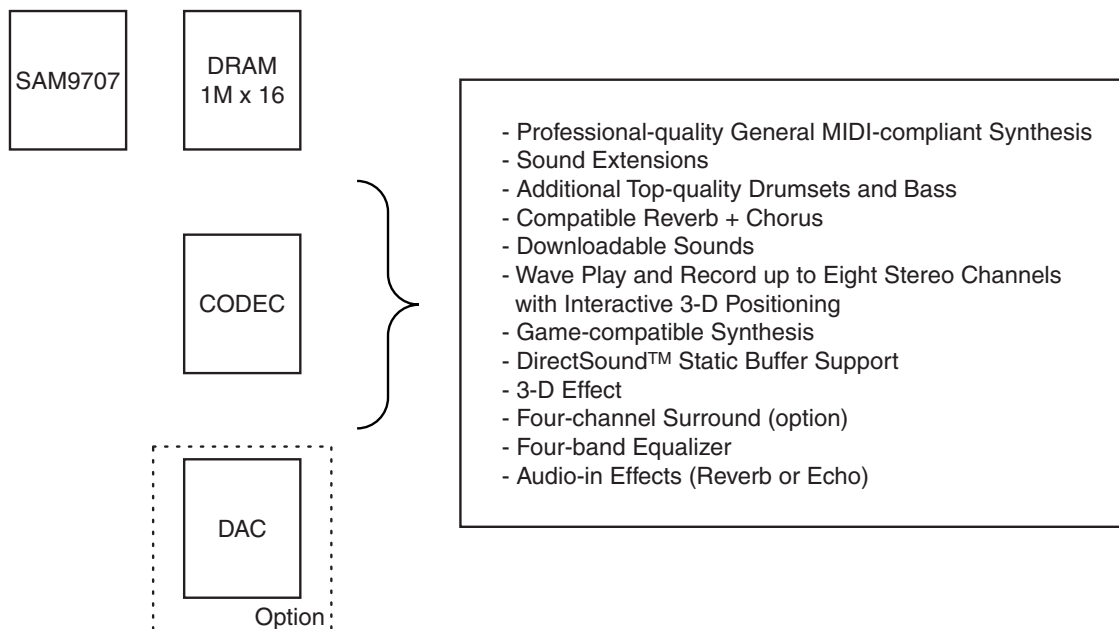
| Pin Name          | Pin Count | Type | Function                                                                                                                                                                         |
|-------------------|-----------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WA0 - 24          | 25        | OUT  | External memory address (ROM/SRAM). Up to 32M words (64M 8-bit samples).                                                                                                         |
| WD0 - 15          | 16        | I/O  | PCM ROM/SRAM/DRAM data                                                                                                                                                           |
| RBS               | 1         | OUT  | SRAM byte select: Should be connected to the lower RAM address when 8-bit wide SRAM is used. The type of RAM (16 bits/8 bits) can be selected by program.                        |
| $\overline{WCS0}$ | 1         | OUT  | PCM ROM chip select, active low.                                                                                                                                                 |
| $\overline{WCS1}$ | 1         | OUT  | SRAM chip select, active low.                                                                                                                                                    |
| $\overline{WWE}$  | 1         | OUT  | SRAM/DRAM write enable, active low. Timing compatible with SIMM DRAM early write feature.                                                                                        |
| $\overline{WOE}$  | 1         | OUT  | PCM ROM/SRAM output enable, active low.                                                                                                                                          |
| BOOT              | 1         | IN   | Active high, specifies that built-in CPU bootstrap should be used at power-up (case of DRAM connection only).                                                                    |
| DRA0 - 11         | 12        | OUT  | Multiplex DRAM address: 9-, 10-, 11-, 12-bit multiplex addressing can be used (from 256K x 16- to 16M x 16-type configurations).                                                 |
| $\overline{RAS}$  | 1         | OUT  | DRAM row address strobe                                                                                                                                                          |
| $\overline{CAS}$  | 1         | OUT  | DRAM column address strobe                                                                                                                                                       |
| P0 - P3           | 4         | I/O  | General-purpose configurable I/O pins. P1 to P3 can be configured as three additional stereo serial audio data inputs, providing the DAAD with up to eight channels of audio-in. |
| S0 - S1           | 2         | OUT  | Indicates type of external memory cycle.<br>S1S0 = 01: Idle or refresh, 00: Synthesis access, 10: Instruction fetch, 11: Processor read/write                                    |
| RUN               | 1         | OUT  | High when the synthesis is initialized. Can be used as $\overline{RESET}$ for an external device (CODEC).                                                                        |
| LFT               | 1         | ANA  | PLL low pass filter. Should be connected to an external RC network test pin; should be returned to GND.                                                                          |
| TEST0 - 2         | 3         | IN   | Test pins; should be returned to GND.                                                                                                                                            |
| $\overline{PDWN}$ | 1         | IN   | Power-down, active low.                                                                                                                                                          |

## Typical Designs

**Figure 2. Lowest Cost Design Architecture**

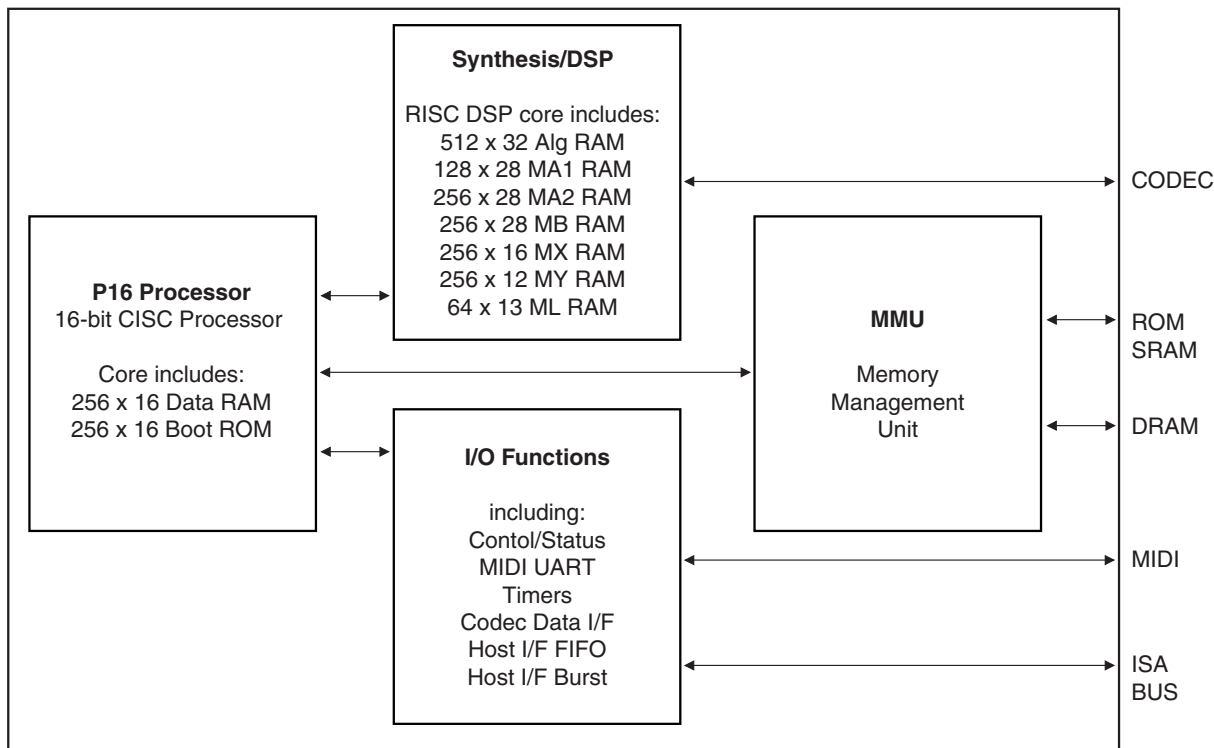


**Figure 3. Typical Design Architecture**



## Functional Description

Figure 4. IC Architecture



### Synthesis/DSP Engine

The synthesis/DSP engine operates on a frame-timing basis with the frame subdivided into 64 process slots. Each process is itself divided into 16 micro-instructions known as “algorithms”. Up to 32 synthesis/DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications. The synthesis/DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24 dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical multimedia application will use half the capacity of the synthesis/DSP engine for synthesis, thus providing state-of-the-art 32-voice wavetable polyphony. The remaining processing power will be used for typical functions such as reverberation, chorus, direct sound, surround effect, equalizer, etc.

Frequently accessed synthesis/DSP parameter data are stored into five banks of on-chip RAM memory. Sample data or delay lines, which are accessed relatively infrequently, are stored in external ROM, SRAM or DRAM memory. The combination of localized micro-program

memory and localized parameter data allows micro-instructions to execute in 20 ns (50 MIPS). Separate buses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to six simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 300 million operations per second (MOPS).

### P16 Control Processor and I/O Functions

The P16 control processor is a general-purpose 16-bit CISC processor core that runs from external memory. A Boot/Macro ROM is included on-chip to accelerate commonly executed routines and to allow the use of RAM-only devices for the external memory. The P16 also includes 256 words of local RAM data memory.

The P16 control processor writes to the parameter RAM blocks within the synthesis/DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the PC ISA interface and then controls the synthesis/DSP by writing into the parameter RAM

banks in the DSP core. Slowly changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the ISA PC interface, through specialized “intelligent” peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

The ISA PC interface is implemented using three address lines (A2, A1, A0), a chip select signal, read-and-write strobes from the host and a 16-bit data bus (D0 - D15).

The data bus can drive the PC bus directly (24 mA buffers). An external decoder (PAL) or plug & play IC is required to map the 12-bit I/O addresses and AEN from the PC into the three address lines and chip select from the SAM9707.

The ISA PC interface supports a byte-wide primary I/O interface, a byte-wide auxiliary interface and a 16-bit port dedicated to burst transfers.

The primary I/O interface is normally used to implement a Roland MPU-401 UART-mode compatible interface. It is specified by address A2A1A0 = 00X, address 000 being

the data register and address 001 being the status/control registers. Besides the standard two status bits of the MPU-401, two additional bits are provided to expand the MPU-401 protocol.

The auxiliary interface is allocated the address range A2A1A0 = 1XX. It is normally used to implement a game-compatible interface.

Address A2A1A0 = 010 specifies a 16-bit I/O port. It is mainly used for burst audio transfers to/from the PC using very efficient PC instructions such as REP OUTSW or REP INSW, which operate at maximum ISA bus bandwidth. This port may also be used for fast program or sound bank uploads.

### **Memory Management Unit (MMU)**

The Memory Management Unit (MMU) block allows external ROM and/or RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single device (i.e., DRAM) to serve as sample memory storage/delay lines for the synthesis/DSP and as program storage/data memory for the P16 control processor.

## Timings

All timing conditions:  $V_{CC} = 5V$ ,  $V_{C3} = 3.3V$ ,  $T_A = 25^\circ C$ , signals I/O READY,  $\overline{I/O\ CS16}$ , D0 - D15 with  $220\Omega$  pull-up, 30 pF capacitance, signal IRQ with  $470\Omega$  pull-down, 30 pF capacitance, all other outputs except X2 and LFT load capacitance = 30 pF.

All timings refer to  $t_{CK}$ , which is the internal master clock period.

The internal master clock frequency is four times the frequency at pin X1. Therefore,  $t_{CK} = t_{XTAL}/4$ .

The sampling rate is given by  $1/(t_{CK} \cdot 1024)$ . The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 kHz sampling rate).

## Crystal Frequency Selection Considerations

There is a trade-off between the crystal frequency and the support of widely available external DRAM/ROM components. Table 2 allows selection of the best fit for a given application.

**Table 2.** Crystal Frequency Selection Considerations

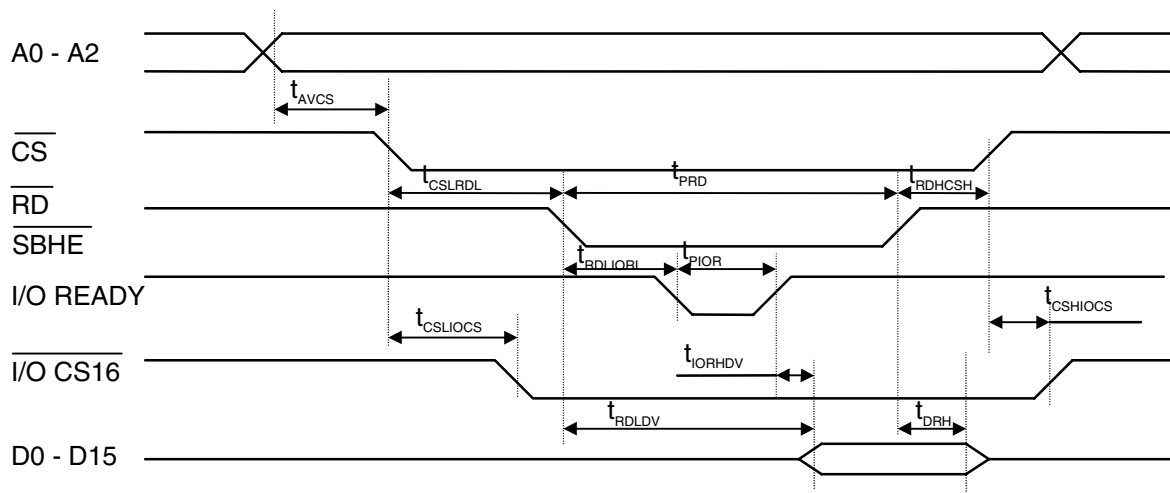
| Sample Rate (kHz) | Crystal (MHz) | $t_{CK}$ (ns) | ROM 1A (ns) | DRAM $t_{RAC}$ (ns) | DRAM $t_{RC}$ (ns) | Comment                         |
|-------------------|---------------|---------------|-------------|---------------------|--------------------|---------------------------------|
| 48                | 12.288        | 20.35         | 92          | 72                  | 92                 | Maximum Frequency               |
| 44.1              | 11.2896       | 22.14         | 101         | 80                  | 101                | Recommended for Current Designs |
| 37.5              | 9.60          | 26.04         | 120         | 95                  | 120                |                                 |
| 31.25             | 8.00          | 31.25         | 146         | 116                 | 146                |                                 |

Using a 11.2896 MHz crystal allows the use of widely available DRAMs (-6 type) with a cycle time ( $t_{RC}$ ) of 100 ns and an  $\overline{RAS}$  access time of 60 ns, as well as widely available

ROMs with 100 ns access time, while providing state-of-the-art 44.1 kHz sampling rate.

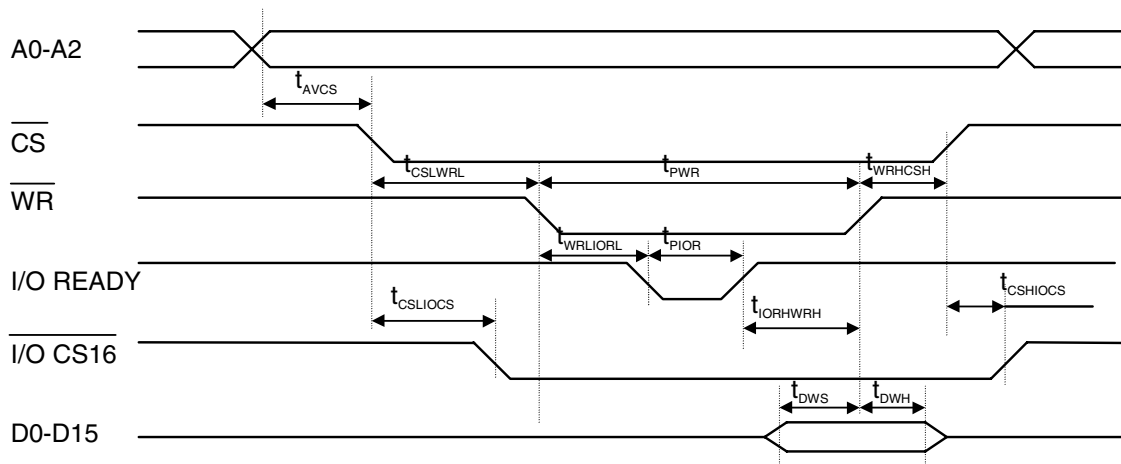
## PC Host Interface Timing

**Figure 5.** PC Host Interface Timing Diagram



Note: D8 - 15 valid only if A2A1 = 10 and  $\overline{SBHE} = 0$ .

**Figure 6. PC Host Interface Write Cycle**



Note: D8 - D15 valid only if A2A1 = 10.

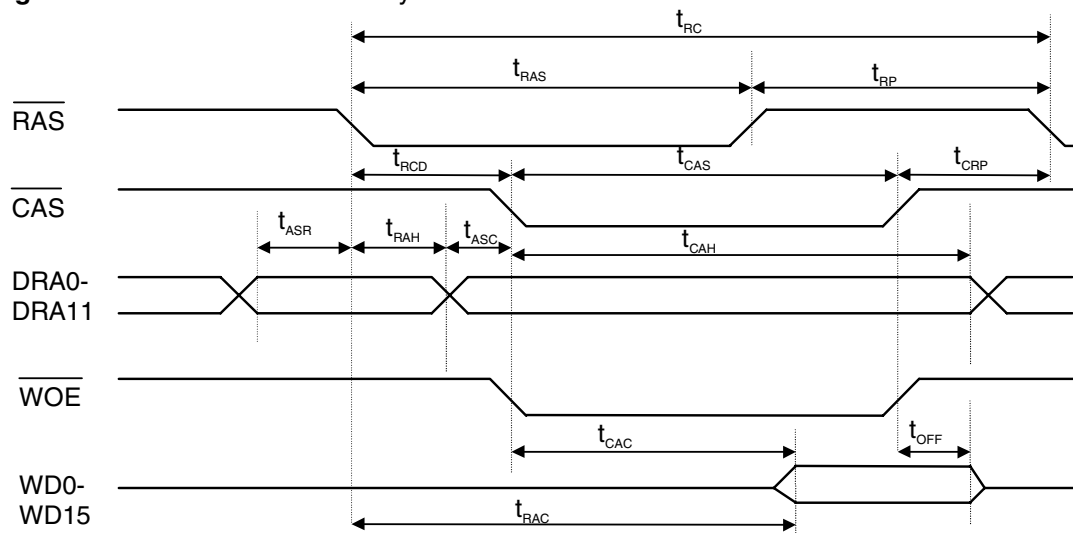
**Table 3. PC Host Interface Timing Parameters**

| Symbol        | Parameter                                                                  | Min | Typ | Max | Unit     |
|---------------|----------------------------------------------------------------------------|-----|-----|-----|----------|
| $t_{AVCS}$    | Address Valid to Chip Select Low                                           | 0   |     |     | ns       |
| $t_{CSLRDL}$  | Chip Select Low to $\overline{RD}$ or $\overline{SBHE}$ Low <sup>(1)</sup> | 5   |     |     | ns       |
| $t_{RDHCSH}$  | $\overline{RD}$ or $\overline{SBHE}$ High to $\overline{CS}$ High          | 5   |     |     | ns       |
| $t_{PRD}$     | $\overline{RD}$ or $\overline{SBHE}$ Pulse Width                           | 50  |     |     | ns       |
| $t_{RDLDV}$   | Data Out Valid from $\overline{RD}$ or $\overline{SBHE}$ <sup>(2)</sup>    |     |     | 20  | ns       |
| $t_{DRH}$     | Data Out Hold from $\overline{RD}$ or $\overline{SBHE}$                    | 5   |     | 10  | ns       |
| $t_{RDLIORL}$ | I/O Ready Low from $\overline{RD}$ or $\overline{SBHE}$ <sup>(3)</sup>     | 0   |     | 10  | ns       |
| $t_{PIOR}$    | I/O Ready Pulse Width <sup>(3)</sup>                                       |     |     | 128 | $t_{CK}$ |
| $t_{IORHDV}$  | I/O Ready Rising to Data Out Valid <sup>(3)</sup>                          |     |     | 0   | ns       |
| $t_{CSLIOCS}$ | $\overline{I/O\ CS16}$ Low from $\overline{CS}$ Low <sup>(4)</sup>         | 0   |     | 20  | ns       |
| $t_{CSHIOCS}$ | $\overline{I/O\ CS16}$ High from $\overline{CS}$ High <sup>(4)</sup>       | 0   |     | 20  | ns       |
| $t_{CSLRWRL}$ | Chip Select Low to $\overline{WR}$ Low <sup>(3)</sup>                      | 5   |     |     | ns       |
| $t_{WRHCSH}$  | $\overline{WR}$ High to $\overline{CS}$ High                               | 5   |     |     | ns       |
| $t_{PWR}$     | $\overline{WR}$ Pulse Width                                                | 50  |     |     |          |
| $t_{WRLIORL}$ | I/O Ready Low from $\overline{WR}$ Low <sup>(3)</sup>                      |     |     | 128 | $t_{CK}$ |
| $t_{IORHWRH}$ | I/O Ready High to $\overline{WR}$ High <sup>(3)</sup>                      | 5   |     |     | ns       |
| $t_{DWS}$     | Write Data Setup Time                                                      | 10  |     |     | ns       |
| $t_{DWH}$     | Write Data Hold Time                                                       | 0   |     |     | ns       |

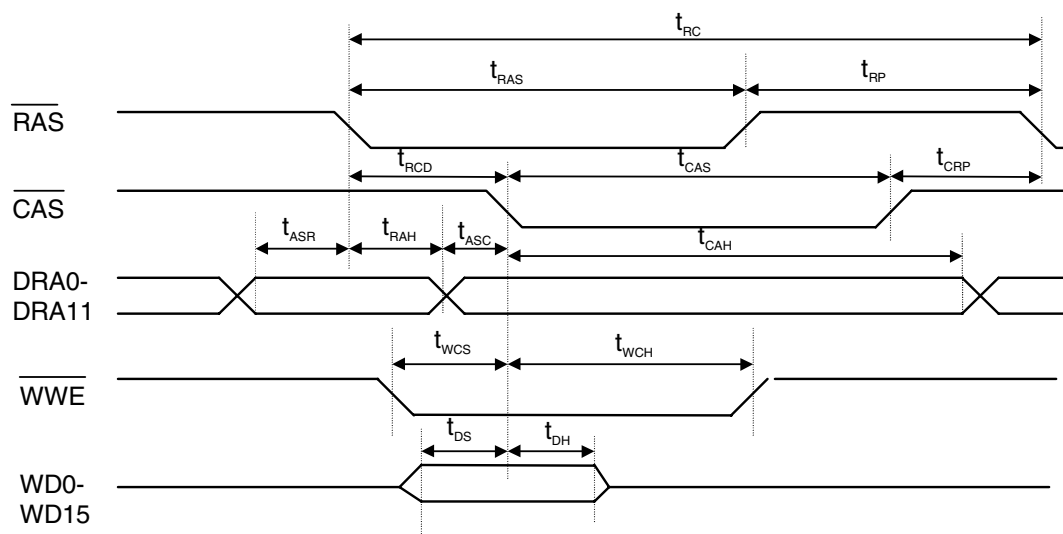
- Notes:
1.  $\overline{SBHE}$  is normally not used (grounded).
  2. When data is already loaded into internal SAM9707 output register. In this case I/O READY will stay high during the read cycle.
  3. I/O READY will go low only if the data is not ready to be loaded into/read from internal SAM9707 register. 128  $t_{CK}$  corresponds to a single worst-case situation. At  $f_{CK} = 11.2896$  MHz, I/O READY is likely never to go low when using standard ISA bus timing.
  4.  $\overline{I/O\ CS16}$  is asserted low by SAM9707 if A2A1 = 10 to indicate fast 16-bit ISA bus transfer to the PC.

## External DRAM Timing

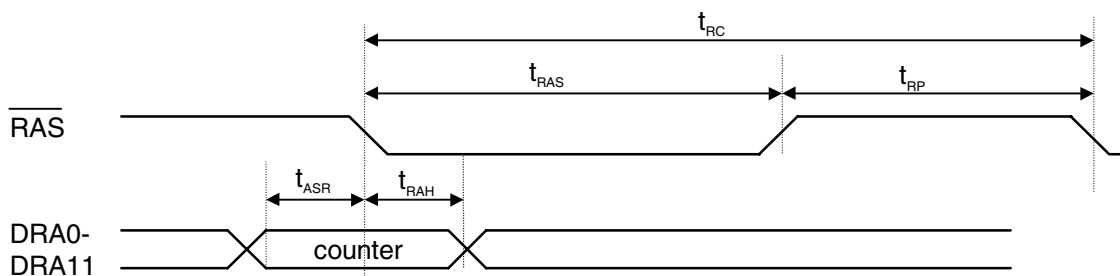
**Figure 7.** External DRAM Read Cycle



**Figure 8.** External DRAM Write Cycle (Early Write)



**Figure 9.** External DRAM Refresh Cycle ( $\overline{RAS}$  Only)



**Table 4.** External DRAM Timing Parameters

| Symbol    | Parameter                                           | Min                   | Typ                 | Max                   | Unit |
|-----------|-----------------------------------------------------|-----------------------|---------------------|-----------------------|------|
| $t_{RC}$  | Read/Write/Refresh Cycle                            | $5 \times t_{CK} - 5$ |                     | $6 \times t_{CK} + 5$ | ns   |
| $t_{RAC}$ | Access Time from $\overline{RAS}$                   |                       |                     | $4 \times t_{CK} - 5$ | ns   |
| $t_{CAC}$ | Access Time from $\overline{CAS}$                   |                       |                     | $4 \times t_{CK} - 5$ | ns   |
| $t_{OFF}$ | $\overline{CAS}$ High to Output High-Z              |                       |                     | $2 \times t_{CK} - 5$ | ns   |
| $t_{RP}$  | $\overline{RAS}$ Precharge Time                     | $2 \times t_{CK}$     |                     |                       | ns   |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width                        | $3 \times t_{CK} - 5$ |                     |                       | ns   |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width                        | $3 \times t_{CK} - 5$ |                     |                       | ns   |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time     | $t_{CK} - 5$          |                     | $t_{CK} + 5$          | ns   |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CK} - 5$          |                     |                       | ns   |
| $t_{ASR}$ | Row Address Setup Time                              | $t_{CK} - 5$          |                     |                       | ns   |
| $t_{RAH}$ | Row Address Hold Time                               | $t_{CK}/2$            |                     |                       | ns   |
| $t_{ASC}$ | Column Address Setup Time                           | $t_{CK}/2 - 5$        |                     |                       | ns   |
| $t_{CAH}$ | Column Address Hold Time                            | $3 \times t_{CK}$     |                     |                       | ns   |
| $t_{WCS}$ | Write Command Setup Time                            |                       | $t_{CK}$            |                       | ns   |
| $t_{WCH}$ | Write Command Hold Time                             |                       | $4 \times t_{CK}$   |                       | ns   |
| $t_{DS}$  | Write Data Setup Time                               |                       | $t_{CK}$            |                       | ns   |
| $t_{DH}$  | Write Data Hold Time                                |                       | $3 \times t_{CK}$   |                       | ns   |
| —         | Refresh Counter Average Period (12-bit Counter)     |                       | $512 \times t_{CK}$ |                       | ns   |

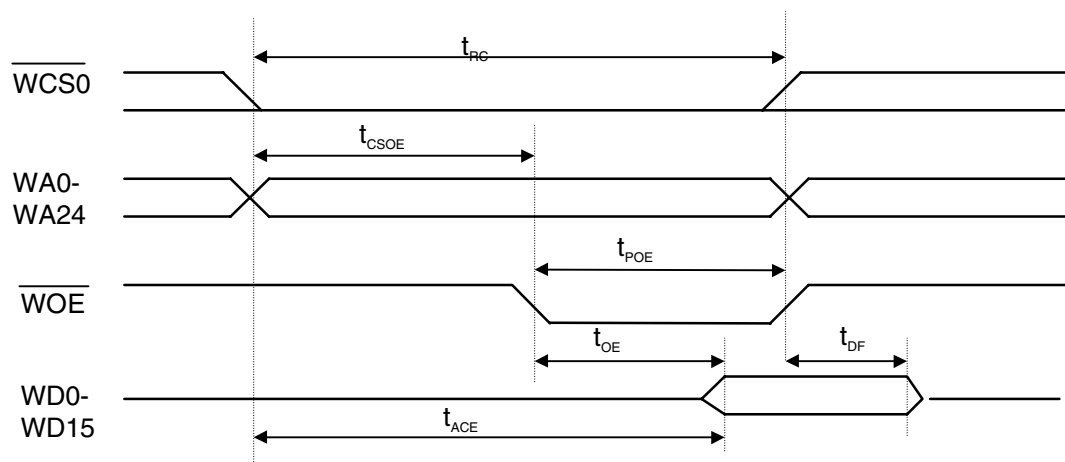
- Notes:
1. The multiplexed CAS, RAS addressing can support memory DRAM chips up to 16 Mb as long as the number of row address lines and column address lines are identical. For example, device type 416C1200 is supported because it is a 1M x 16 organization with 10-bit row and 10-bit column. Device type 416C1000 is not supported because it is a 1M x 16 organization with 12-bit row and 8-bit column.
  2. The signal  $\overline{WOE}$  is normally not used for DRAM connection. It is represented only for reference purposes.
  3. As  $\overline{RAS}$  only counter refresh method is employed, several banks of DRAMs can be connected using simple external  $\overline{CAS}$  decoding. Linear address lines (WAX) can be used to select between DRAM banks. For example, a 1M x 32 SIMM module may be connected as two 1M x 16 banks, with  $\overline{CAS0}$  and  $\overline{CAS1}$  selections issued from  $\overline{CAS}$  and WA20.
  4. During a whole DRAM cycle (from  $\overline{RAS}$  low to  $\overline{CAS}$  rising),  $\overline{WCS0}$  is asserted low.
  5. The equivalence between multiplexed DRAM address lines (DRA0 to DRA11) and the corresponding linear addressing (WA0 to WA23) is as follows:

|                       | DRA11 | DRA10 | DRA9 | DRA8 | DRA7 | DRA6 | DRA5 | DRA4 | DRA3 | DRA2 | DRA1 | DRA0 |
|-----------------------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| $\overline{RAS}$ Time | WA22  | WA20  | WA18 | WA8  | WA7  | WA6  | WA5  | WA4  | WA3  | WA2  | WA1  | WA0  |
| $\overline{CAS}$ Time | WA23  | WA21  | WA19 | WA17 | WA16 | WA15 | WA14 | WA13 | WA12 | WA11 | WA10 | WA9  |

6. To save DRAM power consumption,  $\overline{CAS}$  and  $\overline{RAS}$  are cycled only when necessary. Therefore, depending on firmware loaded, total board power consumption may increase with synthesis processing traffic.

## External ROM Cycle Timing

**Figure 10.** External ROM Read Cycle

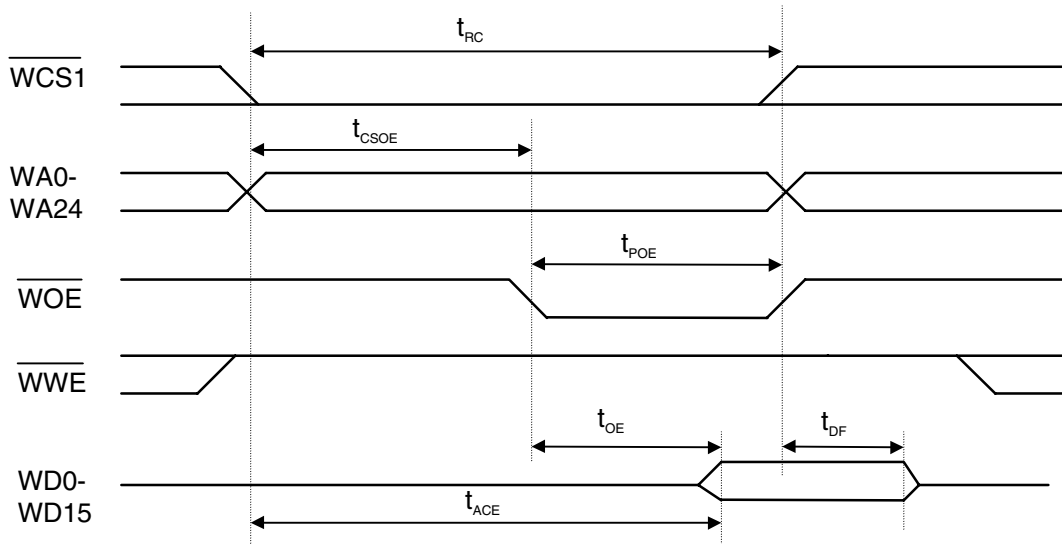


**Table 5.** External ROM Cycle Timing Parameters

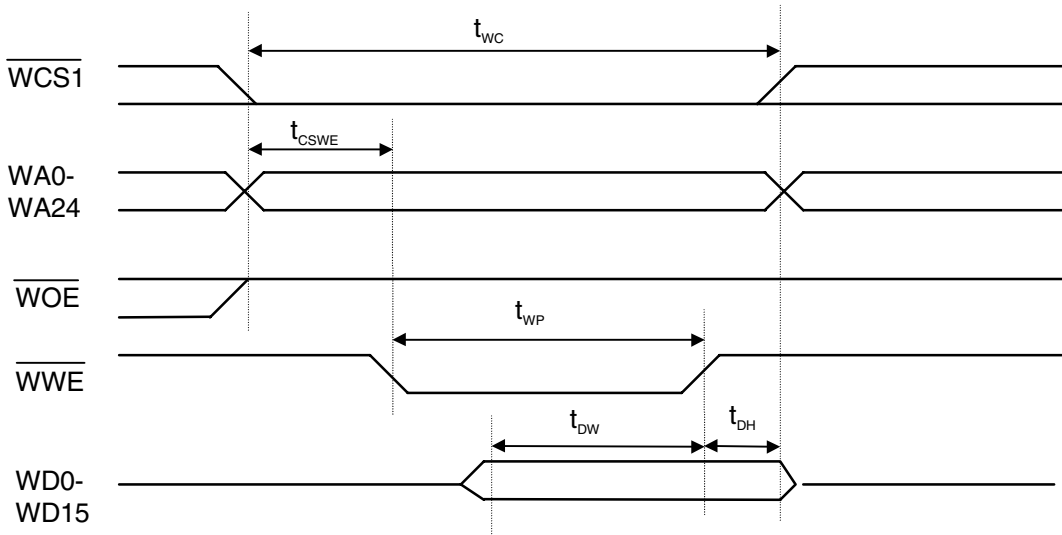
| Symbol     | Parameter                                                 | Min                   | Typ               | Max                   | Unit |
|------------|-----------------------------------------------------------|-----------------------|-------------------|-----------------------|------|
| $t_{RC}$   | Read Cycle Time                                           | $5 \times t_{CK}$     |                   | $6 \times t_{CK}$     | ns   |
| $t_{CSOE}$ | Chip Select Low/Address Valid to $\overline{WOE}$ Low     | $2 \times t_{CK} - 5$ |                   | $3 \times t_{CK} + 5$ | ns   |
| $t_{POE}$  | Output Enable Pulse Width                                 |                       | $3 \times t_{CK}$ |                       | ns   |
| $t_{ACE}$  | Chip Select/Address Access Time                           | $5 \times t_{CK} - 5$ |                   |                       | ns   |
| $t_{OE}$   | Output Enable Access Time                                 | $3 \times t_{CK} - 5$ |                   |                       | ns   |
| $t_{DF}$   | Chip Select or $\overline{WOE}$ High to Input Data High-Z | 0                     |                   | $2 \times t_{CK} - 5$ | ns   |

## External RAM Timing

**Figure 11.** 16-bit SRAM Read Cycle



**Figure 12.** 16-bit SRAM Write Cycle



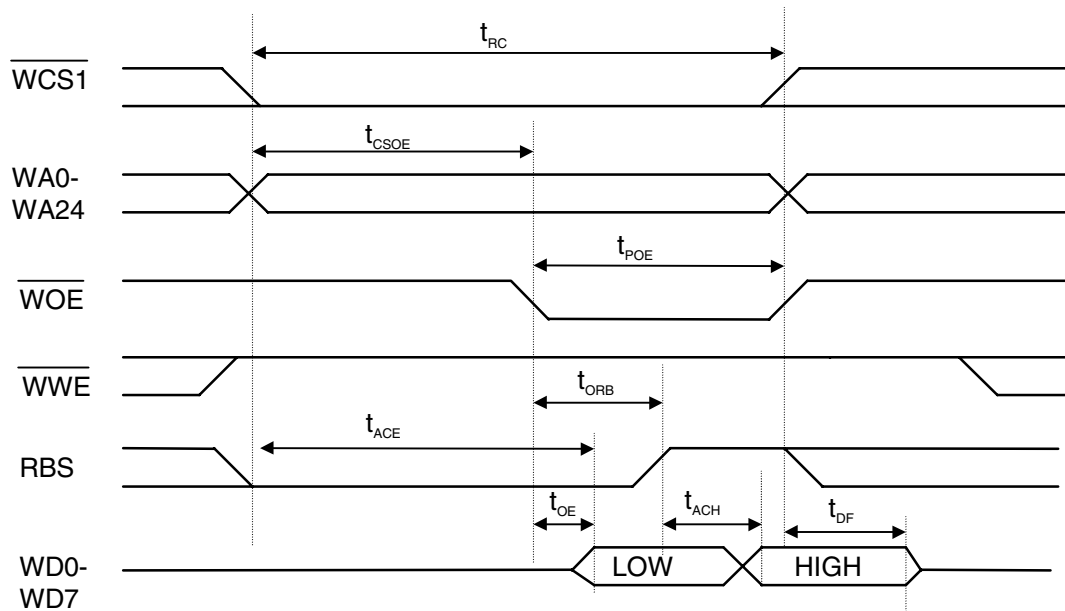
**Table 6.** 16-bit SRAM Timing Parameters

| Symbol     | Parameter                                             | Min                   | Typ               | Max                   | Unit |
|------------|-------------------------------------------------------|-----------------------|-------------------|-----------------------|------|
| $t_{RC}$   | Read Cycle Time                                       | $5 \times t_{CK}$     |                   | $6 \times t_{CK}$     | ns   |
| $t_{CSOE}$ | Chip Select Low/Address Valid to $\overline{WOE}$ Low | $2 \times t_{CK} - 5$ |                   | $3 \times t_{CK} + 5$ | ns   |
| $t_{POE}$  | Output Enable Pulse Width                             |                       | $3 \times t_{CK}$ |                       | ns   |
| $t_{ACE}$  | Chip Select/Address Access Time                       | $5 \times t_{CK} - 5$ |                   |                       | ns   |

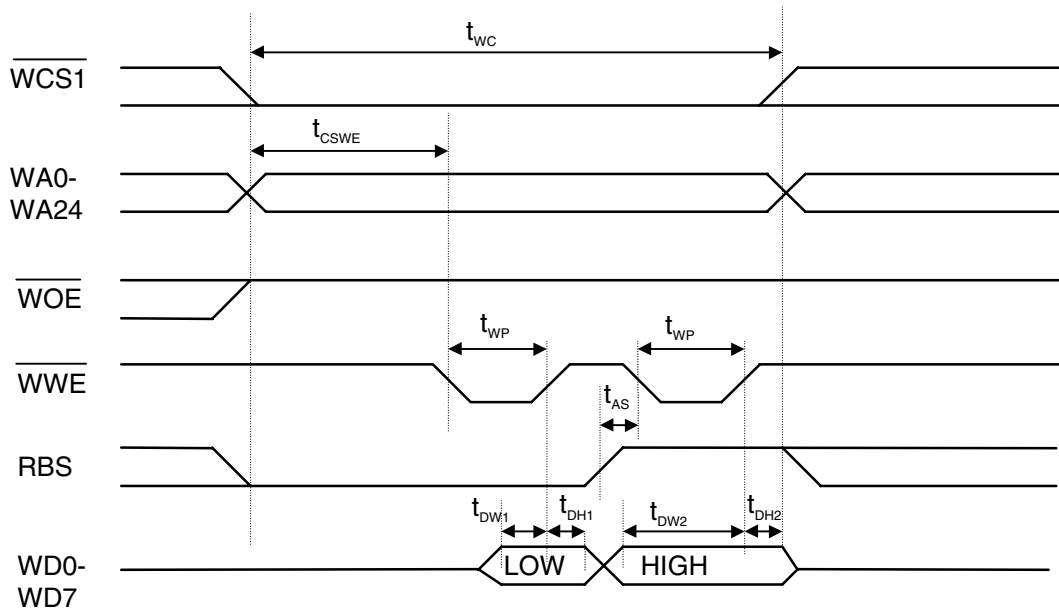
**Table 6.** 16-bit SRAM Timing Parameters

| Symbol     | Parameter                                                            | Min                    | Typ               | Max                   | Unit |
|------------|----------------------------------------------------------------------|------------------------|-------------------|-----------------------|------|
| $t_{OE}$   | Output Enable Access Time                                            | $3 \times t_{CK} - 5$  |                   |                       | ns   |
| $t_{DF}$   | Chip Select or $\overline{WOE}$ High to Input Data High-Z            | 0                      |                   | $2 \times t_{CK} - 5$ | ns   |
| $t_{WC}$   | Write Cycle Time                                                     | $5 \times t_{CK}$      |                   | $6 \times t_{CK}$     | ns   |
| $t_{CSWE}$ | Write Enable Low from $\overline{CS}$ or Address or $\overline{WOE}$ | $2 \times t_{CK} - 10$ |                   |                       | ns   |
| $t_{WP}$   | Write Pulse Width                                                    |                        | $4 \times t_{CK}$ |                       | ns   |
| $t_{DW}$   | Data Out Setup Time                                                  | $4 \times t_{CK} - 10$ |                   |                       | ns   |
| $t_{DH}$   | Data Out Hold Time                                                   | 10                     |                   |                       | ns   |

**Figure 13.** 8-bit SRAM Read Cycle



**Figure 14. 8-bit SRAM Write Cycle**

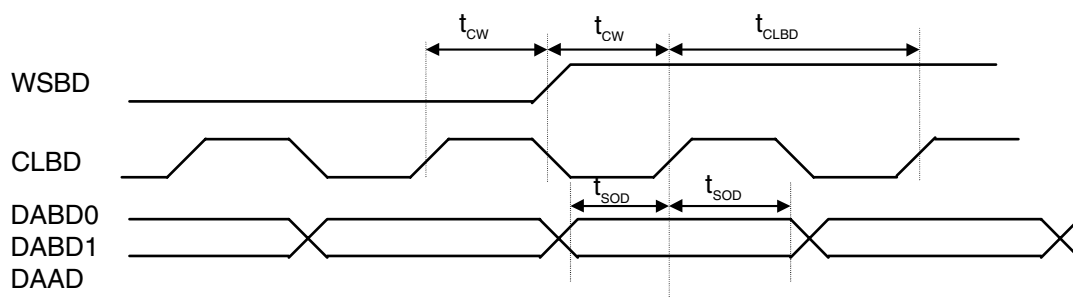


**Table 7. 8-bit SRAM Timing Parameters**

| Symbol     | Parameter                                                                      | Min                      | Typ               | Max                   | Unit |
|------------|--------------------------------------------------------------------------------|--------------------------|-------------------|-----------------------|------|
| $t_{RC}$   | Word Read Cycle Time                                                           | $5 \times t_{CK}$        |                   | $6 \times t_{CK}$     | ns   |
| $t_{CSOE}$ | Chip Select Low/Address Valid to $\overline{WOE}$ Low                          | $2 \times t_{CK} - 5$    |                   | $3 \times t_{CK} + 5$ | ns   |
| $t_{POE}$  | Output Enable Pulse Width                                                      |                          | $3 \times t_{CK}$ |                       | ns   |
| $t_{ACE}$  | Chip Select/Address Low Byte Access Time                                       | $3 \times t_{CK} - 5$    |                   |                       | ns   |
| $t_{OE}$   | Output Enable Low Byte Access Time                                             | $t_{CK} - 5$             |                   |                       | ns   |
| $t_{ORB}$  | Output Enable Low to Byte Select High                                          |                          | $t_{CK}$          |                       | ns   |
| $t_{ACH}$  | Byte Select High Byte Access Time                                              | $2 \times t_{CK} - 5$    |                   |                       | ns   |
| $t_{DF}$   | Chip Select or $\overline{WOE}$ High to Input Data High-Z                      | 0                        |                   | $2 \times t_{CK} - 5$ | ns   |
| $t_{WC}$   | Word Write Cycle Time                                                          | $5 \times t_{CK}$        |                   | $6 \times t_{CK}$     | ns   |
| $t_{CSWE}$ | First $\overline{WWE}$ Low from $\overline{CS}$ or Address or $\overline{WOE}$ | $2 \times t_{CK} - 10$   |                   |                       | ns   |
| $t_{WP}$   | Write (Low and High Byte) Pulse Width                                          | $1.5 \times t_{CK} - 5$  |                   |                       | ns   |
| $t_{DW1}$  | Data Out Low Byte Setup Time                                                   | $1.5 \times t_{CK} - 10$ |                   |                       | ns   |
| $t_{DH1}$  | Data Out Low Byte Hold Time                                                    | $0.5 \times t_{CK} + 10$ |                   |                       | ns   |
| $t_{AS}$   | RBS High to Second Write Pulse                                                 | $0.5 \times t_{CK} - 5$  |                   |                       | ns   |
| $t_{DW2}$  | Data Out High Byte Setup Time                                                  | $2 \times t_{CK} - 10$   |                   |                       | ns   |
| $t_{DH2}$  | Data Out High Byte Hold Time                                                   | 10                       |                   |                       | ns   |

## Digital Audio Timing

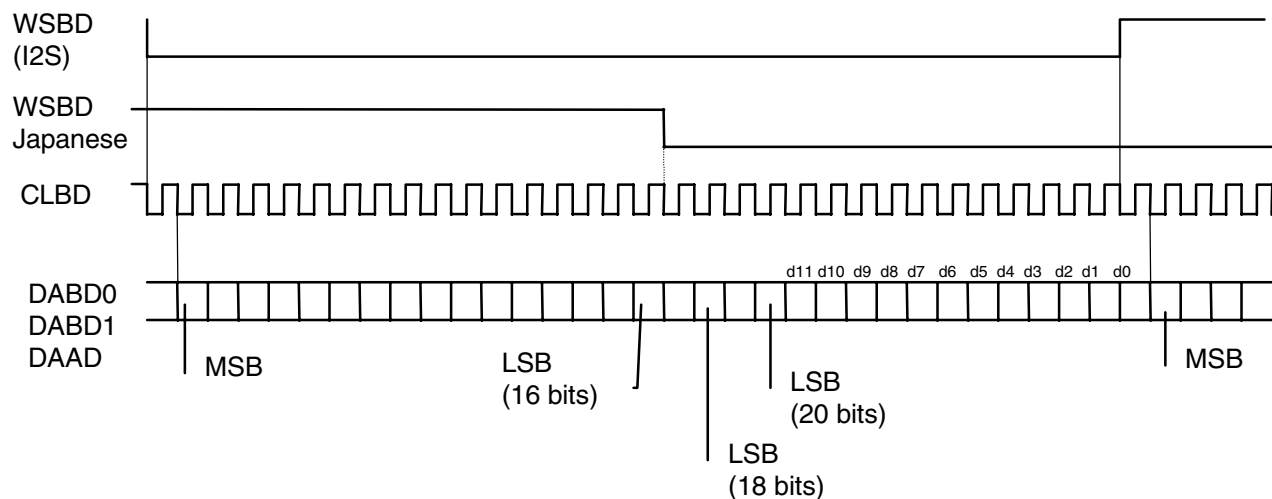
**Figure 15.** Digital Audio Timing



**Table 8.** Digital Audio Timing Parameters

| Symbol     | Parameter                           | Min                    | Typ                | Max | Unit |
|------------|-------------------------------------|------------------------|--------------------|-----|------|
| $t_{WC}$   | CLBD Rising to WSBD Change          | $8 \times t_{CK} - 10$ |                    |     | ns   |
| $t_{SOD}$  | DABD Valid before/after CLBD Rising | $8 \times t_{CK} - 10$ |                    |     | ns   |
| $t_{CLBD}$ | CLBD Cycle Time                     |                        | $16 \times t_{CK}$ |     | ns   |

**Figure 16.** Digital Audio Frame Format



- Notes:
- Selection between I2S and Japanese format is a firmware option.
  - DAAD is 16 bits only.
  - When connected with codecs such as CS4216 or CS4218, D0 - D11 can be used to hold independent auxiliary information on left and right words. Refer to corresponding codec datasheets for details.

## Reset and Power-down

During power-up, the  $\overline{\text{RESET}}$  input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20 ms. The  $\overline{\text{RESET}}$  signal is normally derived from the PC master reset. However, a typical RC/diode power-up network can also be used for some applications.

After the low-to-high transition of  $\overline{\text{RESET}}$ , the following occurs:

- The synthesis/DSP enters an idle state, executing  $\overline{\text{RAS}}$  only refresh cycles.
- The RUN output is set to zero.
- If BOOT is low, then P16 program execution starts from address 0100H in ROM space ( $\overline{\text{WCS0}}$  low).
- If BOOT is high, then P16 program execution starts from address 0000H in internal bootstrap ROM space. The internal bootstrap expects to receive 256 words from the 16-bit burst transfer port, which will be stored from 0100H to 01FFH into the external DRAM space. The bootstrap then resumes control at address 0100H.

If  $\overline{\text{PDWN}}$  is asserted low, then all I/Os and outputs will be floated and the crystal oscillator and PLL will be stopped. The chip enters a deep power-down sleep mode. To exit power-down,  $\overline{\text{PDWN}}$  has to be asserted high, then  $\overline{\text{RESET}}$  applied.

## Recommended Board Layout

Like all HCMOS high-integration ICs, the following simple rules of board layout are mandatory for reliable chip operation:

- GND,  $V_{CC}$ ,  $V_{C3}$  distribution, decouplings

All GND,  $V_{CC}$ ,  $V_{C3}$  pins should be connected. GND and  $V_{CC}$  planes are strongly recommended below the SAM9707. The board GND and  $V_{CC}$  distribution should be in grid form. If 3.3V supply is not available, then  $V_{C3}$  can be derived from  $V_{CC}$  by two 1N4148 diodes in series.

Recommended decoupling is 0.1  $\mu\text{F}$  at each corner of the IC with an additional 10  $\mu\text{F}$  decoupling close to the crystal.  $V_{C3}$  requires a single 0.1  $\mu\text{F}$  decoupling close to the IC.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the SAM9707 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from SAM9707.

- Buses

Parallel layout from D0 - D15 and DRA0 - DRA11/WD0 - WD15 should be avoided. The D0 - D15 bus is an asynchronous, high-transient, current-type bus. Even on short distances, it can induce pulses on DRA0 - DRA11/WD0 - WD15, which can corrupt address and/or data on these buses.

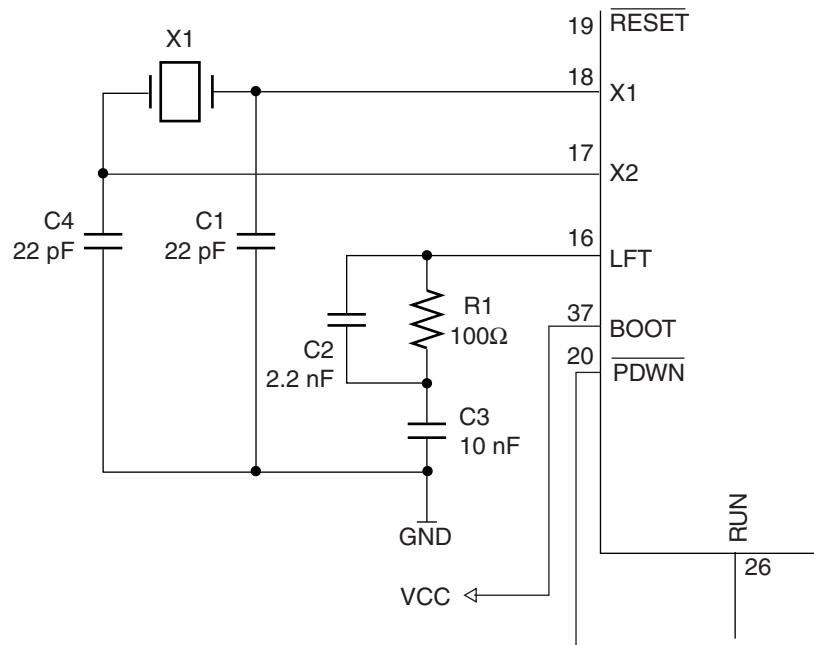
A ground plane should be implemented below the D0 - D15 bus, which connects to the PC-ISA connector and to the SAM9707 GND.

A ground plane should be implemented below the DRA0 - DRA11/WD0 - WD15 bus, which connects to the DRAM SIMM grounds and to the SAM9707.

- Analog section

A specific AGND ground plane that connects by a single trace to the GND ground should be provided. No digital signals should cross the AGND plane. Refer to the codec vendor-recommended layout for correct implementation of the analog section.

## Recommended Crystal Compensation and LFT Filter



## Absolute Maximum Ratings

| Symbol   | Parameter/Condition                                              | Min  | Typ | Max            | Unit |
|----------|------------------------------------------------------------------|------|-----|----------------|------|
|          | Ambient Temperature (power applied)                              | -40  |     | +85            | °C   |
|          | Storage Temperature                                              | -6.5 |     | +150           | °C   |
|          | Voltage on any pin (except X1)                                   | -0.5 |     | $V_{CC} + 0.5$ | V    |
|          | Voltage on X1 pin                                                | -0.5 |     | $V_{C3} + 0.5$ | V    |
| $V_{CC}$ | Supply Voltage                                                   | -0.5 |     | 6.5            | V    |
| $V_{C3}$ | Supply Voltage                                                   | -0.5 |     | 4.5            | V    |
|          | Maximum $I_{OL}$ per I/O pin<br>(except D[15:0], IRQ, I/O ready) |      |     | 10             | mA   |
|          | Maximum $I_{OL}$ , D[15:0], IRQ, I/O ready                       |      |     | 30             | mA   |

Note: All voltages with respect to 0V, GND = 0V

## Recommended Operating Conditions

| Symbol   | Parameter/Condition           | Min | Typ     | Max | Unit |
|----------|-------------------------------|-----|---------|-----|------|
| $V_{CC}$ | Supply Voltage <sup>(1)</sup> | 3   | 3.3/5.0 | 5.5 | V    |
| $V_{C3}$ | Supply Voltage                | 3   | 3.3     | 4.5 | V    |
| $T_A$    | Operating Ambient Temperature | 0   |         | 70  | °C   |

Note: 1. When using 3.3V supply, care must be taken that voltage applied on pin does not exceed  $V_{CC} + 0.5V$ .

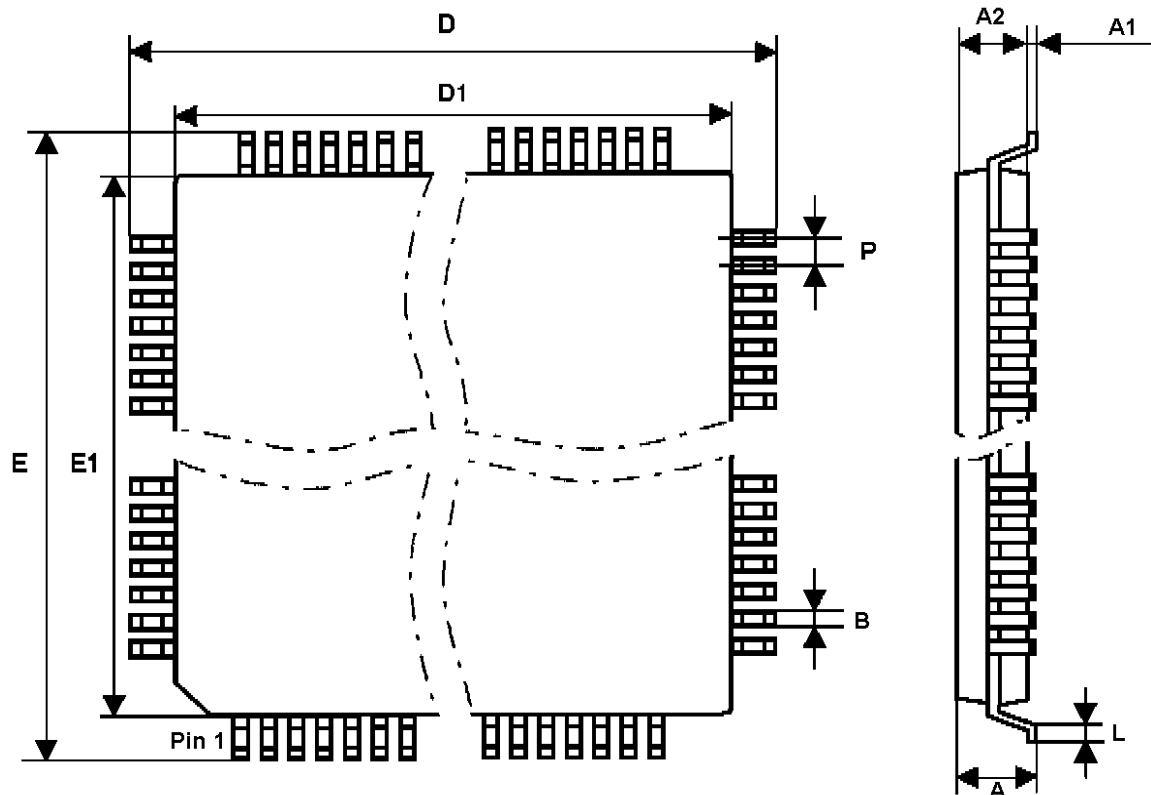
## DC Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{C3} = 3.3V \pm 10\%$

| Symbol   | Parameter/Condition                                                                                                           | $V_{CC}$ | Min  | Typ | Max  | Unit          |
|----------|-------------------------------------------------------------------------------------------------------------------------------|----------|------|-----|------|---------------|
| $V_{IL}$ | Low-level Input Voltage                                                                                                       | 3.3      | -0.5 |     | 1.0  | V             |
|          |                                                                                                                               | 5.0      | -0.5 |     | 1.7  | V             |
| $V_{IH}$ | High-level Input Voltage                                                                                                      | 3.3      | 2.3  |     | 3.8  | V             |
|          |                                                                                                                               | 5.0      | 3.3  |     | 5.5  | V             |
| $V_{OL}$ | Low-level Output Voltage<br>D[15:0], IRQ, I/O ready: $I_{OL} = -24\text{ mA}$<br>others except LFT: $I_{OL} = -3.2\text{ mA}$ | 3.3      |      |     | 0.45 | V             |
|          |                                                                                                                               | 5.0      |      |     | 0.45 | V             |
| $V_{OH}$ | High-level Output Voltage<br>D[15:0], IRQ, I/O ready: $I_{OH} = 10\text{ mA}$<br>others except LFT: $I_{OH} = 0.8\text{ mA}$  | 3.3      | 2.8  |     |      | V             |
|          |                                                                                                                               | 5.0      | 4.5  |     |      | V             |
| $I_{CC}$ | Power Supply Current (crystal freq. = 12 MHz)                                                                                 | 3.3      |      | 70  | 90   | mA            |
|          |                                                                                                                               | 5.0      |      | 25  | 35   | mA            |
|          | Power-down Supply Current                                                                                                     |          |      | 70  | 100  | $\mu\text{A}$ |

## Mechanical Dimensions

**Figure 17.** 144-lead Thin Plastic Lead Quad Flat Pack



**Table 9.** Package Dimensions (in mm)

| Dimension | Min   | Typ   | Max   |
|-----------|-------|-------|-------|
| A         | 1.40  | 1.50  | 1.60  |
| A1        | 0.05  | 0.10  | 0.15  |
| A2        | 1.35  | 1.40  | 1.45  |
| D         | 21.90 | 22.00 | 22.10 |
| D1        | 19.90 | 20.00 | 20.10 |
| E         | 21.90 | 22.00 | 22.10 |
| E1        | 19.90 | 20.00 | 20.10 |
| L         | 0.45  | 0.60  | 0.75  |
| P         |       | 0.50  |       |
| B         | 0.17  | 0.22  | 0.27  |



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