OVERVIEW

- 1.2 Micron CMOS
- 2-level
- 540 to 22,330 Gates
- Up to 210 I/O Pads
- TTL/CMOS Compatible I/O
- >4000V ESD Protection
- FPGA Conversion Utilities
- Full-scan Insertion Available
- >400 Library Components
- Wide Package Selection
- ISO Certified Suppliers
- Extensive Workstation Support

DESCRIPTION

The S1000 family of 1.2 micron CMOS Gate Arrays are fabricated using a 2-level metal oxide-isolated process. The process is unmatched for speed and density, while offering users access to highly integrated logic solutions. The family provides high noise immunity levels and very low power consumption typical of CMOS. All inputs and outputs may be compatible with either TTL or CMOS logic levels and are fully protected from electrostatic discharge and latch-up. The family consist of 10 base sets ranging from 540 to 22,330 equivalent 2-input NAND gates with I/O counts up to 210.

SiQUEST offers complete design support for new designs as well as engineering and software expertise in migrating FPGA's to a better cost effective and performance solution. Extensive library support and other proprietary tools are available on most commercial platforms. SiQUEST also offers FPGA prototyping to verify design integrity prior to manufacturing.

SUMMARY

DEVICE	GATES	USABLE GATES	DEFINABLE IO	DEDICATED PADS	TOTAL PADS
S000	540	500	32	8	40
S100	1,204	963	48	8	56
S200	2,399	1,840	66	8	74
S300	3,624	2,899	82	8	90
S400	5,040	4,032	98	8	106
S500	7,488	5,990	119	8	126
S600	10,360	8,288	142	8	150
S700	13,570	10,856	162	8	170
S800	16,848	13,478	182	8	190
S900	22,330	16,750	202	8	210

MAXIMUM RATINGS

Storage Temperature	**-65C to 150C**
Ambient Temperature	**-55C to 125C**
Voltage on any pin relative to Vss	**-0.3V, +7V**
Voltage on any pin relative to Vdd	**+0.3V**

These ratings define stress parameters under which useful product performance may be impaired. All CMOS circuits are susceptible to damage from stress voltages even when inputs are properly protected internally.

OPERATING CHARACTERISTICS

PARAMETER		CONDITION	TA = +25C VDD = 5.0V		TA = +70C VDD = 4.75V		TA = +125C VDD = 4.50V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
IOH Output High Current		VOH = 2.4V	3, 5, 7, 14		2, 4, 6,12		1.5, 3.2, 5, 10		mA
IOL Output Low Current		VOL = 0.4V	3, 5, 7, 14		2, 4, 6,12		1.5, 3.2, 5, 10		mA
VIH Input High Voltage		TTL Input	2.0		2.0		2.0		Volts
		CMOS Input	3.5		3.5		3.5		Volts
VIL Input Low Voltage		TTL Input		0.8		0.8		0.8	Volts
		CMOS Input		1.5		1.5		1.5	Volts
IIN Input Load Current		VSS<Vin<Vdd		+/- 1.0		+/- 1.0		+/- 1.0	uA
IDD VDD Supply Current		Per Cell Per MHZ (typ)	2.0		2.5		3.0		uA
		Per Cell Per MHZ (typ)	5		10		20		uA
CI Input Capacitance		Typical	4		4		4		pF
CO Output Capacitance		Typical	8		8		8		pF
Output Buffer Delay		Load = 10 LSTTL +40pF	4.0		6.0		8.0		ns
Inverter Delay		Worst Process		0.8		1.4		1.6	ns
2-Input NAND Delay		Worst Process		1.0		1.7		2.0	ns
2-Input NOR Delay		Worst Process		1.4		2.4		2.8	ns
D-Type Flip-Flop	Clk to Q Delay	Fanout = 4		2.0		3.5		4.0	ns
D-Type Flip-Flop	D Setup	TYP Metal	1.5		2.0		3.0		ns
D-Type Flip-Flop	D Hold	TYP Metal	1.5		2.0		3.0		ns
D-Type Flip-Flop	Toggle Rate	TYP Metal	200		125		105		MHZ

Notes:
1. Outputs may be paralleled to increase drive or create special output configurations.
2. Users may select either CMOS or TTL compatible logic levels. TTL interface requires TTL operating voltages.
3. Capacitance is indicated for typical interface conditions. Worst case will depend upon circuit configuration and package being used.
4. Actual internal logic delays depend on a number of factors, including process parameters, supply voltage, temperature, fanout, and interconnect. The values shown are very conservative representations of circuit performance actually experienced across a broad range of applications.