OVERVIEW

- 0.5 Micron CMOS
- 2-level or 3-level Metal
- 8,712 to 215,296 Gates
- Up to 256 I/O Pads
- TTL/CMOS Compatible I/O
- >4000V ESD Protection
- FPGA Conversion Utilities
- Full-scan Insertion Available
- >400 Library Components
- Wide Package Selection
- ISO Certified Suppliers
- Extensive Workstation Support

DESCRIPTION

The S5000 family of 0.5 micron CMOS Gate Arrays are fabricated using either a 2-level or 3-level metal oxide-isolated process. The process is unmatched for speed and density, while offering users access to highly integrated logic solutions. The family provides high noise immunity levels and very low power consumption typical of CMOS. All inputs and outputs may be compatible with either TTL or CMOS logic levels and are fully protected from electrostatic discharge and latch-up. The family consist of 10 base sets ranging from 8,712 to 215,296 available 2-input equivalent NAND gates with I/O counts up to 256.

SiQUEST offers complete design support for new designs as well as engineering and software expertise in migrating FPGA's to a better cost effective and performance solution. Extensive library support and other proprietary tools are available on most commercial platforms. SiQUEST also offers FPGA prototyping to verify design integrity prior to manufacturing.

SUMMARY

DEVICE	TOTAL I/O	TOTAL GATES	USABLE GATES	
			3-METAL	2-METAL
S5068	68	21,780	17,424	10,890
S5084	84	32,000	25,600	16,000
S5100	100	44,180	35,244	22,090
S5128	128	70,805	56,644	35,403
S5144	144	88,445	70,756	44,223
S5164	164	112,500	90,000	56.250
S5184	184	142,805	110,224	71,403
S5208	208	180,500	144,400	90,250
S5240	240	237,620	190,096	118,810
S5256	256	269,120	215,296	134,560

MAXIMUM RATINGS

Storage Temperature	**-65C to 150C**
Ambient Temperature	**-55C to 125C**
Voltage on any pin relative to Vss	**-0.3V, +6V**
Voltage on any pin relative to Vdd	**+0.3V**

These ratings define stress parameters under which useful product performance may be impaired. All CMOS circuits are susceptible to damage from stress voltages even when inputs are properly protected internally.

OPERATING CHARACTERISTICS

PARAMETER		CONDITION	TA = +25C VDD = 5.0V		TA = +70C VDD = 4.75V		TA = +125C VDD = 4.50V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Output High Current (IOH)		VOH = 3.5V	4, 8, 12, 16, 24		4, 8, 12, 16, 24		4, 8, 12, 16, 24		mA
Output Low Current (IOL)		VOL = 0.4V	4, 8, 12, 16, 24		4, 8, 12, 16, 24		4, 8, 12, 16, 24		
Input High Voltage (VIH)		TTL Input	2.0		2.0		2.0		Volts
		CMOS Input	3.5		3.5		3.5		
Input Low Voltage (VIL)		TTL Input		0.8		0.8		0.8	
		CMOS Input		1.5		1.5		1.5	
Schmitt Input (VIH)		TTL	1.87		1.87		1.87		
		CMOS (5V)	3.22		3.22		3.22		
		CMOS (3V)	2.08		2.08		2.08		
Schmitt Input (VIL)		TTL		1.1		1.1		1.1	
		CMOS (5V)		1.8		1.8		1.8	
		CMOS (3V)		1.22		1.22		1.22	
Input Load Current (IIN)		VSS<Vin<Vdd		+/- 1.0		+/- 1.0		+/- 1.0	uA
VDD Supply Current (IDD)		Per Cell Per MHZ (typ)	2.0		2.5		3.0		
		Per Cell Per MHZ (typ)	5		10		20		
Input Capacitance (CI)		Typical	3		3		3		pF
Output Capacitance (CO)		Typical	3		3		3		
Output Buffer Delay (8ma)		Load = 20pF	2.06		2.48		3.10		ns
Inverter Delay		Worst Process Fanout = 8 TYP Metal		0.45		0.54		0.68	
2-Input NAND Delay				0.50		0.61		0.76	
2-Input NOR Delay				0.62		0.74		0.93	
D-Type Flip-Flop	Clk to Q Delay			1.09		1.31		1.65	
	D Setup		0.69		0.83		1.03		
	D Hold		0.17		0.20		0.25		
	Toggle Rate		500		410		325		MHZ

Notes

1. User's may select either CMOS or TTL compatible logic levels. TTL interface requires TTL operating voltages.
2. Capacitance is indicated for typical interface conditions. Worst case will depend upon circuit configuration and package being used.
4. Actual internal logic delays depend on a number of factors, including process parameters, supply voltage, temperature, fanout, and interconnect. The values shown are very conservative representations of circuit performance actually experienced across a broad range of applications.