SiW1601 Link Controller IC

1. INTRODUCTION

The SiW1601 Link Controller IC is part of Silicon Wave's Odyssey™ solutions for Bluetooth™ wireless communications. The SiW1601 IC provides the Bluetooth link management and control functions in a digital ASIC. Combined with the SiW1502 Radio Modem IC, it provides a complete and cost effective hardware solution to integrate into products.

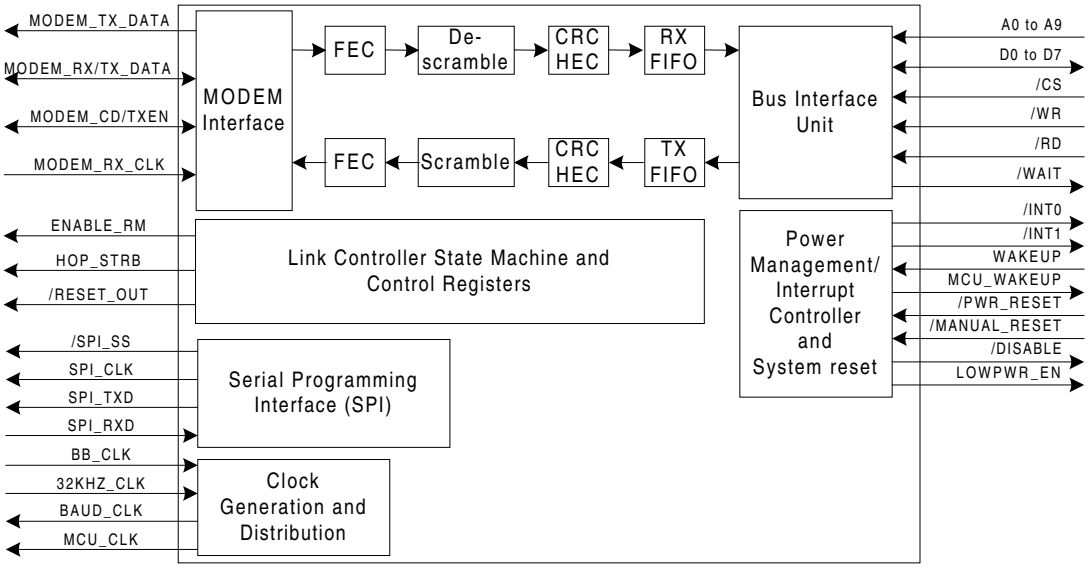


Figure 1: SiW1601 IC Link Controller Functional Block Diagram

2. FEATURES

- Direct interface to SiW1502 Radio Modem IC.
- Link control function implemented in hardware compliant to Bluetooth Specification 1.0 B.
- Support for all Bluetooth packet types.
- ACL and SCO connections at full speed of 1 Mbit/second.
- Piconet and scatternet functions, including master/slave switch capabilities.
- Authentication and encryption as defined in the specification.
- Dual on-chip 384-byte transmit and receive FIFOs ensure packet data is never lost due to interrupt latency.
- Programmable interrupt controller.
- Time-critical packet processing.
- Low-power modes such as page, page scan, inquiry and inquiry scan.
- Support for transmit power control and receiver RSSI functions.
- 108-pin CBGA package.

3. APPLICATIONS

The SiW1601 IC is suitable for all applications requiring packet processing and link management for Bluetooth communications. When combined with the SiW1502 Radio Modem IC, a low power and cost effective solution can be implemented.

- **Individual Use**: mobile phone handset integration and accessories.
- **Office**: office PCs, notebook PCs, and laser printers interconnection.
- **Personal Data**: PDA, palmtop, and personal organizer communications.
- **Consumer**: digital cameras, handheld game units.
- **Automotive**: hands-free car kit.

A typical design of the modular architecture for a Bluetooth compliant product consists of the SiW1502 Radio Modem IC and the SiW1601 Link Controller IC along with the Hitachi H8S/2238 processor. This example illustrates the connection flow between the system's main components.

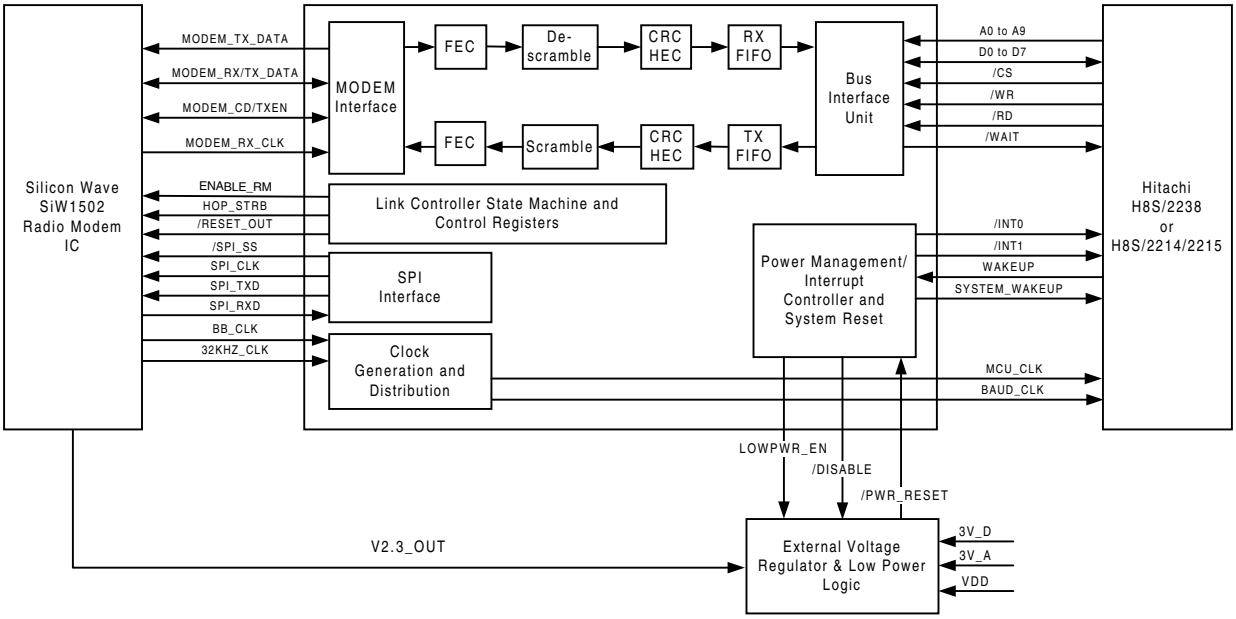


Figure 2: Typical SiW1601 IC Implementation

4. DESCRIPTION

The link controller hardware in the SiW1601 IC implements all the real-time, lower-layer protocol processing. This hardware performs the logical protocol processing within the unit that enables the host to communicate over a Bluetooth link. Real-time functions such as frequency hopping, burst timing, synthesizer programming, and clock synchronization are implemented in hardware. Also incorporated within the SiW1601 IC logic is power management and clock distribution. In addition to the radio control functions described above, the SiW1601 processes Bluetooth transmit and receive data as described below in sections 4.1 through 4.7.

4.1. FEC — Forward Error Correction

FEC corrects errors, which might have occurred during the transmission or receipt of the original data. FEC correction rates at 1/3 and 2/3 are implemented.

4.2. Whiten/De-whiten — Scramble/Unscramble

Whiten/Scramble refers to the process of randomizing transmitted data to avoid any undesirable DC bias effects that might result from long strings of 1's or 0's in data packets. De-whiten/Unscramble is the reversal of the original process where the original data can be extracted.

4.3. Encrypt/Decrypt — Apply/Remove Encryption

Encryption is the security feature where keys are used to prevent unauthorized access to data. This functional block is responsible for the processing of authentication and key management functions required for Bluetooth communications.

4.4. CRC — Cyclic Redundancy Check

This is the error detection function implemented to process the CRC field within the payload section of a Bluetooth transfer packet. On the receive side, the CRC is checked with the expected value based on algorithms. Prior to transmit, a proper CRC is generated and appended to the payload.

4.5. HEC — Header Error Correction

This is the error correction function for the 8-bit HEC field of the Bluetooth packet header as described in Bluetooth Specification 1.0 B.

4.6. Rx Buffers — Storage for received packets

The FIFO buffer is 384 bytes in length. This functional block contains the actual FIFO buffer and the associated control and management functions.

4.7. Tx Buffers — Storage for packets to be transmitted

The FIFO buffer for received packets is 384 bytes in length. This functional block contains the actual FIFO buffers and the associated control and management functions.

5. PIN DESCRIPTIONS

Note that all output pins are full CMOS drivers. There are no open drain drivers on outputs.

5.1. Microprocessor Interface

The main interface to the microprocessor is an 8-bit data bus with a 10-bit address bus. This interface is designed to connect to standard microprocessors with common interface signals. Interrupt request lines provide sleep/wake control to the processor. To facilitate system power management, the SiW1601 IC controls the clock signal to the processor.

Name	Direction	Description
A0 to A9	I	10-bit parallel address from the microprocessor. For the Hitachi H8S/2238, connect to A0 to A9 on the H8.
D0 to D7	I/O	8-bit parallel data bus between the microprocessor and the SiW1601 IC. Since only 8 bits are used, connect these pins to <D8 to D15> of the Hitachi H8 microprocessor. This signal is an input during reset.
/CS	I	Chip select or enable from the microprocessor for selecting the SiW1601 IC. This is an active low signal.
/WR	I	Write signal from the microprocessor. This is an active low signal.
/RD	I	Read signal from the microprocessor. This is an active low signal.
/WAIT	O	Wait state control signal to postpone baseband controller access until the Bluetooth radio modem is ready. This is an active low signal. This signal outputs 1 when in reset.
/INT0	O	Interrupt request 0 to the processor. This is an active low signal. This signal outputs 1 when in reset.
/INT1	O	Interrupt request 1 to the processor. This is an active low signal. This signal outputs 1 when in reset.
WAKEUP	I	Interrupt input from the processor that forces the SiW1601 IC to wake up when in sleep mode.
MCU_WAKEUP	O	Wake up signal to the microprocessor. This signal is typically connected to the non-maskable interrupt (NMI) input of the processor. This signal outputs 0 when in reset.

5.2. Radio Modem Interface

The SiW1601 IC interfaces to the SiW1502 Radio Modem for transmit/receive data and radio control. The SPI bus is used to access the internal control registers of the radio modem. Please refer to the SiW1502 Radio Modem IC Data Sheet for additional information on the modem interface.

Name	Direction	Description
MODEM_TX_DATA	O	Transmit data supplied to the SiW1502 IC. This signal outputs 0 when in reset.
MODEM_RX/TX_DATA	I/O	A bi-directional data pin used to transfer data between the controller and the SiW1502 IC. Direction is programmable, based on SiW1502 register settings. This signal is an input during reset.
MODEM_CD/TXEN	I/O	Dual function Carrier Detect (CD) input from the SiW1502 IC and Transmit Enable (TXEN) to the SiW1502 IC. During transmit, this pin is used as an OUTPUT to indicate valid transmit data. During receive, this pin is used as INPUT to detect valid carrier. This signal is an input when in reset.
MODEM_RX_CLK	I	Receive clock input from the SiW1502 IC.
/SPI_SS	O	SPI slave select signal to the SiW1502 IC to select a device as the target of data transfer. This is an active low signal. This signal outputs 1 when in reset.
SPI_CLK	O	SPI Clock signal. This signal outputs 0 when in reset.
SPI_TXD	O	SPI Transmit data to the SiW1502 IC. This signal outputs 0 when in reset.
SPI_RXD	I	SPI Receive data from the SiW1502 IC.
HOP_STRB	O	Hop strobe signals from the controller to indicate the start of a transmit or receive cycle. This signal outputs 0 when in reset.
ENABLE_RM	O	This is the enable signal for the SiW1502 IC. This signal outputs 1 when in reset.
/RESET_OUT	O	Output signal used to reset the SiW1502 Radio Modem. This is an active low signal. This signal outputs 0 when in reset.

5.3. Power and Ground

Name	Direction	Description
VDD	I	3.0 V supply voltage. Nominal range is 2.7 V to 3.3 V.
VSS	I	Ground input.
GND	I	Unused input. Connect to Ground.

5.4. Clock and Reset Signals

There are two clock inputs into the SiW1601 IC. 32KHZ_CLK is used in the power-down mode to drive the minimal logic circuits to maintain the Bluetooth compliant clock. The 32-MHz clock used for the radio modem is also used to run the SiW1601 IC. When the 32-MHz oscillator is disabled, the current draw will be in the microamperes (µA).

Name	Direction	Description
BB_CLK	I	Baseband main clock input.
32KHZ_CLK	I	32-kHz clock input. This input is typically from the SiW1502 IC 32-kHz output.
MCU_CLK	O	Controlled clock to the microprocessor. This clock is generated from the 32-MHz crystal and is programmable. Typical output to the H8S/2238 is 10.667 MHz. This signal outputs 1 when in reset.
BAUD_CLK	O	Clock output to microprocessor's serial interface clock logic for baud rate generation. This clock rate is derived from the 32-MHz clock and is programmable for various baud rates. This signal outputs 0 when in reset.
/PWR_RESET	I	Resets the MCU_CLK and BAUD_CLK logic only. Will cause /RESET_OUT to go active (low) to reset the SiW1502 IC.
/MANUAL_RESET	I	Reset input signal to reset the SiW1601 IC Bluetooth controller logic, except for MCU_CLK and BAUD_CLK logic. Will cause /RESET_OUT to go active (low) to reset the SiW1502 IC.
/DISABLE	O	Power control signal used to indicate disable state. This signal outputs 1 when in reset.
LOWPWR_EN	O	Power control signal used to indicate low power state. This signal outputs 0 when in reset.

5.5. Test Interface

The SiW1601 IC includes a test interface that will allow test and debug of internal logic.

Name	Direction	Description
JTMS	I	JTAG Test Mode Input.
JTCK	I	JTAG Test clock.
JTDI	I	JTAG Test data serial input.
JTDO	O	JTAG Test data serial output.
JTRST	I	JTAG Test reset in.
NC	I/0	No Connect.

6. PIN ASSIGNMENTS

The I/O signal pin assignments are detailed below but are preliminary and subject to change. Refer to package drawing for correct orientation. This is the TOP view.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	A3	A4	A6	VSS	A8	NC	NC	NC	NC	VDD	NC	GND	NC	GND
B	A1													GND
C	VSS		A2	A7	VDD	NC	NC	NC	VSS	NC	NC	NC		MODEM_ TX_DATA
D	BB_CLK		A0									MODEM_ RX/TX_ DATA		VDD
E	/PWR_ RESET		VDD		A5	A9	NC	NC	GND	HOP_ STRB		VSS		MODEM_ CD/TXEN
F	D6		D7		WAKEUP					LOWPWR_ EN		ENABLE_ RM		MODEM_ RX_CLK
G	VDD		D4		D5					VDD		MCU_ WAKEUP		/DISABLE
H	D2		D3		VSS					SPI_TXD		SPI_RXD		VSS
J	D1		D0		/MANUAL_ RESET					GND		/SPI_SS		SPI_CLK
K	32KHZ_ CLK		VDD		/CS	NC	BAUD_ CLK	JTRST	/RESET_ OUT	VDD		VSS		NC
L	VSS		/WR									GND		VDD
M	/RD		/INT1	NC	VDD	NC	VDD	JTCK	JTDO	VSS	NC	NC		NC
N	/WAIT													GND
P	/INT0	GND	VSS	NC	NC	MCU_ CLK	VSS	JTMS	JTDI	VSS	NC	VDD	GND	VSS

7. SIW1601 IC SPECIFICATIONS

Always turn off power before adding or removing devices from test and/or systems.

7.1. ESD Precautions

These devices are electrostatic sensitive. Devices should by handled in accordance with MIL-STD-1686. Devices should be transported and stored in anti-static containers. Ensure that equipment and personnel contacting the devices are properly grounded. Cover workbenches with grounded conductive mats.

7.2. Absolute Maximum Rating

Parameter	Description	Min	Max	Units
T_{ST}	Storage Temperature	-55	+125	°C
V_{ddmax}	Supply Voltage	-0.3	4.0	V
I_{in}	Input current	-10	10	mA
ESD	ESD Protection – Human Body Model		2000	V
Tj	Junction Temperature		125	°C

7.3. Recommended Operating Conditions

Parameter	Description	Min	Max	Units
T_{OP}	Operating Temperature	-20	+85	°C
V_{dd}	DC supply voltage	2.7	3.3	V

7.4. DC Parameters (T_{op} = -40 to 85°C; V_{DD} = 3.0V)

Parameter	Description	Min	Max	Units
V_{IL1}	Input low voltage, normal input pins	GND – 0.1	$0.3 \cdot V_{DD}$	V
V_{IH1}	Input high voltage, normal input pins	$0.7 \cdot V_{DD}$	V_{DD}	V
V_{IL2}	Input low voltage, D0 to D7, 32KHZ_CLK, BB_CLK, MODEM_CD/TXEN, MODEM_RX/TX_DATA, (Schmitt-trigger input, hysteresis = 0.8 V_{DD})	GND - 0.1	$0.2 \cdot V_{DD}$	V
V_{IH2}	Input high voltage, D0 to D7, 32KHZ_CLK, BB_CLK, MODEM_CD/TXEN, MODEM_RX/TX_DATA (Schmitt-trigger input, hysteresis = 0.8 V_{DD})	$0.8 \cdot V_{DD}$	V_{DD}	V
V_{OL}	Output low voltage, normal output and bi-directional pins	GND	0.4	V
V_{OH}	Output high voltage, normal output and bi-directional pins	$0.8 \cdot V_{DD}$	V_{DD}	V
I_{OH}	Output high current		-3.9	mA
I_{OL}	Output low current		3.9	mA
I_{LI}	Input leakage current, high-impedance state		10	µA
I_{LO}	Output leakage current, high-impedance state		10	µA

7.5. Current Consumption

Parameter	Description	Typical	Units
I_{DD} – (standby)	Current draw in standby mode	1.0	µA
I_{DD} – (idle)	Current draw in idle mode	1.0	mA
I_{DD} – (active)	Current draw in active (Transmit or Receive) mode	4.0	mA

7.6. AC Specifications

7.6.1. Microprocessor Interface: Read Data from an SiW1601 IC Register

Timing for a READ from a SiW1601 IC register is shown here. READ is initiated when the microprocessor asserts the /RD signal and ends with the de-assertion of the /RD signal. The microprocessor must be able to acquire the data within the data-valid timing.

Timing of the SiW1601 microprocessor interface does not depend on the MCU_CLK signal. This signal is shown only for reference relative to the microprocessor clock cycle.

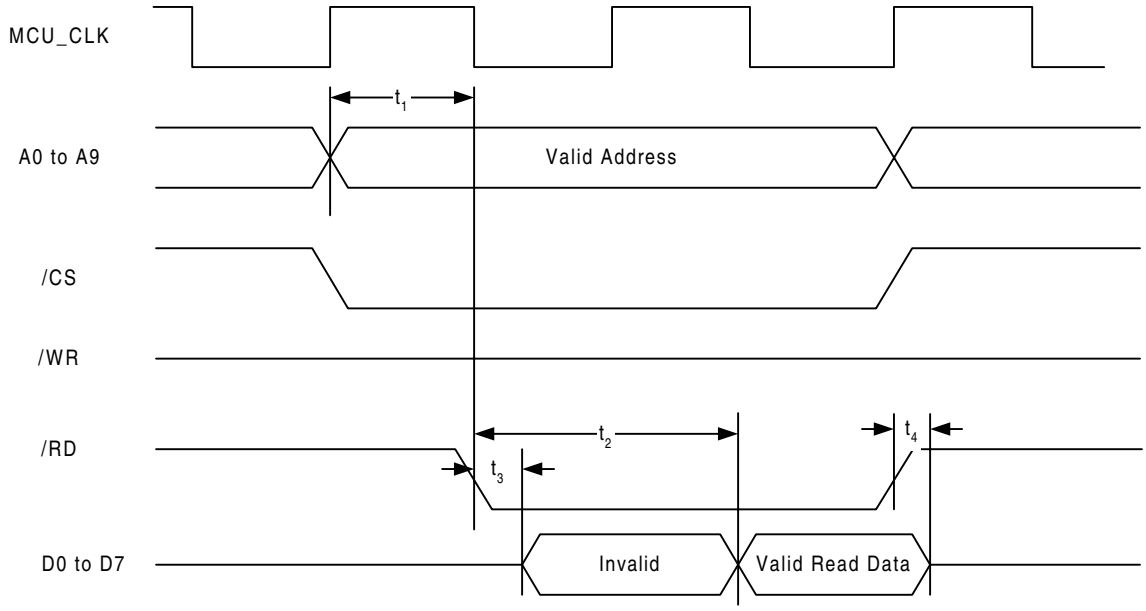


Figure 3: Timing Diagram for Read Cycle

Parameter	Description	Min	Max	Unit
t_1	Address set up time to /RD ↑	10		ns
t_2	/RD active to data valid	40		ns
t_3	Data output turn on time from /RD active	0	10	ns
t_4	Data output turn off time from /RD inactive	0	10	ns

Table 1: Address and Output Timing

7.6.2. Microprocessor Interface: Write Register Data to SiW1601 IC Register

Timing for a WRITE to a SiW1601 IC register is shown here. A WRITE is initiated when the microprocessor asserts the /WR signal and ends with the de-assertion of the /WR signal. WRITE data must meet the required setup and hold times relative to the rising edge of /WR.

Timing of the SiW1601 microprocessor interface does not depend on the MCU_CLK signal. This signal is shown only for reference relative to the microprocessor clock cycle.

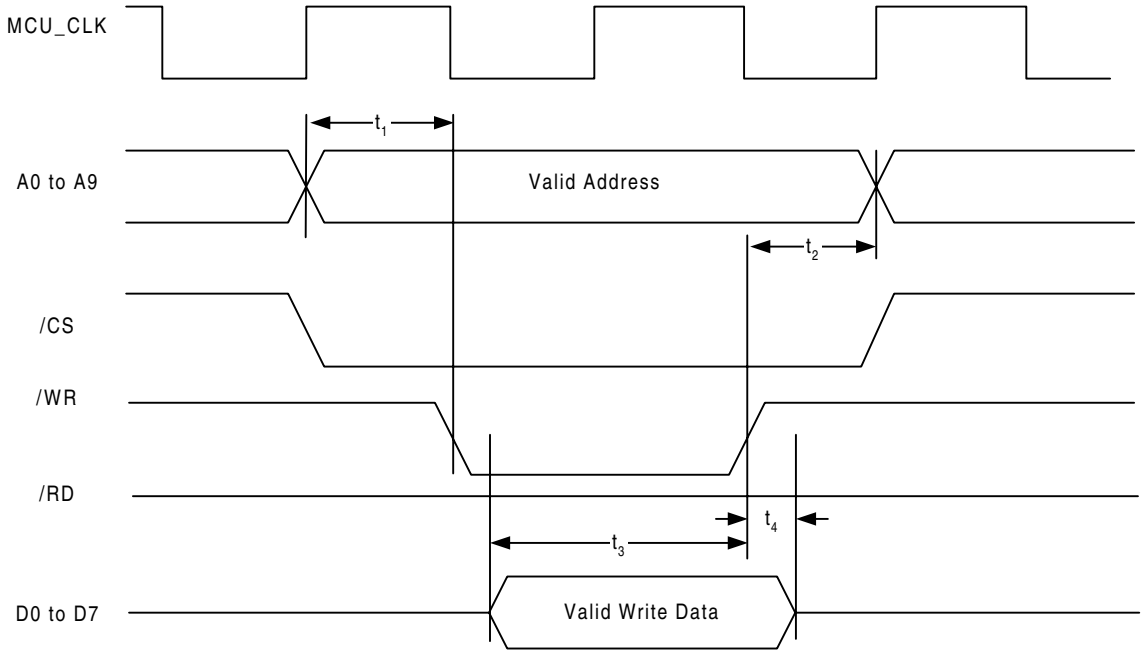


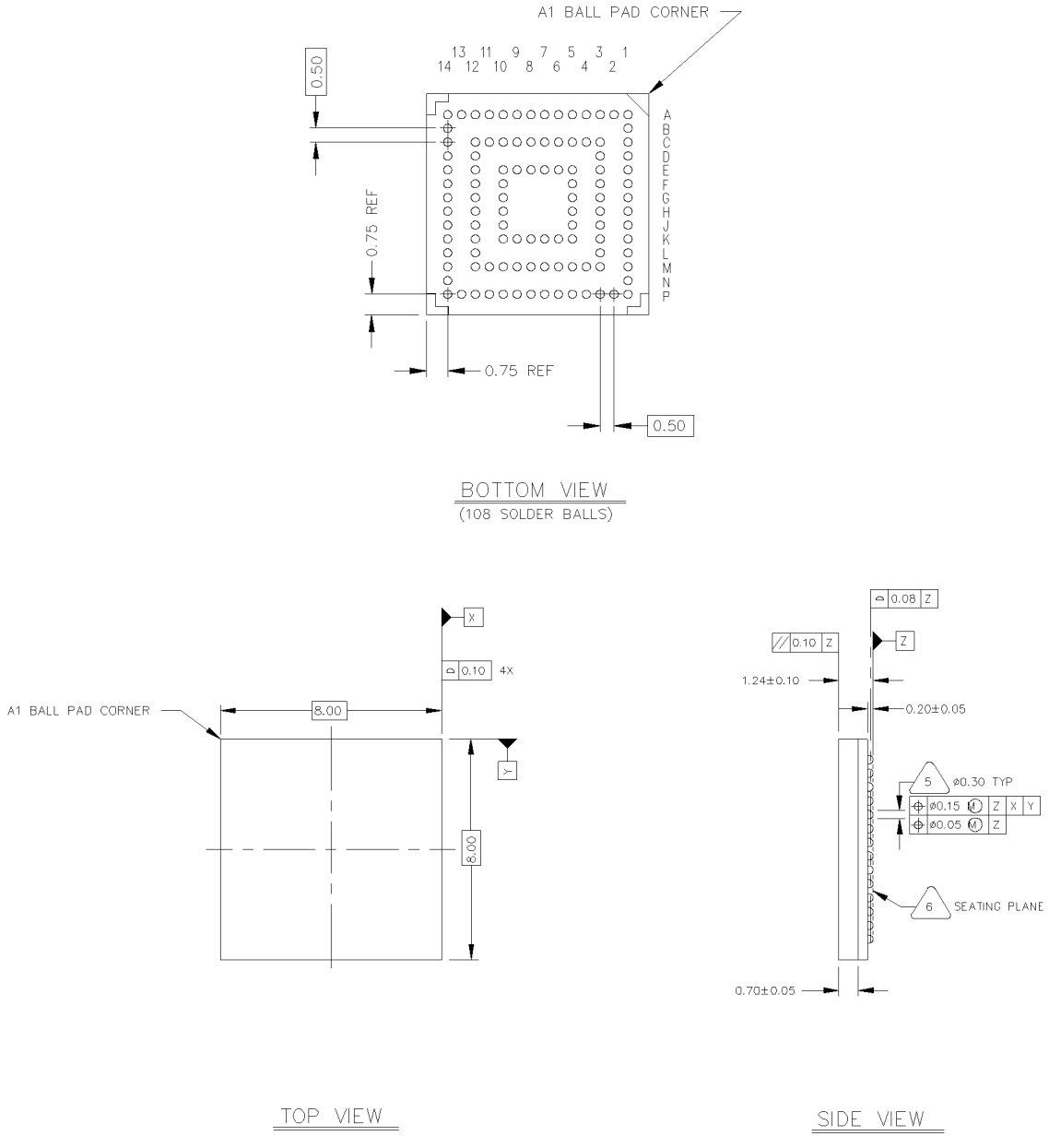
Figure 4: Timing Diagram for Write Cycle

Parameter	Description	Min	Max	Unit
t_1	Address set up time to start of /WR	10		ns
t_2	Address hold time to end of /WR	20		ns
t_3	Write data setup time to end of /WR	20		ns
t_4	Write data hold time relative to /WR inactive	20		ns

Table 2: Address Timing

8. PACKAGING

8.1. SiW1601 IC package: 108-pin CBGA, 8-by-8 mm body, 0.5-mm pitch



9. SOLDERING DATA

To be provided.

10. ORDERING INFORMATION

To be provided.

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