1400 MIPS 16-BIT FIXED POINT DSP (DIGITAL SIGNAL PROCESSOR)

HIGHLIGHTS

The SMJ320C6203 DSP is a member of the SMJ320C62x fixed-point DSP family in the SMJ320C6000 platform. The C6203 device is based on the high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for multichannel and multifunction applications.

Operating over the full military temperature range (-55°C to 125°C) at 175 MHz, the C6203 will be the highest performance, fixed-point, QML-processed DSP available. It can achieve 1400 MIPS (Million Fixed-Point Instructions per Second) peak performance. This DSP will be offered in a 27 x 27 mm, 429-ball, Ceramic Dimpled Ball Grid Array (CBGA) package.

The C6203 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. This processor has 32 general-purpose registers of 32-bit word length and eight highly independent functional units. The eight functional units provide six arithmetic logic units (ALUs) for a high degree of parallelism and two 16-bit multipliers for a 32-bit result. The C6203 can execute two multiply-accumulates (MACs) per cycle. This gives a total of 350 million MACs per second (MMACS) for the military C6203 device. The C6203 DSP includes application-specific hardware logic, on-chip memory and additional on-chip peripherals. The C62x family of DSPs include high density on-chip memory, with the C6203 device offering the most memory at 7 Mbits.

Every one of the high-performance DSPs within the SMJ320C6000 DSP platform are fully software compatible to allow you to start designing today with an assured road map to enhanced performance.

KEY FEATURES/BENEFITS
- Highest Performance Fixed-Point Digital Signal Processor (DSP) SMJ320C6203
  - 5.7-ns Instruction Cycle Time
  - 175-MHz Clock Rate
  - Eight 32-bit Instructions/Cycle
  - 1400 MIPS , 350 MMACS across the full military temperature range (-55°C to 125°C)
- VelociTI™ Advanced Very Long Instruction Word (VLIW) C62x CPU Core
  - Eight Highly Independent Functional Units:
    - Six ALUs (32-/40-bit)
    - Two 16-Bit Multipliers (32-bit Result)
  - Load-Store Architecture with 32 32-bit General-Purpose Registers
  - Instruction Packing Reduces Code Size
  - All Instructions are Conditional
- Instruction Set Features
  - Byte-Addressable (8-, 16-, 32-bit Data)
  - 32-bit Address Range
  - 8-bit Overflow Protection
  - Saturation
  - Bit-Field Extract, Set, Clear
  - Bit-Counting
  - Normalization
- 7M-bit of On-Chip SRAM

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KEY FEATURES/BENEFITS (continued)

- 32-bit External Memory Interface (EMIF)
  - Glueless Interface to Synchronous Memories: SDRAM or SBSRAM
  - Glueless Interface to Asynchronous Memories: SRAM, EPROM, and EEPROM
- Four-Channel Bootloading Direct-Memory-Access (DMA) Controller with an Auxiliary Channel
- Flexible Phase-Locked-Loop (PLL) Clock Generator
- 32-bit Expansion Bus
  - Glueless/Low-Glue Interface to Popular PCI Bridge Chips
  - Glueless/Low-Glue Interface to Popular Synchronous or Asynchronous Microprocessor Buses
  - Master/Slave Functionality
  - Glueless Interface to Synchronous FIFOs and Asynchronous Peripherals
- Multichannel Buffered Serial Ports (McBSPs)
  - Direct Interface to T1/E1, MVIP, SCSA Framers
  - ST-Bus-Switching Compatible
  - Up to 256 Channels Each
  - AC97-Compatible
  - Serial-Peripheral Interface (SPI) Compatible™
- Two 32-Bit General-Purpose Timers
- IEEE-1149.1 (JTAG Standard-Test-Access Port and Boundary Scan Architecture) Boundary-Scan-Compatible

PROCESS/PERFORMANCE OPTIONS

Device	Package	Speed	DSCC SMD	Processing
SN00372GLG Available Now	372-ball C-BGA	N/A	N/A	CBGA Daisy-Chain Package Prototype
SN00429GLE Available Now	429-ball C-BGA	N/A	N/A	C6203 CBGA Package Mechanical Sample
SMJ320C6203GLPM17 Est. Available 1Q01	429-ball C-BGA	175 MHz	5962-0051001QXA Est. Avail. 1Q01	-55°C to +125°C Full Military QML Processing
SM320C6203GLPM17 Est. Available 1Q01	429-ball C-BGA	175 MHz	N/A	-55°C to +125°C Extended Temp Processing

DIE SIZE

The die size of the C6203: 350 x 372 mils.
Bond pad opening: 76 microns
Bond pad pitch: 160 microns

TECHNOLOGY

5-Level Metal CMOS Process Technology / 0.15 μm L-effective (0.18 μm drawn)
3.3-volt I/Os, 1.5-volt Internal
ESD Level = TBD

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POWER DISSIPATION
The C6203 dissipates less than 1 W at 175 MHz (est.). The table below presents modeled package thermal characteristics data. The data can be used for approximating system thermal performance.

C6203 PACKAGE THERMAL CHARACTERISTICS
GLP = 429-ball C-DBGA   Ceramic-Dimpled Ball Grid Array: A C-DBGA weighs 6.3 grams.

The following table and notes define the typical thermal characteristics for the ceramic GLP package. This data is useful for preliminary engineering evaluations.

PARAMETER	TYP	UNIT
$R_{\theta JA}$	14.47	°C/W
$R_{\theta JMA}$ (airflow@150 fpm)	11.79	°C/W
$R_{\theta JMA}$ (airflow@250 fpm)	11.09	°C/W
$R_{\theta JMA}$ (airflow@500 fpm)	10.21	°C/W
$R_{\theta JC}$ /1	7.34	°C/W
$R_{\theta JC}$ /2	3.00	°C/W
$R_{\theta JB}$	6.20	°C/W

Typical GLP Package Thermal Characteristics

Notes:

$R_{\theta JA}$ Junction-to-ambient air thermal resistance: measured in a one cubic foot, still air enclosure.

$R_{\theta JMA}$ Junction-to-moving air thermal resistance: measured in a wind tunnel.

$R_{\theta JC}$ /1   Junction-to-case thermal resistance: measured to the top of the package lid.

$R_{\theta JC}$ /2   Junction-to-case thermal resistance: measured to the bottom of solder ball.

$R_{\theta JB}$ Junction-to-board thermal resistance: measured by soldering a thermocouple to one of the middle traces on the board at the edge of the package.

The above values were obtained by mounting the 429-GLP on a FR-4 board and testing per JESD-51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages. The board design connected all the GND balls directly to a GND plane, V_{DD} balls to a V_{DD} plane, and all the signals were routed on the top layer.

Key features of the thermal test board design are:
- Board material: FR-4
- Board design: 2S2P (double layer, double buried power plane)
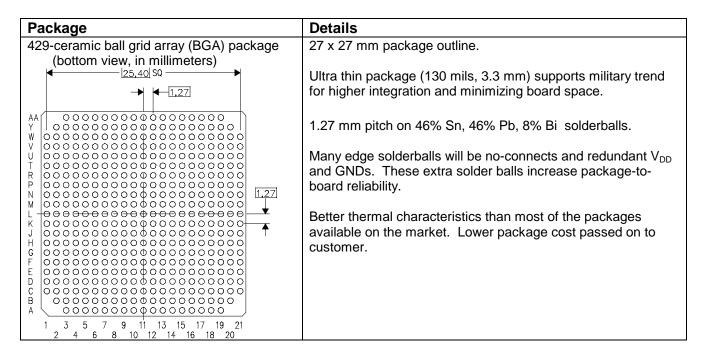- Board thickness: 0.062 +/- 0.006 inches
- Board dimensions: 4.0 x 4.5 inches
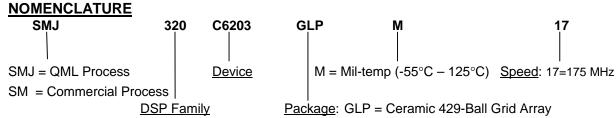- Trace thickness: 0.0028 inches
- Traces: 2 oz +/- 20% copper for signals and 1 oz +/- 10% copper for V_{DD} and GND planes

![Texas Instruments logo]

C6203 PACKAGE INFORMATION

Package	Details
429-ceramic ball grid array (BGA) package (bottom view, in millimeters) 25,40 SQ 1,27 AA Y W V U T R P N M L K J H G F E D C B A 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 1,27	27 x 27 mm package outline. Ultra thin package (130 mils, 3.3 mm) supports military trend for higher integration and minimizing board space. 1.27 mm pitch on 46% Sn, 46% Pb, 8% Bi solderballs. Many edge solderballs will be no-connects and redundant V_{DD} and GNDs. These extra solder balls increase package-to-board reliability. Better thermal characteristics than most of the packages available on the market. Lower package cost passed on to customer.

NOMENCLATURE

SMJ	320	C6203	GLP	M	17

SMJ = QML Process   Device   M = Mil-temp (-55°C – 125°C)   Speed: 17=175 MHz

SM = Commercial Process

DSP Family   Package: GLP = Ceramic 429-Ball Grid Array

DESIGN-IN SUPPORT

TI has the most extensive DSP application support

Product Information Center: (972) 644-5580 (For general information, availability, etc.)
DSP Developer's Village: dspvillage.ti.com/docs/dspvillagehome.jhtml
DSP Hotline (Technical questions):   www.ti.com/sc/docs/dsps/hotline/support.htm
Third Parties URL: www.ti.com/sc/docs/general/dsp/third/index.htm
Military DSP Info: http://www.ti.com/sc/docs/products/military/processr/index.htm

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Product Information Center

North America
Telephone # - 972-644-5580 (English)
Fax # - 972-480-7800
PIC - www.ti.com/sc/docs/pic/home.htm
PIC E-mail - sc-infomaster@ti.com
Military Products –
www.ti.com/sc/docs/military/welcome.htm
Distributor Listing - www.ti.com/sc/docs/distmenu.htm

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Italiano:	800 79 11 37 (free phone)
Deutsch:	+49-(0)8161-80 33 11
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Daisy Chain packages are used to evaluate/measure the package to board assembly process. They allow designers to verify the reliability of the package-to-board interface over temp cycles, shocks, aging, etc.

Daisy Chain CBGA (p/n=SN00372GLG)
for Ceramic-BGA to board Evaluation only

"GLG" and "GLP" Package Notes

D/C "GLG" package has 1.27 mm ball pitch
  same pitch as C6203 "GLP" package

D/C has Larger array size 22x22, not 21x21

D/C has Larger package 29mm Sq, not 27mm

Notes: A All linear dimensions are in millimeters
B. This drawing is subject to change without notice

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The hermetic CBGA (GLP) package is used for production builds of the C6203 DSP.

GLP (S-CBGA-N429)   CERAMIC BALL GRID ARRAY

27,20 / 26,80 SQ

25,40 TYP

1,27

AA Y W V U T R P N M L K J H G F E D C B A

1 3 5 7 9 11 13 15 17 19 21
2 4 6 8 10 12 14 16 18 20

1,27

1,22 / 1,00

3,30 MAX

Seating Plane

0,90 / 0,60   ⊕ ⌀ 0,10 Ⓜ

0,70 / 0,50

◁ 0,15

4164732/A 08/98

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice and should be used for initial evaluation purposes only.
         C. Falls within JEDEC MO-156

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