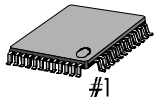
INTRODUCTION

S5L9290X is a signal processing LSI for the CD. Digital processing function (EFM demodulation, error correction), spindle motor servo processing, wide capture range DPLL and 1-bit DAC for the CD player are installed in S5L9290X.

48-LQFP-0707



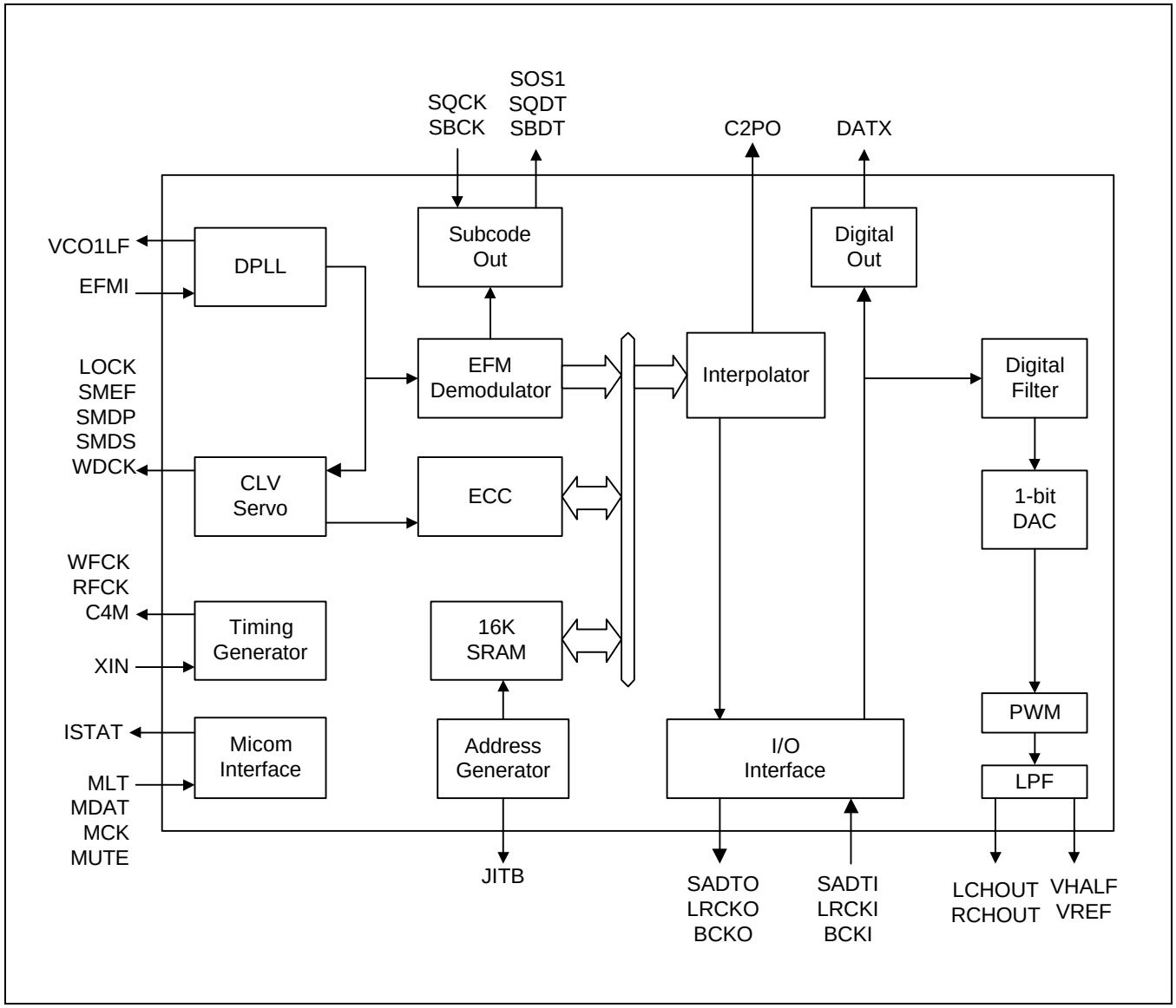
FEATURES

- Signal processing part
  - — EFM data demodulation
  - — Frame sync detection, protection, insertion
  - — Sub code data processing (Q data CRC check, Q data register installed)
  - — Error correction (C1: 2 error correction, C2: 4 erasure correction)
  - — Installed 16K SRAM for De-interleave
  - — Interpolation
  - — Digital audio interface
  - — CLV servo control (X1, X2)
  - — Wide capture range digital PLL (± 50%)
- Digital filter, DAC part
  - — 4 times over sampling digital filter
  - — Digital de-emphasis (can be process the 32kHz, 44.1kHz, 48kHz)
  - — Sigma-delta stereo DAC installed
  - — Audio L.P.F installed

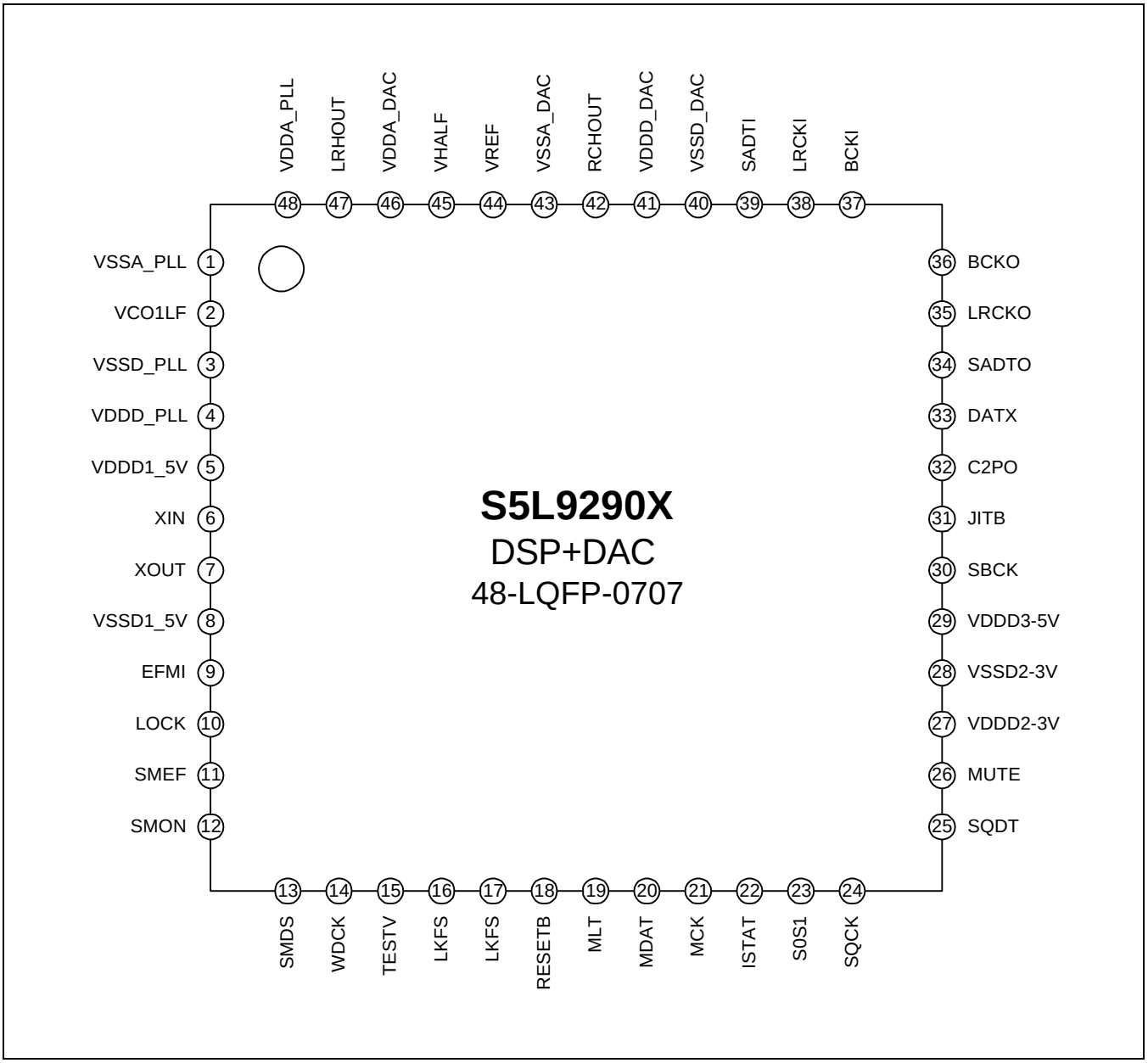
ORDERING INFORMATION

Device	Package	Supply Voltage	Operating Temperature
S5L9290X01—L0R0	48-LQFP-0707	2.7V — 3.3V (Analog, Internal logic) 2.7V — 5.5V (I/O port)	-20°C — +75°C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Table 1. Pin Description

NO.	NAME	I/O	Pin Description
1	VSSA_PLL	-	Analog Ground for DPLL
2	VCO1LF	O	Pump out for VCO1
3	VSSD_PLL	-	Digital Ground Separated Bulk Bias for DPLL
4	VDDD_PLL	-	Digital Power Separated Bulk Bias for DPLL (3V Power)
5	VDDD1-5V	-	Digital Power (5V Power, I/O PAD)
6	XIN	I	X'tal oscillator input (16.9344MHz)
7	XOUT	O	X'tal oscillator output
8	VSSD1	-	Digital Ground (I/O PAD)
9	EFMI	I	EFM signal input
10	LOCK	O	CLV Servo locking status output
11	SMEF	O	LPF time constant control of the spindle servo error signal
12	SMDP	O	Phase control output for Spindle Motor drive
13	SMDS	O	Speed control output for Spindle Motor drive
14	WDCK	O	Word clock output (Normal Speed : 88.2KHz, Double Speed : 176.4KHz)
15	TESTV	I	Various Data/Clock Input
16	LKFS	O	The Lock status output of frame sync
17	C4M	O	4.2336MHz clock output
18	RESETB	I	System Reset at 'L'
19	MLT	I	Latch signal input from Micom
20	MDAT	I	Serial data input from Micom
21	MCK	I	Serial data receiving clock input from Micom
22	ISTAT	O	The internal status output to Micom
23	S0S1	O	Subcode sync signal(S0+S1) output
24	SQCK	I	Subcode-Q data transfering bit clock input

Table 1. Pin Description (continued)

NO.	NAME	I/O	Function Description
25	SQDT	O	Subcode-Q data serial output
26	MUTE	I	System mute at 'H'
27	VDDD2-3V	-	Digital Power (3V Power, Internal Logic)
28	VSSD2	-	Digital Ground (Internal Logic)
28	VDDD3-5V	-	Digital Power (5V Power, I/O PAD)
30	SBCK	I	Subcode data transfering bit clock
31	JITB	O	Internal SRAM jitter margin status output
32	C2PO	O	C2 pointer output
33	DATX	O	Digital audio data output
34	SADTO	O	Serial audio data output (48 slot, MSB first)
35	LRCKO	O	Channel clock output
36	BCKO	O	Bit clock output
37	BCKI	I	Bit clock input
38	LRCKI	I	Channel clock input
39	SADTI	I	Serial audio data input (48 slot, MSB first)
40	VSSD_DAC	-	Digital Ground for DAC
41	VDDD_DAC	-	Digital Power for DAC (3V Power)
42	RCHOUT	O	Right-Channel audio output through DAC
43	VSSA_DAC	-	Analog Ground for DAC
44	VREF	O	Referance Voltage output for bypass
45	VHALF	O	Referance Voltage output for bypass
46	VDDA_DAC	-	Analog Power for DAC (3V Power)
47	LCHOUT	O	Left-Channel audio output through DAC
48	VDDA_PLL	-	Analog Power for PLL (3V Power)

MAXIMUM ABSOLUTE RATINGS

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	3V: -0.3 — 3.8 5V: -0.3 — 7.0	V
Input supply voltage	V_I	3V I/O: -0.3 — V_{DD} + 0.3 5V I/O: -0.3 — 5.5	V
Operating temperature	T_{OPR}	-20 — 75	°C
Storage temperature	T_{STG}	-40 — 125	°C

ELECTRICAL CHARACTERISTICS

OPERATING CONDITION

Item	Symbol	Operating Range	Unit
Power supply voltage	V_{DD}	3V: 2.7 — 3.3 5V: 4.5 — 5.5	V
Operating temp.	T_{OPR}	-20 — 75	°C

DC CHARACTERISTIC (V_{DD} = 3.0V, V_{SS} = 0V, TA = 25°C)

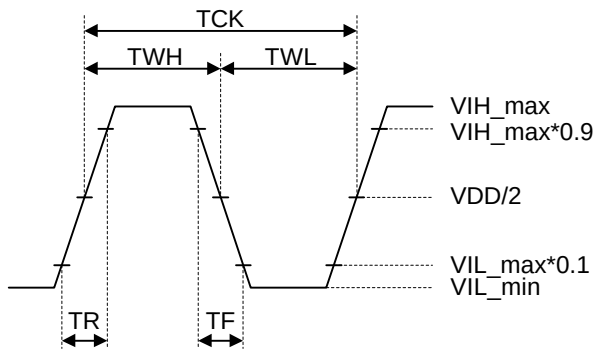
Item	Symbol	Condition	Design Values			Unit	Comment
			Min	Typ	Max		
'H' input voltage	VIH		0.8VDD	-	-	V	(Note 1)
'L' input voltage	VIL		-	-	0.2VDD	V	
'H' output voltage	VOH(1)	IOH = -1mA	VDD-0.2	-	-	V	(Note 2)
'L' output voltage	VOL(1)	IOL = 1mA	-	-	0.4	V	
Input leak current	ILKG	VI = 0-VDD	-10	-	10	uA	(Note 3)
Three state output leak current	I_{OZ}	VO = 0-VDD	-10	-	10	uA	(Note 4)

NOTES:
1. Related pins: All input terminal
2. Related pins: All output terminal
3. Related pins: All input terminal
4. Related pins: SMEF, SMDP, SMDS, ISTAT

AC CHARACTERISTIC

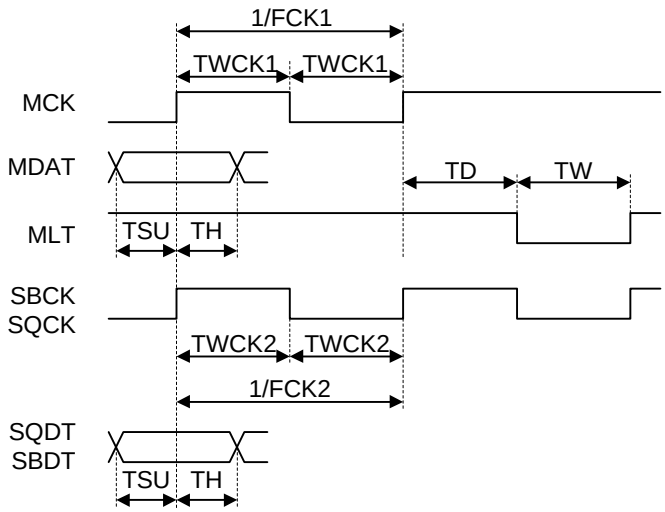
When Pulse is Applied to XIN (Ta = 25°C, VDD = 3.0V, VSS = 0V)

Item	Symbol	Min	Typ	Max	Unit
'H' level pulse width	TWH	13	-	-	ns
'L' level pulse width	TWL	13	-	-	ns
Pulse frequency	TCK	26	-	-	ns
Input 'H' level	VIH	VDD-1.0	-	-	V
Input 'L' level	VIL	-	-	0.8	V
Rising & falling time	TR,TF	-	-	10	ns



MCK, MDAT, MLT (Ta = 25°C, VDD = 3.0V, VSS = 0V)

Item	Symbol	Max	Typ	Min	Unit
Clock frequency	FCK1	1	-	-	MHz
Clock pulse width	TWCK1	-	-	500	ns
Setup time	TSU	-	-	300	ns
Hold time	TH	-	-	300	ns
Delay time	TD	-	-	300	ns
Latch pulse width	TW	-	-	1000	ns
SQCK frequency	FCK2	1	-	-	MHz
SQCK pulse width	TWCK2	-	-	500	ns

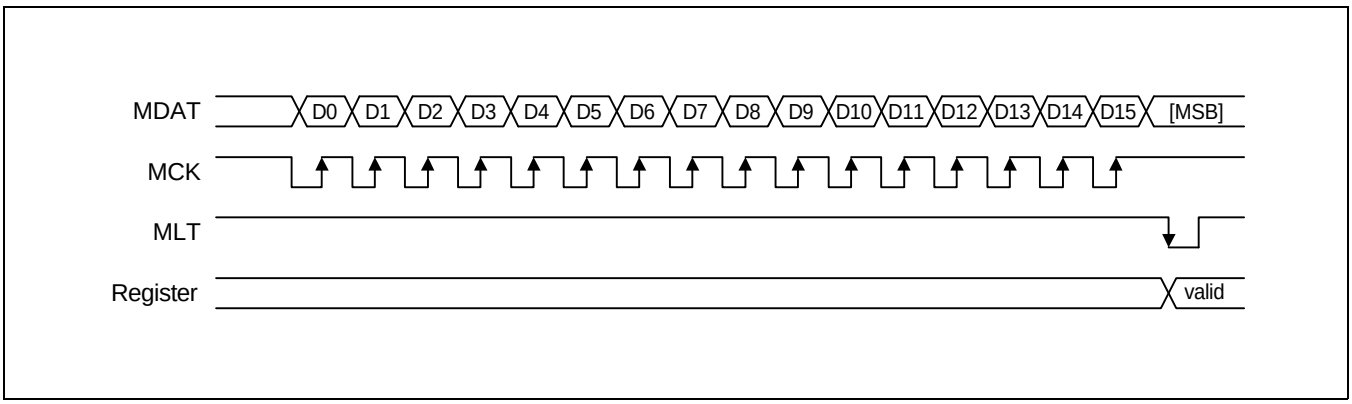


DESCRIPTION OF OPERATION

MICOM INTERFACE

Each command is executed when data and command is input as LSB first according to timing shown in the figure below through MDAT, MCK, and MLT inputs and ISTAT output.

- Address: 8 bit
- Data: 8 bit (writing), 8/16 bit (reading)



DSP Command

Command	Address	Data								ISTAT pin
		D7	D6	D5	D4	D3	D2	D1	D0	
DPLL control 1	10001000 ($88)	WIDE	PHSE DET	PHASE GAIN	DLF GAIN	ACC3t		CO3T	RETREF	Hi-Z
DPLL control 2	10001001 ($89)	REF98[1:0]		REF98[1:0]		MAXTGAIN[1:0]		CAPRANGE [1:0]		Hi-Z
DPLL control 3	10001010 ($8A)	DIVS1 [1:0]		DIVP1 [1:0]						Hi-Z
DPLL control 4	10001100 ($8C)	DIVM1[7:0]								Hi-Z
DPLL control 5	1000101 ($8D)	CMD SPLIT	PHASE ONLY	MRANGE[1:0]		FSREG	PLL TEST	PLL PWDN1	-	Hi-Z
Function control	10010000 ($90)	CDROM	FDEEM	DEEM	ERA OFF	C1PNT	-	-	JITM	EMPH
Audio control	10010001 ($91)	MUTE	ZCMT	ZDENL	ATTN	DAC MUTE	VFLGC	DATX MUTE	DATX OENB	S0S1
Frame Sync control	10010010 ($92)	FSEL [1:0]		WSEL[1:0]		FSMD [1:0]		-	-	LKFS
Mode control 1	10010011 ($93)	GNR PWDN	-	DAC PWDNB	-	ECLV	ECLV PD	NCLV	CRCQ	JITB
Mode control 2	10010100 ($94)	MSCK SW	-	-	-	RFCK SW	-	-	JTFRV1	LOCK
CLV gain control	10011000 ($98)	OVSPL	WBN	WPN	-	OVSPL MS	WB	WP	GAIN	EFMFLAG
CLV mode control	10011001 ($99)	UNLOCK[1:0]		CLV IDLE	PCEN	CM3	CM2	CM1	CM0	/(PW≥64)
CLV control 1	10011010 ($9A)	STRIO	SMM	PME	SME	PCKSEL[1:0]		PGAIN[1:0]		Hi-Z
CLV control 2	10011011 ($9B)	LC	PML	SML[1:0]		POS	SGAIN[2:0]			Hi-Z
CLV control 3	10011100 ($9C)	POFFSET[7:0]								Hi-Z
CLV control 4	10011101 ($9D)	SPLUS	SDD	PHASEDIV[1:0]		SMOFFSET[3:0]				Hi-Z
CLV control 5	10011110 ($9E)	SOFFSET[7:0]								Hi-Z
CLV control 6	10011111 ($9F)	SMEFOUTB	CLV DEFT	-	DSVEN	DSV3T	DSVINV	DSVGAIN[1:0]		Hi-Z

Command	Address	Data								ISTAT pin
		D7	D6	D5	D4	D3	D2	D1	D0	
1-bit DAC & DATX control	10100011 ($A3)	TXSF [3:0]				SC[3:0]		SPLFREQ[1:0]		Hi-Z
1-bit DAC attenuation control	10100100 ($A4)	M5	M4	M3	M2	M1	M0	SOFT ATTN	CMD DIRECT	Hi-Z
Output port control	10101001 ($A9)	TALK [3:0]				-	-	-	-	Hi-Z
SADT I/F control	10110000 ($B0)	-	-	-	-	-	-	-	MSON	Hi-Z
Play mode control	11110000 ($F0)	DS1	DS0	-	-	-	DFCK	-	-	Hi-Z
TEST mode control	11111111 ($FF)	TEST [3:0]				-	-	-	-	Hi-Z

$88 Command

Digital PLL control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 1	10001000 ($88)	WIDE	PHASE DET	PHASE GAIN	DLF GAIN	ACC3t	-	CO3T	RETREF

Bit	Name	Data = 0	Data = 1	Comment
D7	WIDE	Normal	Wide	Wide mode selection
D6	PHASE-DET	Now	new	Phase detection method selection (option)
D5	PHASE-GAIN	1/2t	1t	Phase Adjust gain selection (option)
D4	DLF-GAIN	1/2^10	1/2^9	Digital loop filter gain selection (option)
D3	ACC3t	ignore ± 3t	accept ± 3t	ROM coefficient selection (option)
D2	-	-	-	-
D1	CO3T	Normal	3T	3T correction (option)
D0	REFRET	± 1.1%	± 2.3%	Reference when return to M1 = 98

$89 Command

Digital PLL control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 2	10001001 ($89)	REF98[1:0]		REF[1:0]		MAXTGAIN[1:0]		CAPRANGE[1:0]	

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[7:6]	REF98[1:0]	± 1.7%	± 2.3%	± 3.4%	± 4.6%	Outward reference when M1 = 98
D[5:4]	REF[1:0]	± 1.7%	± 2.3%	± 3.4%	± 4.6%	Outward reference when M1≠ 98
D[3:2]	MAXTGAIN[1:0]	1	1/2	1/4	1/8	MAX T accumulation gain
D[1:0]	CAPRANGE[1:0]	50%	40%	30%	20%	Capture range selection

$8A Command

Digital PLL control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 3	10001010 ($8A)	DIVS1[1:0]		DIVP1[5:0]					

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[7:6]	DIVS1[1:0]	1	1/2	1/4	1/8	PLL1 post scalar

Bits	Name	Data = 000000 - 111111	Comment
D[5:0]	DIVP1[5:0]	0 - 63	PLL1 pre divider

$8C Command

Digital PLL Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 4	10001100 ($8C)	DIVM1[7:0]							

Bits	Name	Data = 00000000 - 11111111	Comment
D[7:0]	DIVM1[7:0]	0 - 255	PLL1 main divider

$8D Command

Digital PLL control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DPLL control 5	10001101 ($8D)	CMD SPLIT	PHASE ONLY	MRANGE[1:0]		FSREG	PLLTEST	PLL PWRDN1	-

CMD_SPLIT (option)

The digital PLL control micom command is automatically applied when the speed is changed($F0) or at Jitter Free2($94).
H : Each DPLL control Micom Commands ($8A, $8B, $8B) are applied using the Micom Interface terminals (MCK, MDAT, MLT).
L : DPLL control Micom Command ($8A, $8B, $8B) is applied automatically inside.

PHASE_ONLY (option)

Controls phase compensation status at DPLL.
H : Phase compensation
L : Phase compensation + Frequency compensation

MRANGE[1:0]

Controls the range of the PLL1 Main Divider M value range

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[5:4]	MRANGE[1:0]	50%	40%	30%	20%	Lock Range

FSREG

Verifies the Frame Sync status(|Thigh-Tlow| $\leq$ 1) at MAX T
H : Verify
L : Ignore

PLLTEST

PLL1 TEST mode
H : TEST (M1<=M2), L : Normal

PLL PWDN1

PLL1 Power Down mode
H : Power Down, L : Normal

$90 Command

DSP Function Control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Function control	10010000 ($90)	CDROM	FDEEM	DEEM	ERA OFF	C1PNT	-	-	JITM

CDROM

H: CDROM mode
L: CDP mode

FDEEM, DEEM

De-Emphasis Automatic control and compulsion control select

FDEEM	DEEM	De-emphasis on/off	Comment
0	0	Off	-
0	1	On/Off	Automatic operate to detect emphasis signal of subcode information
1	0	Off	-
1	1	On	Operate without regard to emphasis signal of subcode information

ERA_OFF:

H: Erasure correction off
L: Erasure correction on

C1PNT :

C1 2 Error correction C1 pointer set/reset control
H: C1PNT = reset
L: C1PNT = set

C1PNT (option)

Mute SRAM Address copy permission (Write base count copy from read base counter)

H: Accept
L: Reject

$91 Command (Default value: 00000000)

Control of each function related to audio data

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Audio control	10010001 ($91)	MUTE	ZCMT	ZDENL	ATTN	DAC MUTEB	VFALG	DATX MUTE	DATX ENB

MUTE

DSP MUTE enable signal
H: DSP MUTE on
L: DSP MUTE off

ZCMT

DSP Zero cross mute enable signal (effective when MUTE signal is ON)
H: DSP Zero cross mute on
L: DSP Zero cross mute off

ZDENL

1-bit DAC Zero detection MUTE disable signal
H: 1-bit DAC Zero detection MUTE off
L: 1-bit DAC Zero detection MUTE on

ATTN

DSP -12dB attenuation enable signal
H: DSP Attenuation on
L: DSP Attenuation off

DAC MUTEB

Set the input data 1-bit DAC function block to 'L'
H: DAC MUTE off. L: DAC MUTE on

VFALG:

Control the input V-bit to DATX Block
H: 'L' set
L: C2PO use

DATX_MUTE:

Set the input data to digital audio interface function block to 'L'
H: DATX MUTE on
L: DATX MUTE off

DATX_ENB:

DATX function disabled, fixed DATX output.
H: DATX output disable
L: DATX output enable

ATTN	MUTE	dB
0	0	0
0	1	- ∞
1	0	- 12
1	1	- 12

<ATTN and MUTE relation>

$92 Command

Control of functions related to frame sync

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Frame sync control	10010010 ($92)	FSEL[1:0]		WSEL[1:0]		FSMD [1:0]		-	-

FSEL[1:0]: Control of cycle for frame sync protection and insertion

FSEL[1:0]	Control Cycle (Frame)
00	2
01	4
10	8
11	13

WSEL[1:0]: Control of window size related to frame sync protection

WSEL[1:0]	Window Size(t)
00	± 3
01	± 7
10	± 13
11	± 26

FSMD: [1:0] Frame sync detection method control

FSMD [1:0]	Detection Method	Comment
00	Pattern	11t — 11t
01	Compensation	11t — 11t, 10 — 12t, 12t — 10t
10	Cycle 1	10t — 11t, 11t — 12t, 11t — 11t, 11t — 10t, 12t — 11t
11	Cycle 2	cycle 1, 10t — 12t, 12t — 10t

$93 Command

Control of modes of functions in DSP

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Mode control 1	10010011 ($93)	GNR PWRDN	-	DAC PWPDNB	-	ECLV	ECLV PD	NCLV	CRCQ

GNR_PWDN

DSP Power Down
H : Power Down On, L : Power Down Off

DAC_PWDNB

1-bit DAC function Power Down
H : Power Down Off, L : Power Down On

ECLV

Emergency CLV Servo, Overflow prevention
H : Repeat output of H, Hi-Z, and L at a regular cycle through the SMDP terminal

L : normal operation

ECLV_PD

SMDP output cycle control at ECLV
H: Bottom Hold cycle (Refer to $98)
L : Peak Hold cycle(Refer to $98)

NCLV

H : CLV phase servo driven by frame sync
L : CLV phase servo driven by base counter

CRCQ

L : SQDT without SQOK
H : SQDT with SQOK (If S0S1 is 'H', SQDT = SQOK)

$94 Command

Control of function modes in DSP

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Mode control 2	10010100 ($94)	MSCK SW	WDCK SW	-	-	RFCK SW	-	-	JTFRV1

Bit	Name	Data = 0	Data = 1	Comment
D7	MSCK_SW	Internal	External	Input SBCK terminal when input the 1-bit DAC master clock in external
D6	WDCK_SW	X'tal	VCO2	WDCK frequency selection
D5	-	-	-	-
D4	-	-	-	-
D3	RFCK_SW	MICOM	TESTV	Use RFCK clock in CLV sero processing according to jitter mode
D2	-	-	-	-
D1	-	-	-	-
D0	JTFRV1	X'tal	VCO1	Use VCO1 clock in data processing

$98 Command

Control cycle and gain control in CLV speed mode

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV gain control	10011000 ($98)	OVSPL	WBN	WPN	-	OVSPL MS	WB	WP	GAIN

OVSPL (option)

Output by oversampling the CLV output (SMDP, SMDS) cycle by 7.35kHz *4
H : Over-sampling Enable, L : Over-sampling Disable

WBN (option)

Bottom Hold Cycle control in the CLV speed mode
H : RFCK/64, L : determined by WB

WPN (option)

Peak Hold cycle control in the CLV speed mode
H : RFCK/8, L : determined by WP

OVSPL_MS (option)

SMDS output mode setting at over-sampling enable
H : PWM (H, L), L : Tri-State (H, Hi-Z, L)

WB

Bottom Hold cycle control in the CLV speed mode
H : RFCK/16, L : RFCK/32

WP

Peak Hold cycle control in the CLV speed mode
H : RFCK/2, L : RFCK/4

GAIN

SMDS output gain control in the CLV speed mode
H : 0dB, L : -12dB

$99 Command

CLV mode control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV mode control	10011001 ($99)	UNLOCK [1:0]		CLV IDLE	PCEN	CM3	CM2	CM1	CM0

UNLOCK[1:0]
unlock cycle control

UNLOCK[1:0]	Function
00	If LKFS can remain at 'L' for 128 frames, the LOCK is 'L'.
01	If LKFS can remain at 'L' for 112 frames, the LOCK is 'L'.
10	If LKFS can remain at 'L' for 96 frames, the LOCK is 'L'.
11	If LKFS can remain at 'L' for 80 frames, the LOCK is 'L'.

CLV_IDLE
Use to place CLV servo control in idle mode. (Set POS ($9B) to 'H')
H : Output a specific error ($9E, SOFFSET[7:0])to the SMDS terminal, IDLE mode.
L : Normal Mode

PCEN
Phase Error Masking status determination when setting the dead zone.
H : SMDP Phase Error Masking Enable. (When WFCK frequency Error has entered the Dead Zone)
L : SMDP Phase Error Masking Disable.

CM3 — CM0
CLV Servo Control Mode Setting

Mode	D3-D0	SMDP	SMDS	SMEF	SMON	Function
Forward (KICK)	1 0 0 0	H	Hi-Z	L	H	Spindle motor forward mode
Reverse (BRAKE)	1 0 1 0	L	Hi-Z	L	H	Spindle motor reverse mode
Speed (CLV-S)	1 1 1 0	Speed	Hi-Z	L	H	Rough servo mode at start up
Phase (CLV-P)	1 1 1 1	Phase	Phase	Hi-Z	H	PLL servo mode
XPHSP (CLV-A)	0 1 1 0	Speed Phase	Hi-Z Phase	L Hi-Z	H	Normal play mode (When LOCK is 'H', CLV-P operation and when 'L', CLV-S operation)
VPHSP (CLV-A)	0 1 0 1	Speed Phase	Hi-Z Phase	L Hi-Z	H	Automatic servo mode (When LOCK is 'H' or GFS is 'H', operate in CLV-P, but others, operate in CLV-S')
Stop (STOP)	0 0 0 0	L	Hi-Z	L	L	Spindle motor stop mode

$9A Command

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 1	10011010 ($9A)	STRIO	SMM	PME	SME	PCKSEL[1:0]		PGAIN[1:0]	

STRIO: Tri-state out enable in phase mode
H: Tri-state
L: PWM

SMM: SMDS mask limit manual setting enable
H: Manual setting
L: Auto setting

PME: SMDP mask enable
H: Mask enable
L: Mask disable

SME SMDS mask enable (dead zone enable)
H: Mask enable
L: Mask disable

PCKSEL[1:0]: MDP resolution clock selection

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[3:2]	PCKSEL [1:0]	CLK4M_CLV/2	CLK4M_CLV/4	CLK4M_CLV/8	CLK4M_CLV/ 16	MDP resolution clock selection

PGAIN: SMDP gain setting

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[1:0]	PGAIN[1:0]	1	1/2	1/4	1/8	MDP gain selection

$9B Command

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 2	10011011 ($9B)	LC	PML	SML[1:0]		POS	SGAIN[2:0]		

LC: Lock control
H : 1x → 2x or 2x → 1x then LOCK is forced to 0
L : Normal LOCK control

PML : MDP mask limit
H : SMDP mask for SMDS error center value ± 50%
L : SMDP mask for SMDS error center value ± 25%

SML: MDS mask limit (dead zone area) at MDS error error center value

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[5:4]	SML[1:0]	± 0%	± 6.25%	± 12.5%	± 25%	Dead zone selection

When it enters the dead zone around the data rate, the MDS error value is output as 0.

This minimizes the change in plus(+) and minus(-) frequently generated in the reference data rate and reduces the number of times required for motor control to reduce power consumption.
The phase control also turns off in this dead zone.

POS: MDP output selection
H: Gain controlled SMDP
L: Normal SMDP

SGAIN: SMDS gain setting

SGAIN[2:0]	Gain Value
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

$9C Command

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 3	10011100 ($9C)	POFFSET[7:0]							

POFFSET[7]:SMDP offset sign
H: Minus (-)
L: Plus (+)

POFFSET[6:0]: SMDP offset absolute value

$9D Command

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 4	10011101 ($9D)	SPLUS	SDD	PHASEDIV[1:0]		SMOFFSET[3:0]			

SPLUS:
SMDS offset plus enable
H: Enable
L: Disable

SDD: SMDS speed down control disable
H: Speed down control disable
L: Speed down control enable

PHASEDIV[5:4]: Phase comparator period setting

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[5:4]	PHASEDIV[1:0]	RFCK/2	RFCK/4	RFCK/8	RFCK/16	Phase comparator period selection

SMOFFSET[3:0]:SMDS mask limit value
0000 - 1111

$9E Command

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
CLV control 5	10011110 ($9E)	SOFFSET[7:0]							

SOFFSET[7:0]:

SMDS offset

If SPLUS is 1, add SOFFSET to SMDS error to output the final error.

$9F Command

Digital CLV control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
SBS Filter Gain Control 2	10011111 ($A2)	SMEF OUTB	CLV DFCT	-	DSVEN	DSV3T	DSVINV	DSVGAIN[1:0]	

SMEF_OUTB

Control the SMEF output

SMEF_OUTB		SMDP	SMDS	SMEF	SMON
0	Speed mode	H, L, Hi-Z	Hi-Z	L	H
	Phase mode	H, L, Hi-Z	Hi-L	Hi-Z	H
1	Speed mode	H, L, Hi-Z	Hi-Z	Hi-Z	H
	Phase mode	H, L, Hi-Z	Hi-L	L	H

CLV_DFCT

If the EFM pulse width is greater than 64T, it assumes a defect in the CLV servo control; makes SMDP and SMDS to Hi-Z; and stops the CLV servo control

H: Defect detection control enable

L: Defect detection control disable

DSVEN

DSV output enable signal

H: DSV signal output in LKFS termianl

L: DSV output disable (LKFS signal out)

DSV3T

Calculate only the 3T in EFM signal

H: Only 3T L: All T

DSVINV

Invert output the DSV signal

H: Invert output L: Normal output

DSVGAIN [1:0]

Decide the DSV output gain

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[1:0]	DSVGAIN[1:0]					

$A3 Command

1-bit DAC Mode control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
1-bit DAC & DATX control	10100011 ($A3)	TXSF[3:0]				SC[1:0]		SPLFREQ [1:0]	

TXSF [3:0]

DATX Sampling rate control
Control the sampling rate (bit 24 - bit 27) among the control status data in digital audio output signal (DATX)

TXSF [3:0]	Sampling rate
0000	44.1kHz
0100	48kHz
1100	32kHz
Others	Reserved

SC[1:0]

Calibration range scale control

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[1:0]	SC[1:0]	X1	X2	X4	X0.5	Effective when use the zero detection mute

SPLFEQ[1:0]

Decide the 1-bit DAC Sampling frequency

Bits	Name	Data = 00	Data = 01	Data = 10	Data = 11	Comment
D[1:0]	SPKFREQ[1:0]	44	48	32	Reserved	Audio data sampling frequency (kHz)

$A4 Command

Digital attenuation level control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
DAC ATTN control	01011101 ($5D)	M5	M4	M3	M2	M1	M0	SOFT ATTN	CMD DIRECT

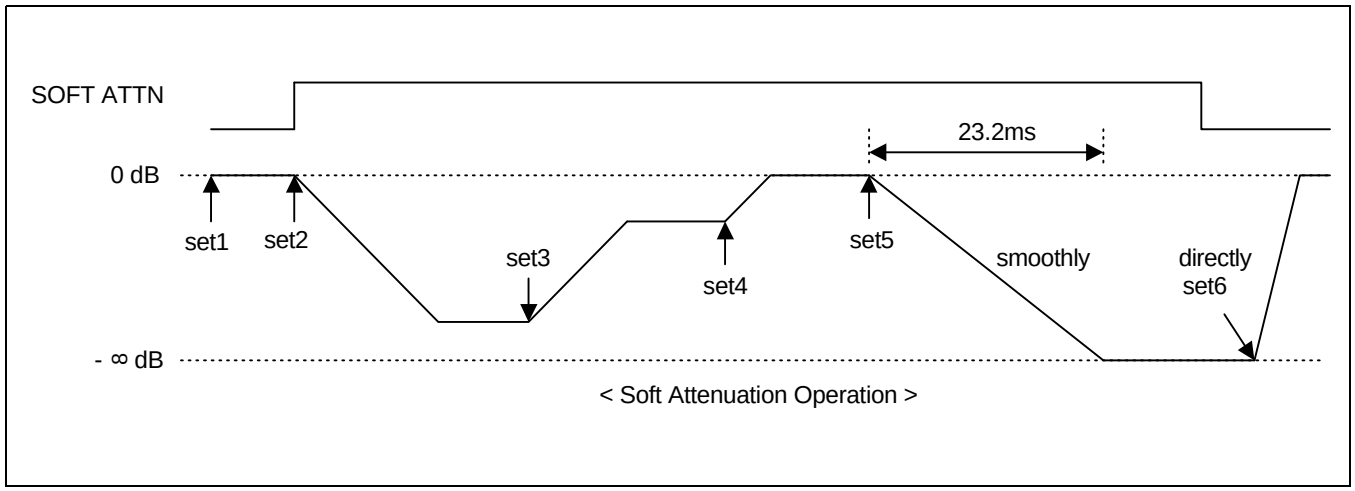
M5 - M0

Attenuation level control (64 step)

MDAT (MSB M5 M4 M3 M2 M1 M0 LSB)	Attenuation Level (dB)	MDAT (MSB M5 M4 M3 M2 M1 M0 LSB)	Attenuation Level (dB)
0 0 0 0 0 0	0	1 0 0 0 0 0	-6.30
0 0 0 0 0 1	-0.28	1 0 0 0 0 1	-6.58
0 0 0 0 1 0	-0.42	1 0 0 0 1 0	-6.88
0 0 0 0 1 1	-0.56	1 0 0 0 1 1	-7.18
0 0 0 1 0 0	-0.71	1 0 0 1 0 0	-7.50
0 0 0 1 0 1	-0.86	1 0 0 1 0 1	-7.82
0 0 0 1 1 0	-1.01	1 0 0 1 1 0	-8.16
0 0 0 1 1 1	-1.16	1 0 0 1 1 1	-8.52
0 0 1 0 0 0	-1.32	1 0 1 0 0 0	-8.89
0 0 1 0 0 1	-1.48	1 0 1 0 0 1	-9.28
0 0 1 0 1 0	-1.64	1 0 1 0 1 0	-9.68
0 0 1 0 1 1	-1.80	1 0 1 0 1 1	-10.10
0 0 1 1 0 0	-1.97	1 0 1 1 0 0	-10.55
0 0 1 1 0 1	-2.14	1 0 1 1 0 1	-11.02
0 0 1 1 1 0	-2.32	1 0 1 1 1 0	-11.51
0 0 1 1 1 1	-2.50	1 0 1 1 1 1	-12.04
0 1 0 0 0 0	-2.68	1 1 0 0 0 0	-12.60
0 1 0 0 0 1	-2.87	1 1 0 0 0 1	-13.20
0 1 0 0 1 0	-3.06	1 1 0 0 1 0	-13.84
0 1 0 0 1 1	-3.25	1 1 0 0 1 1	-14.54
0 1 0 1 0 0	-3.45	1 1 0 1 0 0	-15.30
0 1 0 1 0 1	-3.66	1 1 0 1 0 1	-16.12
0 1 0 1 1 0	-3.87	1 1 0 1 1 0	-17.04
0 1 0 1 1 1	-4.08	1 1 0 1 1 1	-18.06
0 1 1 0 0 0	-4.30	1 1 1 0 0 0	-19.22
0 1 1 0 0 1	-4.53	1 1 1 0 0 1	-20.56
0 1 1 0 1 0	-4.76	1 1 1 0 1 0	-22.14
0 1 1 0 1 1	-5.00	1 1 1 0 1 1	-24.08
0 1 1 1 0 0	-5.24	1 1 1 1 0 0	-26.58
0 1 1 1 0 1	-5.49	1 1 1 1 0 1	-30.10
0 1 1 1 1 0	-5.75	1 1 1 1 1 0	-36.12
0 1 1 1 1 1	-6.02	1 1 1 1 1 1	-∞

SOFT ATTN

Enable soft attenuation.
The attenuation level is divided into 64 steps.



< Soft Attenuation Operation >

— CMD DIRECT (option)

L : Attenuate the 1-bit DAC using the soft attenuation block.

H : Apply direct attenuation level to the 1-bit DAC without using the soft attenuation block. This disables the soft attenuation.

$A9 Command

Output signal on/off control and monitor output selection

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Output port control 2	10101001 ($A9)	TALK[3:0]				-	-	-	-

TALK [3:0]: Monitoring Terminal output selection
If MSON of $B0 is "H" state, SET TALK [2:0] = 0000

Bit Name	Output Description					
TALK[3:0]	**LKFS**	**C2PO**	**JITB**	**SADTO**	**LRCKO**	**BCKO**
0000	LKFS	C2PO	JITB	SADTO	LRCKO	BCKO
0001	LKFS	C2PO	ECFL3	ECFL2	ECFL1	ECFL0
0010	PLCK	C2PO	FSYNC	FSDW	ULKFS	EFMFLAG
0011	WFCK	C2PO	RFCK	SQOK	TIM2	EMPH
0100	Fchange	DIVN98	DIVNFAST	AT2T	EFMIN	EFMOUT
0101	DIVN[5]	DIVN[4]	DIVN[3]	DIVN[2]	DIVN[1]	DIVN[0]
0110	LKFS	C2PO	JITB	DAC_SADT	DAC_LRCK	DAC_BCK
0111	LKFS	LKFS	JITB	SADTO	LRCKO	BCKO
1XXX	LKFS	C2PO	SBDT	SADTO	LRCKO	BCKO

$B0 Command

Serial aduio data interface control

Command	Address	Data							
		D7	D6	D5	D4	D3	D2	D1	D0
SADT I/F control	10100000 ($B0)	-	-	-	-	-	-	-	MSON

MSON:

Serial audio data interfce on/off (ESP on/off)
H: On
L: Off

$F0 Command

Data processing speed control

Command	Address	Data							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Play mode control	11110000 ($A9)	DS1	DS0	-	-	-	DFCK	-	-

DS1, DS0: X1, X2 speed control

DS1	DS0	Mode
0	0	1X
1	1	2X

DFCK 1-bit DAC speed control
H: 2X L: 1X

EFM DEMODULATION

EMF block is a circuit, which demodulates the EMF signal read from the disc, and is composed of the frame sync detection circuit and the control signal generator circuit.

EFM Demodulation

When the modulated 14 channel bit data is input, they are demodulated to 8 bit data. The demodulated data are classified into two types, the subcode data and audio data. The subcode data is input to the subcode processing block and the audio data is stored in the internal SRAM, after which it is corrected for error.

Frame Sync Detection/Protection/Insertion

Frame sync detection

The data is configured in the unit of frames, of which frame sync, subcode data, audio data, redundancy data are configured in one frame. The frame sync is detected because it is used as the reference signal to synchronize the data output from the frame sync for extracting correct data. (Related Command Register: $92, FSMD [1:0])

Frame sync protection/insertion

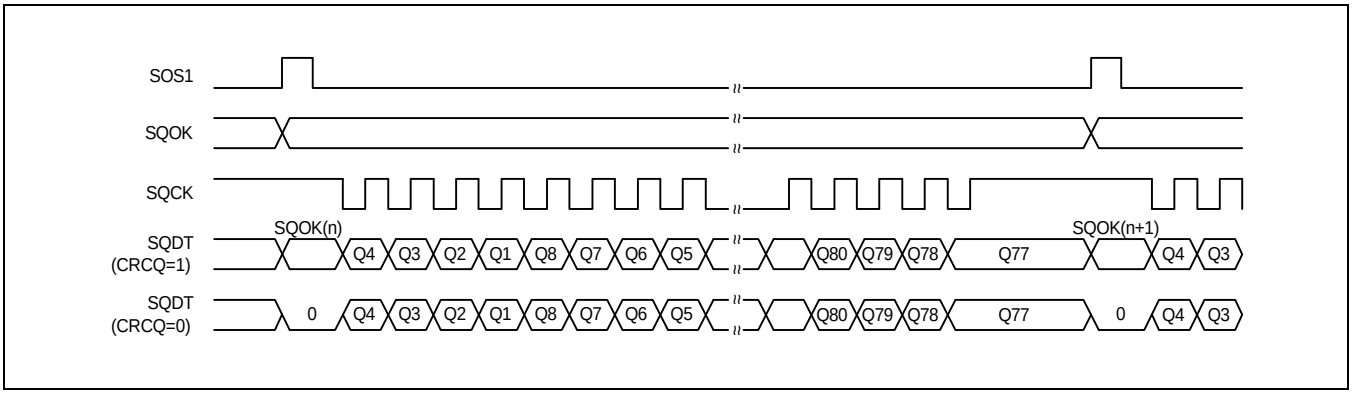
Frame sync may be detected in data besides that of frame sync or omitted due to effects from disc defects or jitters etc. In such cases, frame sync must be protected and inserted. A window must be made according to the $92 command register's WSEL[1:0] to protect frame sync. The data that enter this frame syn is the valid data and the frame sync that exits this window is ignored. If frame sync is not detected in the frame sync protection window, the frame sync made in the internal counter is inserted. If frame sync is inserted continuously to reach the number of frames specified by FSEL[1:0] of the $92 command register, the frame sync protection window is ignored as ULKFS becomes 'H' and the following frame sync detected is immediately accepted. If the frame sync is accepted, ULKFS signal becomes "L" to accept the frame sync detected in the window.

SUBCODE

The subcode sync signal SOS1 is detected in the subcode sync block. After SO is detected, S1 is detected after one frame passes. At this time, SO+S1 signal is output through the SOS1 terminal, and SOS1 signal is output through the SBDT terminal when the SOS1 signal is ' H'. Of the data input to the EFMI terminal, 14-bit subcode data is EFM demodulated, synchronized with the WFCK signal to become 8-bit (P, Q, R, S, T, U, V, W) subcode data and output as SBDT through the SBCK clock. Of the 8 subcode data, only Q data is selected and saved in 80 shift registers using the WFCK signal.

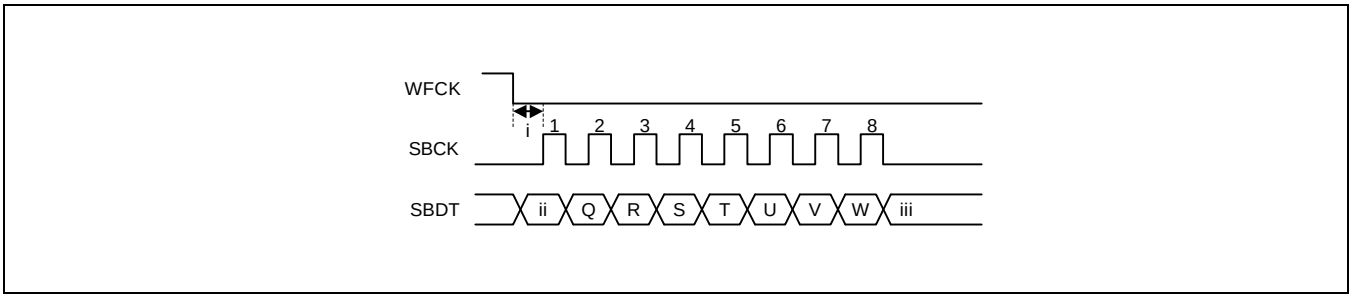
The CRC results of the stored data are synchronized to the S0S1 positive edge and output through the SQOK. If the CRC results are error, 'L' is output to the SQOK terminal and, if not, 'H' is output. If CRCQ's $93 command register is 'H', CRC results are output through the SQDT terminal from the interval that SOS1 is 'H' to the negative edge of SQCK. The following illustrates the timing diagram of the subcode block.

SQCK, SQDT, S0S1 Timing Relationship



NOTE: If CRCQ of the subcode-Q data is 'H', SQOK signal is output through SQDT according to the SQCK signal and, if CRCQ is 'L', SQOK signal is not output through SQDT.

SBDT, SBCK Timing Relationship



i. SBCK is set to 'L' for approximately 10us after WFCK becomes negative edge.

ii. If SOS1 is 'L', subcode P is output but , if SOS1 is 'H', SOS1 is output.

iii. If more than 7 pulses are input to the SBCK terminal, subcode data P, Q, R, S, T, U, V, W data are output repeatedly.

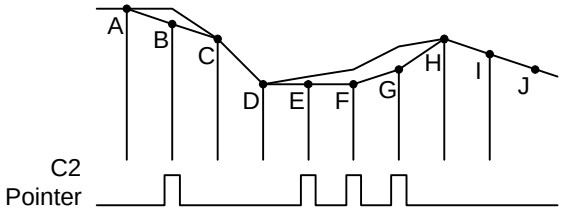
ECC (ERROR CORRECTION CODE)

If the data on the disc is damaged, the ECC (Error Correction Code) block is used to correct data. The CIRC (Cross Interleaved Reed-Solomon Code) is used to correct to 2 errors for C1 (32, 28) and 4 erasures for C2 (28, 24). For error correction, the data is processed in 1 symbol of 8-bit. Furthermore, the ECC block has the pointer function which generates the C1 pointer for C1 correction and C2 pointer for C2 correction. C1 and C2 pointers output flags for ECC processed data to indicate that the data has error. This flag signal is input to the º¸Ł block and used to process the error data. The error correction results can be monitored through MNT3-MNTO terminals. (Related Command Register: $A9, TALK[2:0])

Mode	MNT3	MNT2	MNT1	MNT0	Comment
	ECFL3	ECFL2	ECFL1	ECFL0	
C10 error	0	0	0	0	C1 flag = reset
C11 error	0	0	1	0	C1 flag = reset
C12 error	0	1	0	0	C1 flag = set/reset
C1 correction impossible	1	0	0	0	C1 flag = set
C20 error	0	0	0	1	C2 flag = reset
C21 error	0	0	1	1	C2 flag = reset
C22 error	0	1	0	1	C2 flag = reset
C23 error	0	1	1	1	C2 flag = reset
C24 error	1	0	0		C2 flag = reset
C2 correction impossible 1	1	0	1	1	C2 flag = set
C2 correction impossible 2	1	1	0	1	Copy C1 flag

INTERPOLATION

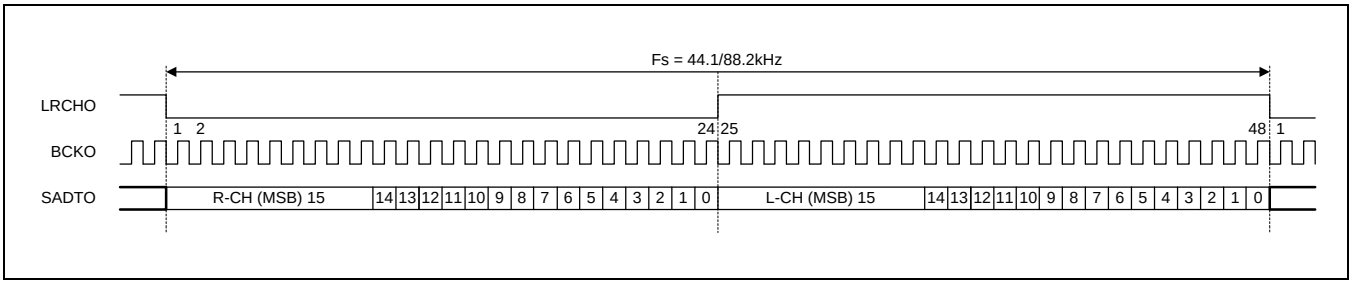
When a burst error is generated on the disc, there are cases when the data cannot be corrected even with the ECC process. The interpolator block uses the ECC'S C2 pointer to interpolate the data. The audio data is input for L/R-ch in 8-bit C2 point, lower data 8-bit, and upper data 8-bit order, respectively, to the data bus. If C2PO terminal is 'H' and there is only one error, the average value is interpolated, but, if there are 3 continuous errors, all values are hold interpolated. If LRCK is 'L' for one LRCK cycle, R-ch data is output, and, if 'H', L-ch is output. The timing clock in the interpolator block is shown below.



B: Average value interpolation
F = E = D: All value hold interpolation
G: Average value interpolation

SERIAL AUDIO DATA INTERFACE

Converts the 16-bit parallel data sent by the interpolation block to serial data. S5L9290X supports the following serial audio data format. The LRCK frequency for 1X is 44.1kHz and 2X is 88.3kHz.



MUTE & ATTENUATION

The mute signal can be accepted in two ways.

- When mute port (pin #: 44) is "H"
- When $91 command register's D7 bit is "H"

The audio data is either muted or reduced based on the mute signal and ATTN signal of the $91 command register.

Zero Cross Mute

After ZCMT of the $91 command register is set to 'H', and the mute signal becomes 'H', and the audio data top 6-bit all are either 'L' or 'H', the audio data is muted.

Mute

When ZCMT of $91 command register is 'L' and the mute signal becomes 'H', the audio data is muted.

Attenuation

The signal is reduced by the ATTN of $91 command register and mute signals.

ATTN	MUTE	Degree of Attenuation [dB]
0	0	0
0	1	-∞
1	0	-12
1	1	-12

Digital Attenuation

By referencing command register $5D, 2^6 = 64 attenuation levels can be controlled. When the reset signal becomes 'L', the attenuation level is initialized to 0dB.

$$Gain = 20 \times \log \frac{Dattn}{64}$$

Soft Mute

When the digital attenuation level is controlled from 0dB to -∞dB, the soft mute function can be configured.

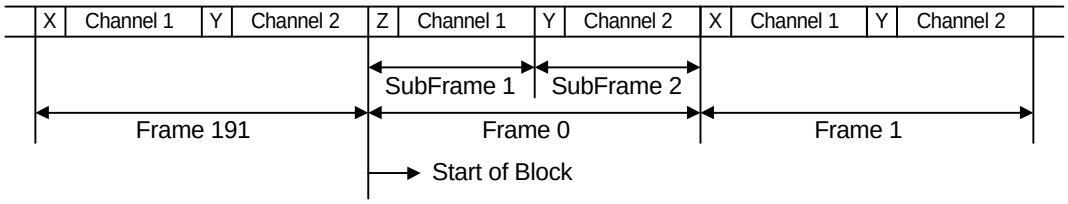
DAC Mute

When the $91 command register's DAC_MUTE is "H", only the DAC block is muted.

DIGITAL AUDIO OUT

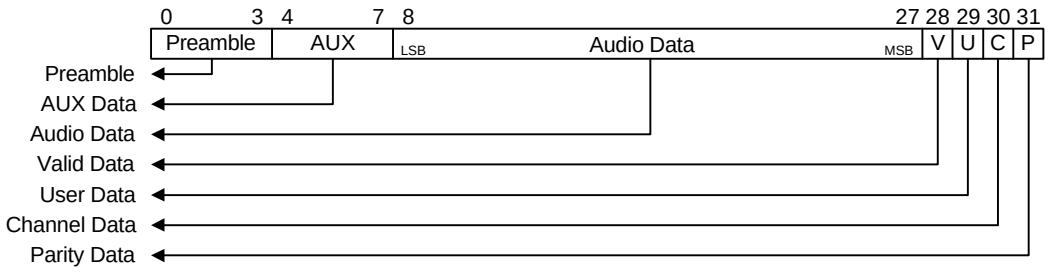
This digital audio out block outputs 2-channel and 16-bit data to another digital set in serial format based on the digital audio interface format. The advantage of this interface method is that communication is possible with only one pin, that is, additions such as a separate clock are not required.

CD digital audio interface format



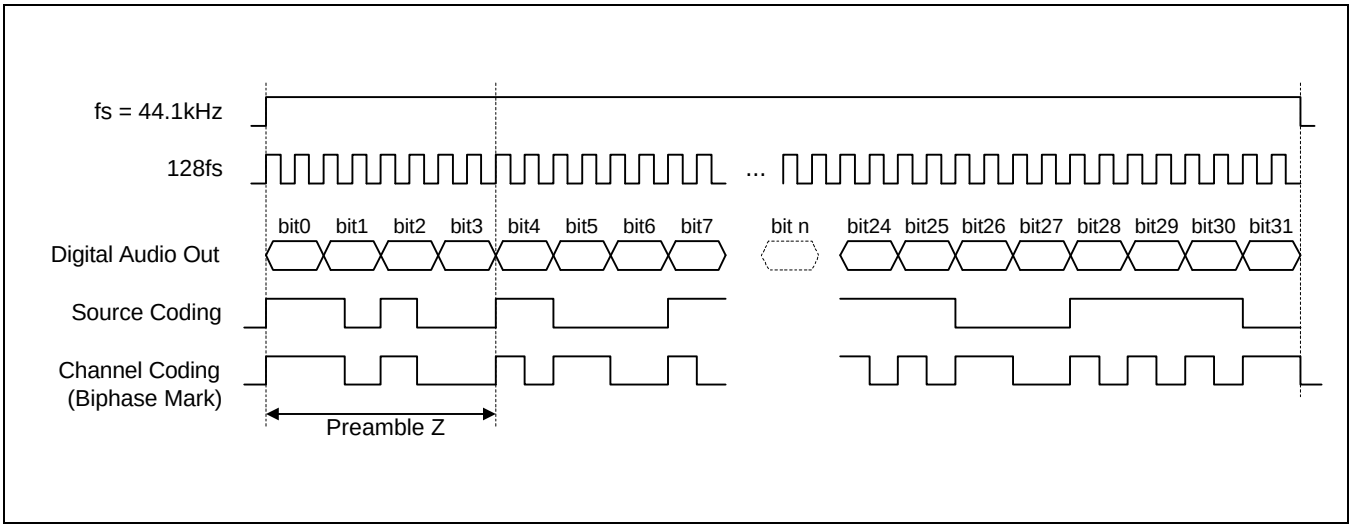
1. 1 block = 192 frame
2. 1 frame = 2 subframe
3. Frame 0, channel 1
   - Block sync preamble, Z included Ch.1 format
4. Frame 1, channel 1-frame 191, channel 1
   - Ch.1 sync preamble, X included Ch.1 format

Frame 0, channel 2-frame 191, channel 2
- Ch.2 sync preamble, Y included Ch.2 format



Digital Audio Interface Timing Chart

Each subframe is composed of 32 time slots, and audio data is included in the subframe. Two subframes make one frame, which has both left and right stereo signal components; 192 frames make one block, which is in the control bit data unit.



SUBFRAME FORMAT

Preamble (4 bits):

The preamble has each subframe and block sync data. The preamble is not converted to biphase signal to maintain the inherent characteristic of the sync. On the other hand, it starts with the values opposite the phase 1 values of all the. The preamble requires three patterns, that is, a pattern to distinguish between and right and patterns that indicate start of the block. These patterns are shown.

Preceding State	**0**	**1**	
	Channel Coding		
"X"	11100010	00011101	Subframe 1
"Y"	11100100	00011011	Subframe 2
"Z"	11101000	00010111	Subframe 1 and block start

Preamble 'X' is the channel 1 sync; preamble 'Y' is the channel 2 sync; and preamble 3 is to show the start sync of the block. The reason that there are 2 sync patterns for preamble is that the value reverses according to the phase of the previous data.

AUX (4 bits):

Auxiliary data area.

Audio data (20 bits):

Although the audio data resolution for the CD transmitted to digital out is usually 16 bits, it can also be transmitted as 20 bits or 24 when AUX is to be included. This area is LSB first.

Validity bit (1 bit):

If the audio sample word can be converted to analog audio signal, the validity bit to '1' and, if not, to '0'. For the CD, set it to '0'.

User data (1 bit):

This domain is used to transmit the subcode data for CD.

Control status data (1 bit):

Data is input for each subframe, and 192 subframes must be gathered to make one control data. This domain has both the consumer mode and professional mode, of which S5L9288X the consumer mode. The control status data for CD has the following meaning.

Parity data (1 bit):

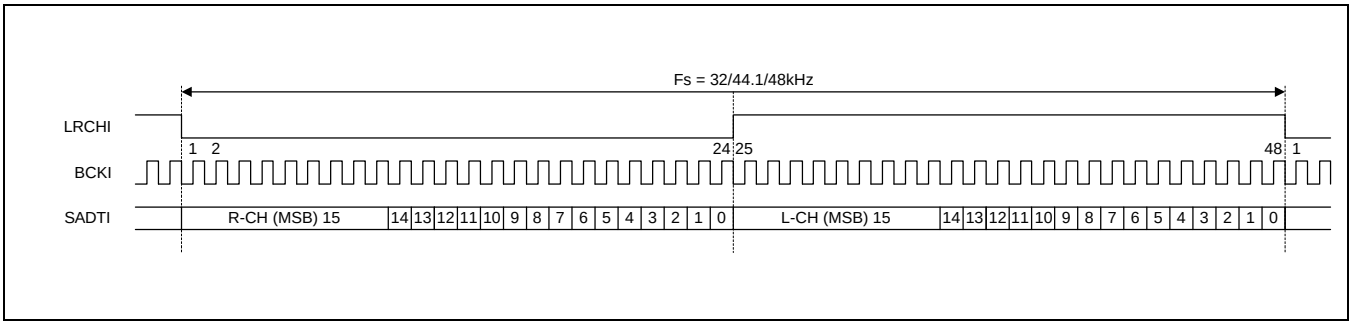
Use even parity

Bit	Control Status Data	Default Value
0	0 : Consumer use 1 : Professional use	0
1	0 : Normal audio mode 1 : Non-audio mode	0
2	0 : Copy prohibit 1 : Copy permit	0/1
3	0 : No pre-emphasis 1 : Pre-emphasis	0/1
4	Reserved	0
5	0 : 2-channel 1 : 4-channel	0
6 - 7	Mode 00 : mode 0 other : Reserved	00
8 - 15	Category code 10000000 : 2-channel CD player	10000000
16 - 19	Source number	0000
20 - 23	Channel number	0000
24 - 27	Sampling rate 0000 : 44.1kHz 0100 : 48kHz 1100 : 32kHz other : reserved	-
28 - 29	Clock Accuracy 00 : Normal accuracy 10 : High accuracy 01 : Variable speed	-
30 - 191	Dont care	all zero

SIGMA-DELTA STEREO DAC

As a digital-to-analog converter that uses the $\sum \Delta$ modulation, the DAC installed in S5L9290X is composed of the digital attenuation, de-emphasis filter, FIR filter, SINC filter, digital sigma-delta modulator, analog post-filter, anti-Image filter etc. Normal input/output characteristics exist at 20kHz. It has SNR (Signal to Noise Ratio) above 90dB.

Timing Chart



32/44.1/48kHz Sampling Frequency (Fs) Support

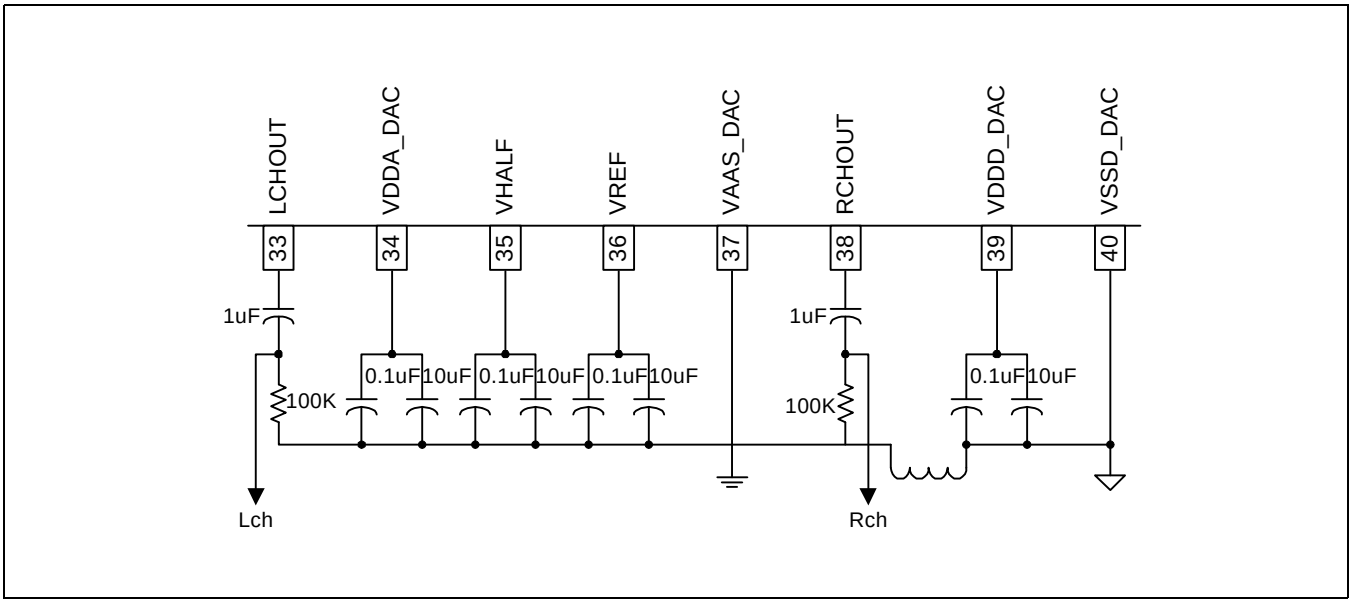
If the DAC master clock is applied to 384 $\times$ Fs cycle, it supports 3 sampling frequencies.

If the command register $94's MSCKSW is "H" and command register $A9's RFCK_OEN is "L", the external master clock can be applied to the RFCK terminal.

X1, X2 Speed Support

If the command register $93's DFCK is set to "H", the internal data input rate becomes 2*Fs and the speed becomes 2X.

Application Circuit



DIGITAL CLV SERVO

This block controls the spindle motor speed by using RFCK and WFCK data to generate the control .Digital CLV Servo control related Command Registers are $93, $94, and $98 — $9E.

Forward (Kick) Mode

Mode ($99) that rotates the spindle motor in forward direction.

SMDP	SMDS	SMEF	SMON
H	Hi-Z	L	H

Reverse (Brake) Mode

Mode ($99) that rotates the spindle motor in the reverse direction.

SMDP	SMDS	SMEF	SMON
L	Hi-Z	L	H

Stop Mode

Mode ($99) that stops the spindle motor.

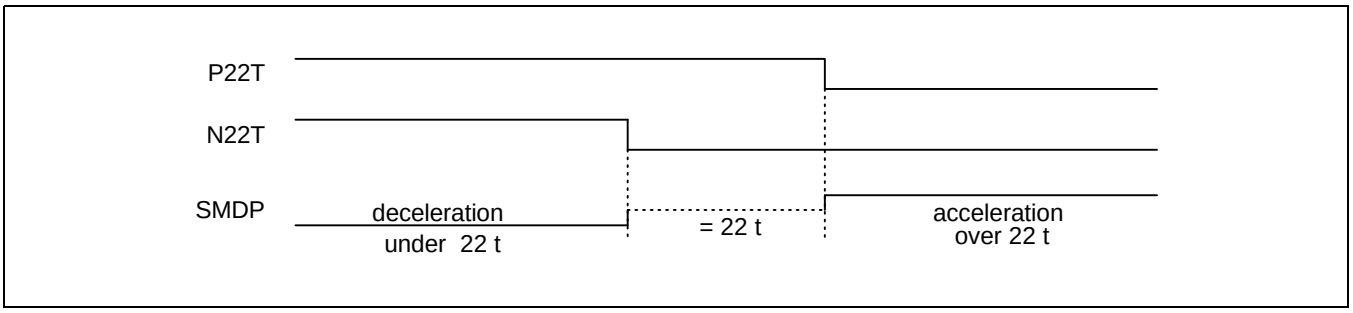
SMDP	SMDS	SMEF	SMON
L	Hi-Z	L	L

Speed (CLV-S) Mode ($99)

Controls the spindle motor during a track jump or if the EFM phase is unlocked.
Although the pulse width of the frame sync signal detected from the EFM signal is exactly 22T in PLCK cycle (T), it can be greater or less than 22T depending on the player status.
WB and WP of the command register $98 are used to control the frame sync detection cycle.

SMDP	SMDS	SMEF	SMON
L : deceleration H : acceleration Hi-Z : remain	Hi-Z	L	H

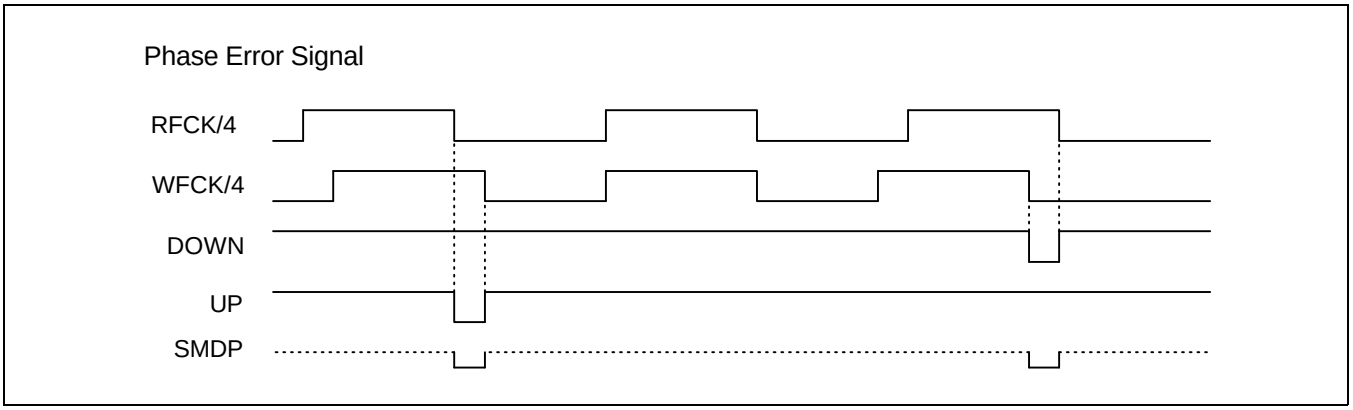
Detected Frame Sync Pulse Width	SMDP	Comment
≤ 21T = 22T ≥ 23T	L (deceleration) Hi-Z (remain) H (acceleration)	If the command Register $98's GAIN is 'L', the SMDP output is output after it has been attentuated by -12dB, but if 'H', it is output without being attentuated.



<SMDP output waveform in Speed (CLV-S) Mode>

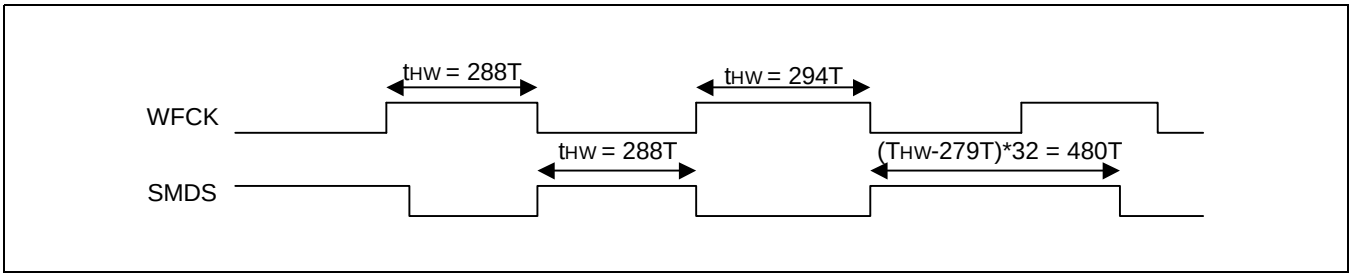
Phase (CLV-P) Mode (Command Register : $99)

As the EFM signal phase control mode, this mode precisely controls the spindle motor rotation speed.
Two methods of control are Phase control and Frequency control and the two signals produced, are sent to the SMDP and SMDS, respectively.
NCLV of the command register $93 can be used to change the reference clock, which is used in phase control. The phase control signal is sent to SMDP and its waveform is shown below.



<SMDP output waveform in the Phase (CLV-P) Mode >

If the system clock and C4M cycles are T and WFCK's width, 'H', is t_{HW}, SMDS outputs 'H' starting from WFCK's negative edge for (tHW - rise_mtval) × SGAIN and then falls to 'L'. Here, the rise_mtval and SGAIN values can be set through command register $9B.



< SMDS output waveform in Phase (CLV-P) Mode: SGAIN = 32, rise_mtval = 279 >

XPHSP (CLV-A) Mode (Command Register : $99)

In this normal operation mode, the speed mode and phase mode are change alternately by the lock signal. After the LKFS signal generated by the frame sync block is sampled in WFCK/16 cycles and is detected to be 'H', the phase mode executes and, if it is detected as 'L' eight consecutive times, the speed mode automatically executes.

LOCK generation

If the LKFS signal remains at 'L' for the frame time, provided by Micom Command $99's UNLOCK[1:0], or for less, LOCK remains at 'H'. However, if it remains at 'L' for more than the given frame, the LOCK changes to 'L'. The time in LOCK is the same for 1X and 2X speed.

Additional Functions ($9B's POS must be set to = 'H')

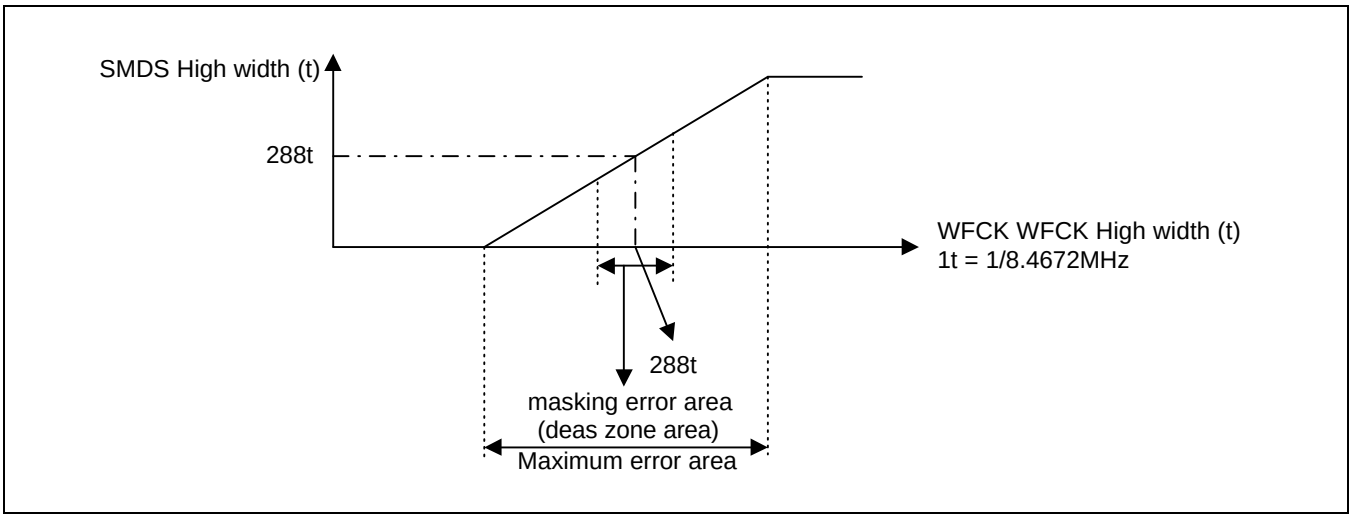
1) SMDS masking

This function prevents sensitive CLV servo response to small frequency error changes.
If the SME of $9A is set to 'H', it operates in the SMDS masking mode (dead zone enable).
The SML[1:0] masking range of $9B is set, and, if $9A's SMM bit is 'H', SML value becomes the absolute value of the masking range, set by 9D'h SMOFFSET[3:0], but if 'L', then the value is set to the one shown in the table below. If SMDS frequency error, that is, WFCK high width is within the masking range, the SMDS output is PWM of 50:50 or Hi-Z is output. (Determined by $9A's STRIO)
If SMDS masking occurs, SMDP output is masked automatically and Hi-Z is output.

Command order : $9B(SML) → $9D(SMOFFSET) → $9A (SME, SMM)

SML[1:0]	masking error range (SML = 'L')
00	0 %
01	± 6.25 %
10	± 12.5 %
11	± 25 %

< SML[1:0] setting >



< Dead Zone Area >

SMDP masking

When the SMDS masking is enabled, the SMDP output is automatically masked in the dead zone area. There are two modes for masking only the SMDP without masking the SMDS.
In the first mode, if $9A's SME is set to 'L' and PME is set to 'H', the SMDP masking mode operates. At this time, if the phase error is greater than ± 50% or ± 25% of the WFCK frequency error (determined by $9B's PML), SMDP output is masked. That is, the output is Hi-Z.
This is to reduce the phase error effect at the state in which the frequency error is not sufficiently small. In the second mode, after setting SME and PME of $9A, PCEN of $99 can be used to set SMDP masking. In this case, if PCEN of $99 is set to 'H' and WFCK frequency error enters the dead zone area set by SML, the SMDP output is maked to Hi-Z.

Command order : $9B(PML) → $9A(PME), $9B(SML) → $99(PCEN)

CLV emergency mode (ECLV)

When there are events such as a focus drop, an unstable EFM is input and this in turn causes the spindle motor to overload. To prevent such an overload, the Micom notifies the CLV servo of such emergency conditions, and then CLV servo outputs H, Hi-Z and L repeatedly in regular intervals. This is all executed by the micom, which sets the ECLV of $93 to 'H' and changes the CLV mode to CLV-S mode. Then, SMDS outputs Hi-Z and SMDP outputs H, Hi-Z and L repeatedly in an interval determined by ECLV_PD of $93.

ECLV_PD	Comment
1	bottom hold pulse interval
0	peak hold pulse interval

Command order : $93(ECLV, ECLV_PD) → $99(CM3,CM2,CM1,CM0)

Defect response mode

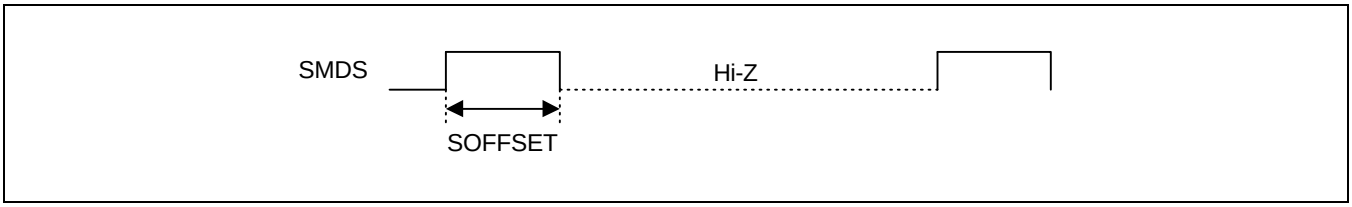
If the EFM enters as'L' for a specific time due to a Scratch or defect, there is no PLL control, which fixes the PLCK to any frequency; this in turn fixes the WFCK and consequently the CLV servo output is fixed in the direction of acceleration or deceleration. In such a case, the final CLV speed can be reduced when normal EFM re-enters. If CLV_DFCT of $A2 is set to 'H', the CLV servo outputs, SMDP and SMDS, can be output as Hi-Z and 50:50, when EFM width is greater than 64t to prevent deceleration or acceleration.

Oversampling output

The SMDS output frequency is 7.35kHz at 1X speed and 14.7kHz at 2X speed. These are within the audio frequency range, so they be used as normal audio output noise source. Therefore, OVSPL of $98 can be set to 'H' and SMDS and SMDP frequencies can be oversampled by four times at 7.35KHz * 4 = 29.4kHz and output. If OVSPLMD of $98 is set to 'H', the SMDS becomes tri-state t output and, if set to 'L', SMDS become a PWM output.

CLV IDLE mode

This mode rotates the spindle motor at a fixed rate regardless of the EFM input.
To operate in the CLV IDLE mode, the $9E's SOFFSET[7:0] value, which represents the SMDS high width, must be set. Furthermore, if $99's CLV_IDLE is set to 'H', the SMDP output becomes Hi-Z, and SMDS outputs High for the duration of SOFFSET set value * 118ns in one cycle and outputs Hi-Z in the remaining intervals.



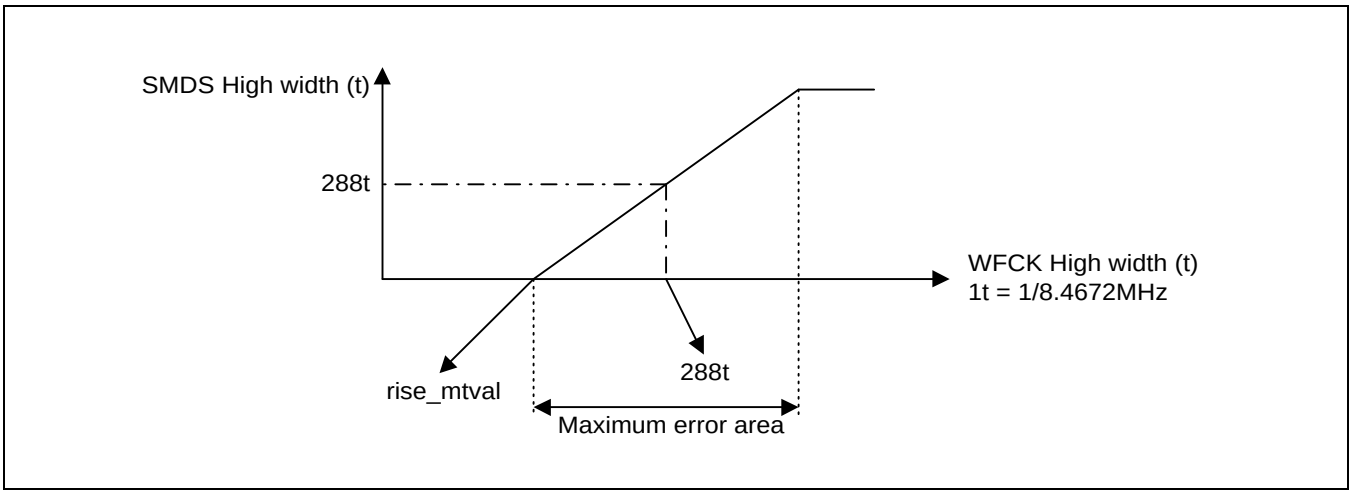
< SMDS output >

SMDS gain control

If the pickup or spindle motor is changed, the entire CLV loop transfer function changes and thus CLV gain must be controlled. The CLV servo is changed to PI controller type; we can assume that the frequency error output SMDS controls the P gain and the phase error output SMDP controls the I gain. SMDS gain can be set to 9B'h SGAIN[2:0] , where gain values of SGAIN are shown below. In terms of a graph, the gain is the slope.

SGAIN[2:0]	Gain Value	rise_mtval
000	1	0
001	2	144
010	4	216
011	8	252
100	16	270
101	32	279
110	64	283
111	128	285

< SMDS gain setting >



< SMDS gain vs SMDS output >

There is an additional feature which allows the addition of an offset to WFCK frequency error for output. If $9D's SPLUS is set to 'H' and $9E's SOFFSET[7:0] is set, the SOFFSET value is added to the frequency error, and the product of this value and the gain is output to SMDS.

SMDP gain control

The 9B'h POS must be set to 'H' for SMDP gain control. Furthermore, SMDP gain must be set to $9A's PGAIN[1:0]. The clock resolution, which measures WFCK and RFCK's phase error, must be set to $9A's PKSEL.

PGAIN[1:0]	gain
00	1
01	1/2
10	1/4
11	2

<SMDP gain setting >

PKSEL[1:0]	frequency
00	clk4M/2
01	clk4M/4
10	clk4M/8
11	clk4M/16

< Phase error resolution clock setting >

If POFFSET[7] is 'H', the value is subtracted and, if 'L', added. .

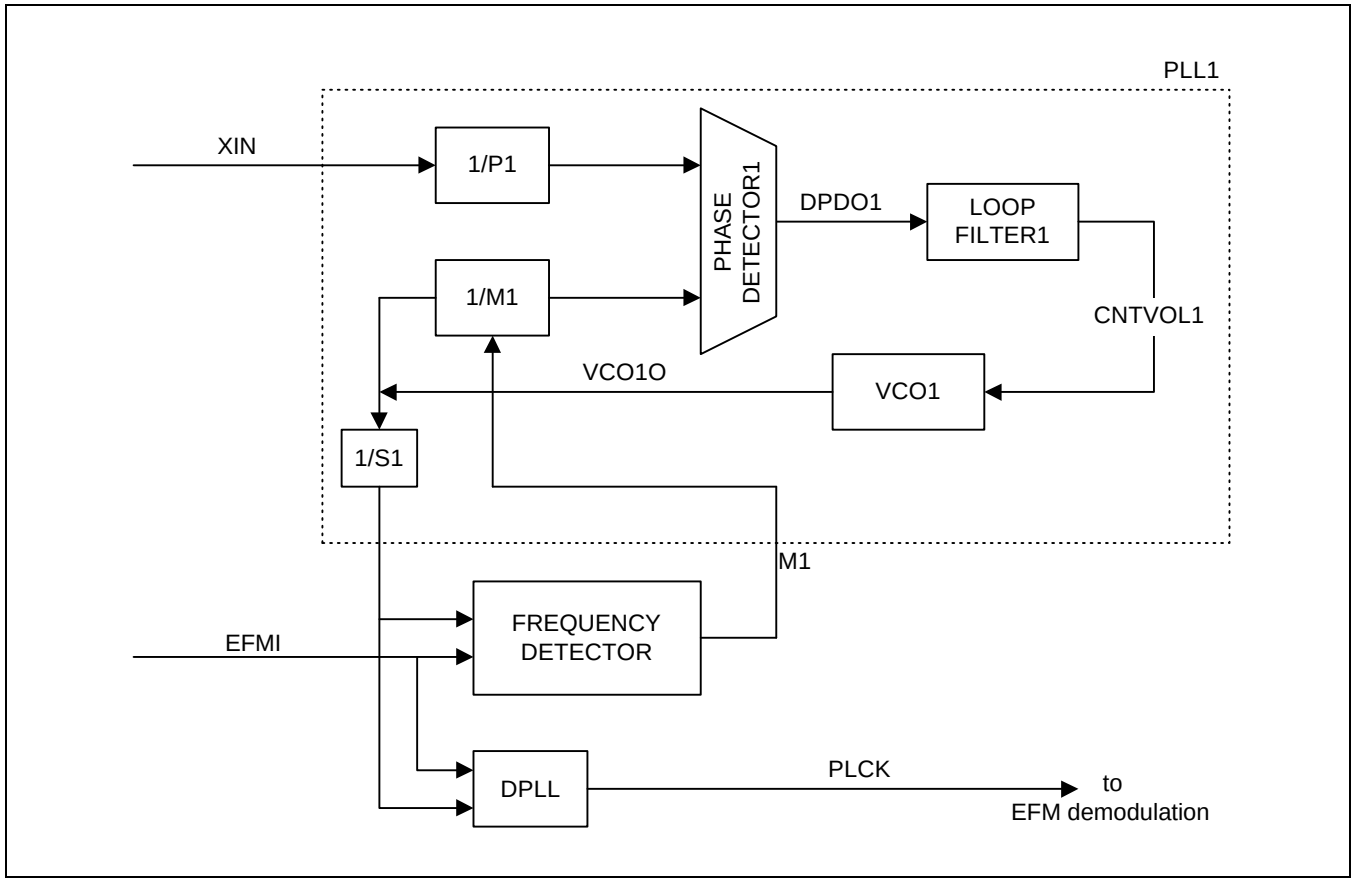
SMDS output Mode

If $9A's STRIO is set to 'H', the SMDS is output in tri-state (H, Hi-Z, L) states in phase mode.
If $9D's SDD is set to 'H', the SMDS outputs as Hi-Z in phase mode if the WFCK frequency error is a deceleration error. Even if SMDS is output as Hi-Z, this mode can reduce the power consumption by utilizing the principle of deceleration due to motor friction.

DIGITAL PLL

Essentially uses the existing digital PLL configuration while changing the frequency of the frequency synthesizer, which suppliew the DPLL clock, according to the EFM signal bit rate to allow wide capture range PLL.

Wide capture range PLL is generated the SRAM jitter by changeing the in/output rate of SRAM buffer and can selected the jitterfree mode to prevent the SRAM jitter.



< Block Diagram >

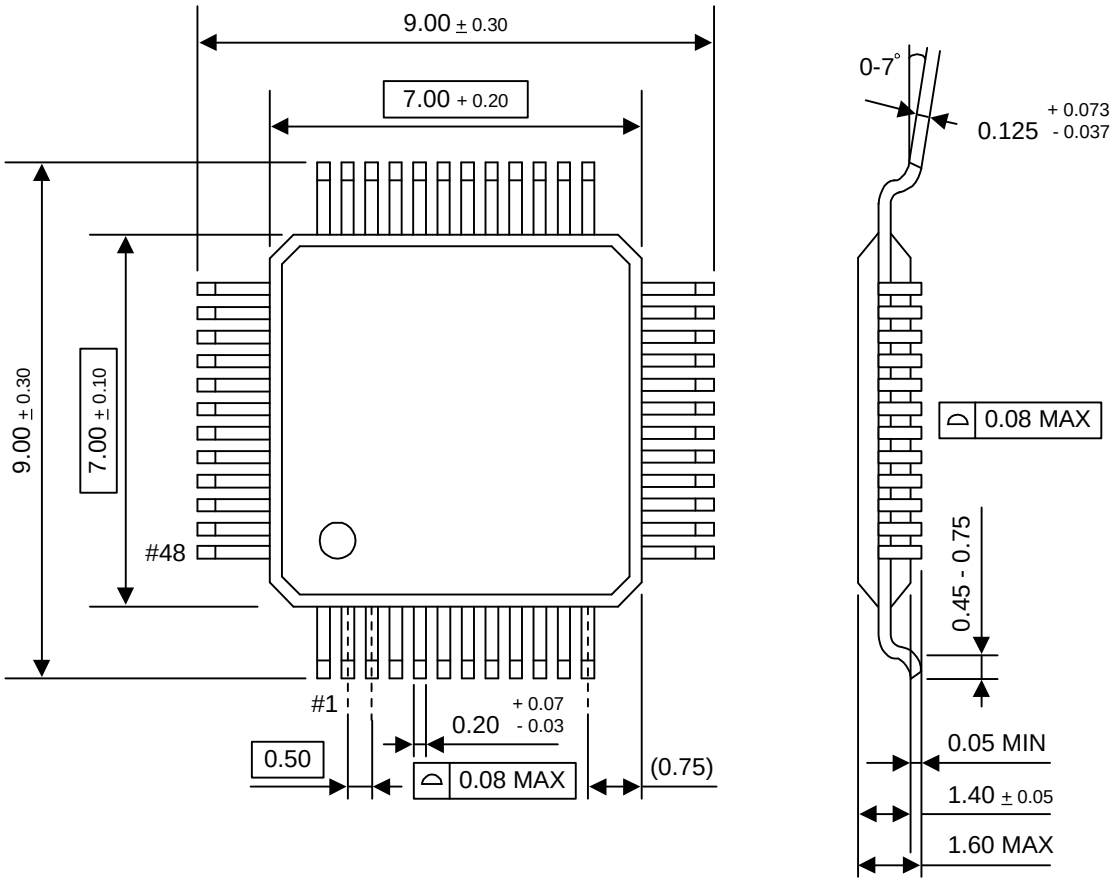
PLL1 is the frequency synthesizer to supply the reference clock in DPLL and receives the crystal input (16.9344MHz) to generate a clock with Xtimes of PLCK.

The next is frequency equation of frequency synthesizer and is changed the divider value automally by sekect the times

$$Font = Fin \times \frac{m}{p \times s}$$

Fin: input frequency, Font: output frequecy
p: ore-divider (=DIVP+2), m: main-divider (DIVM+8), s: port-scalor (2DIVS)

PACKAGE DIMENSION



NOTE: Dimensions are in millimeters.