SE6100

ASK Transceiver IC

1 Short Description

The SE6100 is a single chip ASK (Amplitude Shift Key) transceiver IC. It is designed to operate in low power µC-controlled and stand alone applications with half duplex data transmission. The unsymmetrical antenna input and output are separated for applications with apart transmission and receiving antenna. The SE6100 is suitable for European or North American ISM band applications. Integrated functions as stand by mode, low bat control, RSSI output, level detector, locked loop detection, and clock output for µC offer features for universal applications.

2 Features

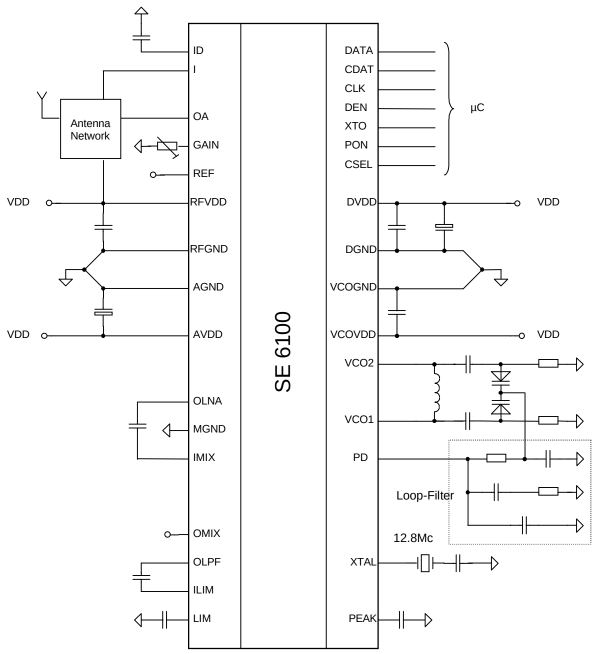
- Single chip ASK Transceiver
- Wide frequency range (200 .. 435 MHz)
- Low voltage operation (2.3 .. 3.6 V)
- Low power consumption
- PLL (25 kHz/ 50 kHz channel space, 64/32 channels available)
- Adjustable output power
- High sensitivity
- Data rates up to 9600 bps
- Stand alone application available
- Automotive temperature range
- TQFP32 Package and Die

3 Applications

- Intelligent keyless entry
- Security systems
- Remote control systems
- Communication systems
- Medical applications

Typical Application

Low power data transceiver using SE6100



4 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances.

Symbol	Parameter	Min	Max	Unit
Tj	Junction Temperature	-55	150	°C
Tstg	Storage Temperature Range	-55	150	°C
V_{DD}	Supply Voltage	-0.5	5.5	V
	Voltage at any Pin (except IMIX, OLNA, I1, OA, VCO1 VCO2)	-0.5	VDD+0.5	V
	Voltage at Pins IMIX, OLNA, I1, OA, VCO1 VCO2	-0.5	5.5	V

5 Electrical Characteristics

5.1 Operational Range

Within the operational range the IC operates as described in the circuit description. The DC and AC limits are not guaranteed.

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	2.3	3.6	V
f	frequency range	200	435	MHz
$N_{CHANNEL}$	Number of channels available	32	64	-
T_A	Ambient Temperature	-25	85	°C

5.2 DC Characteristics

Supply voltage: V_{DD} = 3.0 V; Ambient temperature: T_A = 27°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD} TX	Supply Current (TX Mode)			4.8 [1)]	5.6	mA
I_{DD} RX	Supply Current (RX Mode)			4.6	5.4	mA
I_{DD} 0	Supply Current (Sleep Mode)			0.6	1	µA
V_{REF}	Reference Voltage	I_{load}=200µA	1.05	1.14	1.25	V
V_{IH}	Data Input Voltage - logic high	[3)]	$0.7*V_{DD}$	V_{DD}	V_{DD}+0.5	V
V_{IL}	Data Input Voltage - logic low	[3)]	-0.5	0	0.3* VDD	V
I_{IH}	Data Input Current - logic high	[3)]		0	1	µA
$-I_{IL}$	Data Input Current - logic low	[3)]		0	1	µA
V_{OH}	Output Voltage - logic high	[4)]	$0.7*V_{DD}$	V_{DD}	V_{DD}	V
V_{OL}	Output Voltage - logic low	[4)]	0	0	$0.3* V_{DD}$	V
I_{OH}	Output Current - logic high	[4)]	50	>1000		µA
$-I_{OL}$	Output Current - logic low	[4)]	50	>1000		µA

[1)] R_{GAIN} = 0Ω, DataRate = 5kBit, DutyCycle = 50%
[2)] R_{GAIN} = 50Ω||100p, DataRate =5kBit, DutyCycle=50%
[3)] Pins CSEL, PON, DATA, CDAT, CLK, DEN, XTO
[4)] Pins DATA, XTO

5.3 AC Characteristics

Supply voltage: V_{DD} = 3.0 V; Ambient temperature: T_A = 27°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
g_{RX}	RX gain (LNA+Mixer)		33	38	44	dB
g_{RX}	RX gain attenuation	LNAGAIN =high	-23	-20	-18	dB
	Sensitivity	BW=25kHz		-102 [2)] -95 [4)]		dBm
BW1	Bandwidth LPF	BW=low		75		kHz
BW2	Bandwidth LPF	BW=high		38		kHz
DR1	Data Rate	DR=low			9600	bps
DR2	Data Rate	DR=high			4800	bps
$t_{ON\ RX}$	Receiver power on settling time	CHCP=low		18	25	ms
$t_{ON\ TX}$	Transmitter power on settling time	CHCP=low		18	25	ms
$t_{SET\ PLL}$	PLL settling Time (e.g. after channel change)	CHCP=low		4	10	ms
$\lvert I_{PD}\rvert$	Phase Detector Output Current	CHCP=low	20	38	60	µA
$\lvert I_{PD}\rvert$	Phase Detector Output Current	CHCP=high	40	77	120	µA
f_{XTAL}	Reference Oscillator Frequency Range	Depends on used Crystal	8	12.8	13	MHz
	Osc. Temperature Stability	Without influence of crystal	-5	-	5	ppm
$I_{RF\ OUT}$	RF Output Current (Transmit Mode)	[3)]	0.9	1.4		mA
P_A	Output Power (Transmitting Mode)		0.3 [3)]	0.5 [3)]		mW

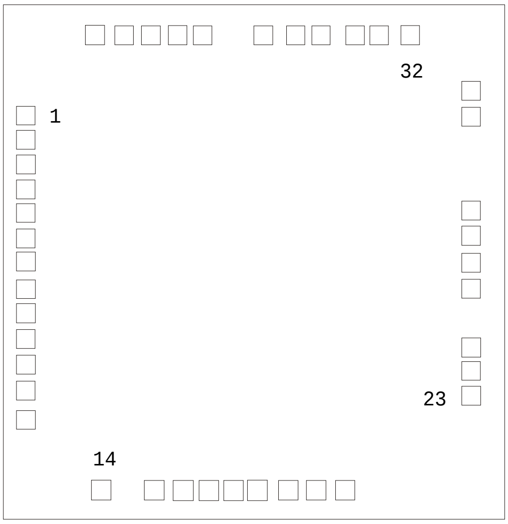
[2)] transformer circuit

[3)] $R_{GAIN} = 0\Omega$

[4)] v_{imin} at the IC ($R_{SOURCE} = 50\Omega$)

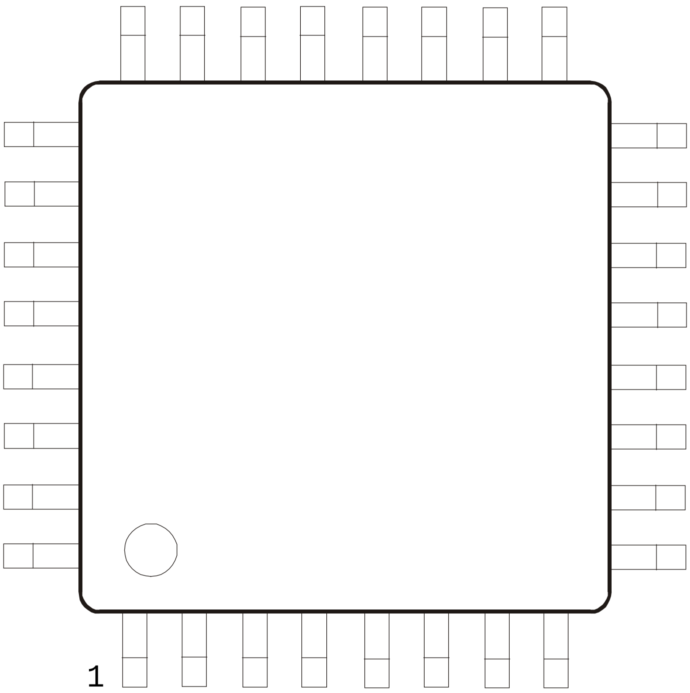
6 Package Outline

6.1 Pad-Layout



Chip size: 2.53 mm x 2.59 mm
Chip thickness: 340 µm

6.2 PIN-Layout



Housing type**:** TQFP 32

6.3 Pad Coordinates, DIE

Pad-No.	Name	X	Y	Pad X	Pad Y	Remarks	Side info
1	IMIX	-1176.6	738.0	90.0	75.0		left
2	RFVDD	-1176.6	613.0	90.0	75.0	Optional	left
3	RFVDD	-1176.6	488.0	90.0	75.0		left
4	OLNA	-1176.6	363.0	90.0	75.0		left
5	ID	-1176.6	238.0	90.0	75.0		left
6	I	-1176.6	113.0	90.0	75.0		left
7	RFGND	-1176.6	-12.0	90.0	75.0		left
8	RFGND	-1176.6	-137.0	90.0	75.0		left
9	OA	-1176.6	-262.0	90.0	75.0		left
10	GAIN	-1176.6	-387.0	90.0	75.0		left
11	GAIN	-1176.6	-512.0	90.0	75.0		left
12	(-)	-1176.6	-664.4	90.0	75.0	Spare pad, don't connect	left
13	(-)	-1176.6	-802.5	90.0	75.0	Spare pad, don't connect	left
14	REF	-819.8	-1207.4	75.0	90.0		bottom
15	CLK/CS2	-528.7	-1207.4	75.0	90.0		bottom
16	CDAT/CS1	-391.8	-1207.4	75.0	90.0		bottom
17	DEN/NSEL	-259.1	-1207.4	75.0	90.0		bottom
18	DATA	-124.8	-1207.4	75.0	90.0		bottom
19	XTO/SEL	12.8	-1207.4	75.0	90.0		bottom
20	CSEL	148.2	-1207.1	75.0	90.3		bottom
21	PON	296.0	-1207.4	75.0	90.0		bottom
22	MDO	439.9	-1207.5	75.0	90.9	Test pad, don't connect	bottom
23	XTAL	1176.7	-724.1	90.0	75.6		right
24	DGND	1176.7	-599.2	90.0	75.3		right
25	DVDD	1176.7	-474.4	90.0	75.0		right
26	VCO1	1176.7	-181.0	90.0	75.3		right
27	VCO2	1176.7	-56.3	90.0	75.0		right
28	VCOGND	1176.7	93.5	90.0	75.3		right
29	VCOVDD	1176.7	218.8	90.0	75.0		right
30	R2	1176.7	690.1	90.0	75.3	Test pad, don't connect	right
31	PD	1176.7	847.4	90.0	75.0		right
32	PEAK	792.3	1207.2	75.0	90.3		top
33	AVDD	621.0	1207.5	75.0	90.0		top
34	AVDD	496.0	1207.2	75.0	90.3		top
35	LIM	330.9	1207.5	75.0	90.0		top
36	ILIM	185.8	1207.2	75.0	90.3		top
37	OLPF	33.5	1207.5	75.0	90.0		top
38	AGND	-273.5	1207.5	75.0	90.0		top
39	AGND	-398.5	1207.5	75.0	90.0		top
40	ILPF	-552.5	1207.5	75.0	90.0		top
41	OMIX	-677.5	1207.5	75.0	90.0		top
42	MGND	-822.1	1207.5	75.0	90.0		top

The coordinates are related to the die centre of the die (0, 0). The pad coordinates represent the pad centre.

Gross Die Size: 2.72 x 2.78 mm² = 7.56 mm²   Scribe Line Width: 190µm
Net Die Size: 2.53 x 2.59 mm² = 6.55 mm²   Die thickness: 340µm

6.4 Device PinOut / package: TQFP32

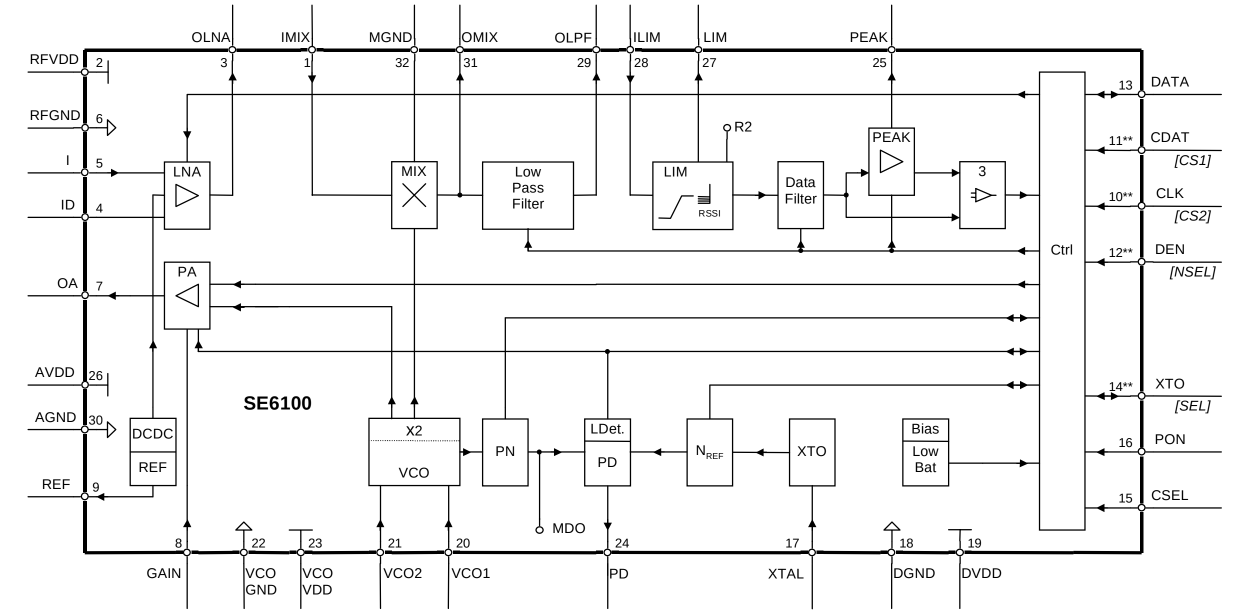
Pin	Pad	Symbol	Description
1	1	IMIX	Mixer Input
2	2,3	RFVDD	RF Supply
3	4	OLNA	Low Noise Amplifier Output
4	5	ID	LNA Input decoupling (emitter)
5	6	I	LNA Input (base)
6	7,8	RFGND	RF Supply Ground
7	9	OA	Power Amplifier Output
8	10,11	GAIN	Gain Adjust (Power Amplifier)
	12		Not used
	13		Not used
9	14	REF	Reference voltage output(for external LNA/Power Amp)
10	15	CLK / CS2 [1]	Shift Register Clock / Channel Selector Bit 2 [1]
11	16	CDAT / CS1 [1]	Serial Input for Control Data Shift Register / Channel Selector Bit 1 [1]
12	17	DEN / NSEL [1]	Control Data Enable / Divider Switch [1]
13	18	DATA	Data-Input/Output
14	19	XTO / SEL [1]	Clock Output for µC / RX/TX Selection [1]
15	20	CSEL	Control Switch
16	21	PON	Power up/down
	22	MDO	Test Pad, do not connect
17	23	XTAL	Crystal-Oscillator Input
18	24	DGND	Digital Supply Ground
19	25	DVDD	Digtal Supply Voltage
20	26	VCO1	Voltage Controlled Oscillator
21	27	VCO2	Voltage Controlled Oscillator
22	28	VCOGND	VCO Supply Ground
23	29	VCOVDD	VCO Supply
	30	R2	Test Pad, do not connect
24	31	PD	Charge Pump Output
25	32	PEAK	Peak Detector Output, RSS / Output
26	33,34	AVDD	Analog Supply Voltage
27	35	LIM	Limiter Decoupling
28	36	ILIM	Limiter Input
29	37	OLPF	Low Pass Filter Output
30	38,39	AGND	Analog Supply Ground
31	40	ILPF	Low Pass Filter Input
	41	OMIX	Mixer Output
32	42	MGND	Mixer Ground

[1] different pin function in case of stand alone mode

ESD protection according to MIL-STD. 883c (minimum 2kV)
except pins IMIX, OLNA, I1, OA, VCO1, VCO2 (minimum 1kV)

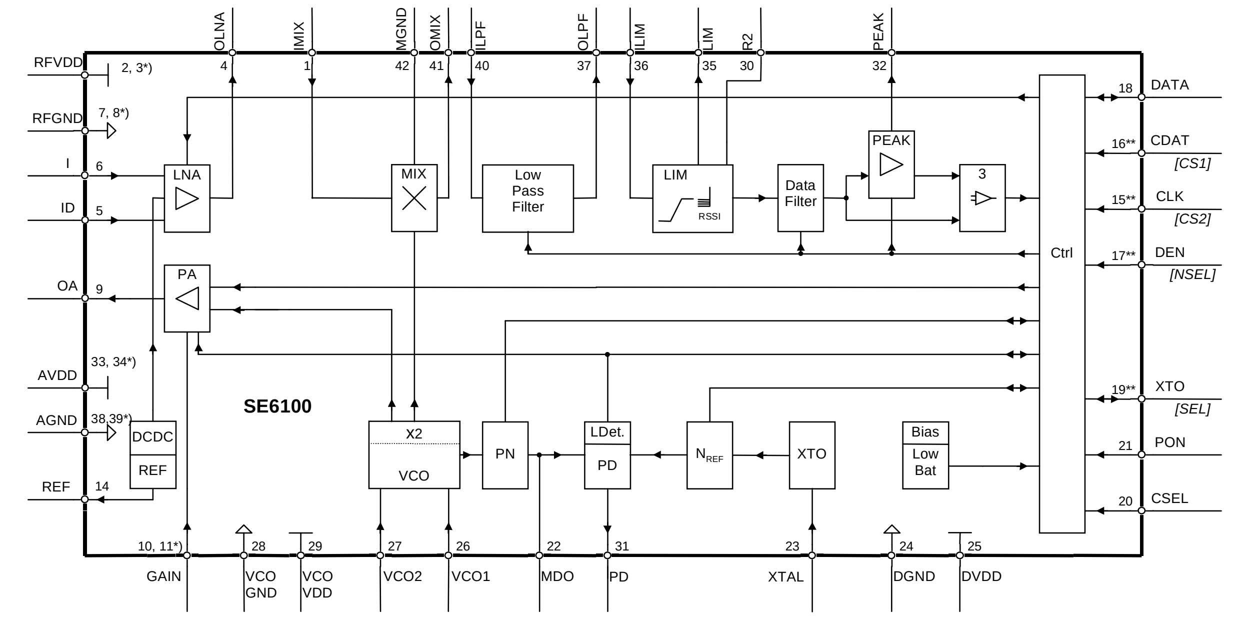
7 Device Block Diagram

TQFP32 (Pin-No.)



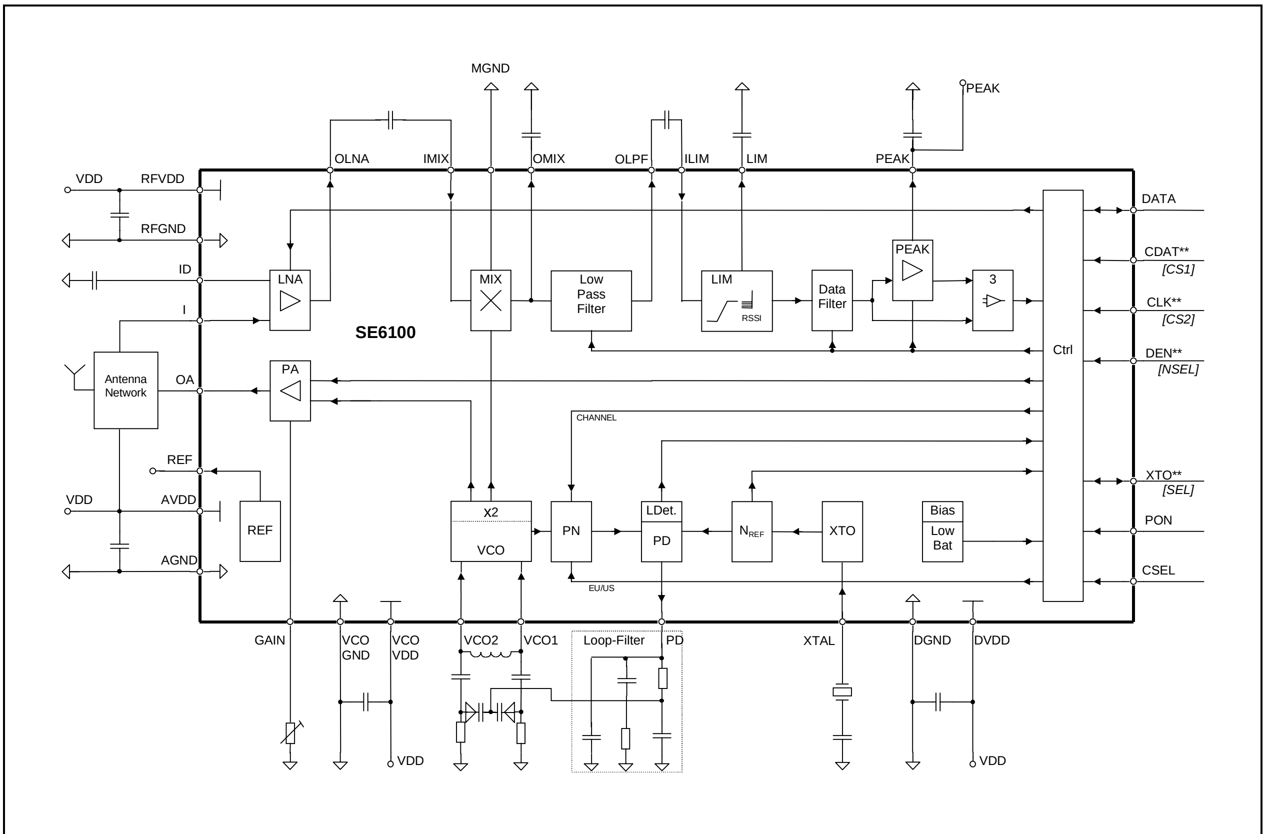
[**] different Pin functions in case of stand alone application

DIE (Pad-No.)



[*] double bonding required
[**] different Pad functions in case of stand alone application

8 Functional Block Diagram



[**] different Pin functions for stand alone application

9 Block by Block Description

- LNA
  Single input and output
  Especially designed for small loop antennas
  Disable feature (for using external LNA)
  Suitable to use the same antenna for receiving and transmitting mode (half duplex)
  full gain: -17dB (depending on external circuitry)
  gain reducing: about 17dB (using the -20dB switch)
  IP3 = +1.3dBm (full gain)
  IP3 = +4dBm (reduced gain)
  NF ≈ 3dB (R_G=1.5kΩ)

- Mixer
  Single input and single current output
  Maximum output frequency 100kHz
  Mixer gain: 27dB

- LPF
  Single current input
  Bessel filter (n=10)
  Selectable Bandwidth 40kHz / 80kHz
  Gain ≈ -2dB
  3dB Bandwidth: 38kHz / 75kHz
  maximum attenuation: 77dB (BW=80kHz); >80dB (BW=40kHz)
  70dB attenuation @ 270kHz (BW=40kHz); @450kHz (BW=80kHz)

- Mixer/LPF
  IP3 = 4.5dBm (at limiter input)
  V_{ONOISE} = 150µV (BW=40kHz)
  V_{INOISE} = 8µV (R_G = 50Ω)

- Limiter / RSSI Detector
  Limiter amplifier with 7 stages
  internal speed load circuit for input coupling capacitors
  t_{ON} about 5ms
  RSSI Detector with 7 stages and current output
  IF Bandwidth about 150kHz
  Dynamic Range about 70dB
  minimum input sensitivity: 200µV_{RMS}

- Data Demodulator / Signal Detector
  Data Filter: Sallen-Key-Low Pass Filter
  Selectable Bandwidth: 5k / 10k bps
  1 Comparator for pulse generation
  3 comparators to detect input voltage level

- Whole Receiver
  minimum input sensitivity: 4µV (R_G = 50Ω)
  minimum input sensitivity with transformation circuit: -102dBm
  maximum input voltage (full LNA gain): 2mV
  maximum input voltage (reduced LNA gain): 11mV
  maximum input voltage (LNA disabled): 100mV
  IP3: -14dBm (full LNA gain)
  IP3: 1.8dBm (reduced LNA gain)
  power on settling time: 18ms
  60 channel change settling time (µC-mode): 4ms
  TX → RX mode settling time (µC-mode): 3ms
  RX → TX mode settling time (µC-mode): 2ms

- Power Amplifier (ASK)
  Single output (open collector)
  Output current control (external resistor)

- Whole Transmitter
  TX-Peak Current consumption (DATA=high): about 5.6 mA
  TX-Quiescent Current consumption (DATA=low): about 3.1mA
  RF output voltage @ 50Ω: about 190mV_{RMS}
  RF_ON / RF_OFF blanking : about 75dB
  power on settling time: 18ms
  RX → TX mode settling time: 2ms

- Voltage Controlled Oscillator
  Cross coupled oscillator
  Oscillator frequency f_{Center} = 216.95 MHz / 157.5 MHz (EU / US)
  Fixed Frequency-Doubler (multiplies by 2)
  Frequency control by external Varicap and other external components
  Tuning range ± 5 MHz (depends on external components)
  $V_{VCO1/2}$ = 320mV_{PP} (L_{OSC} = 120nH)

- Reference Oscillator (XTO)
  Crystal oscillator
  Frequency 12.8 MHz
  V_{XTAL} = 1.9V_{PP}
  Power on settling time (measured at XTO –output): 15ms

- Reference Divider
  Divides by 1024 → 12.5kHz channel space for PLL (with multiplier: 25 kHz)
  XTO output: 25 kHz, 50 kHz, 100kHz, 200kHz, 400kHz, 800kHz, 1.6MHz, no signal (recommended if not used)

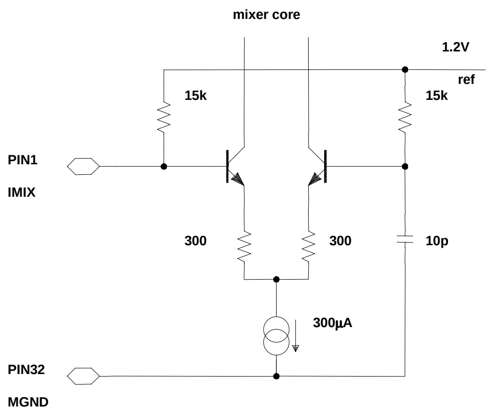
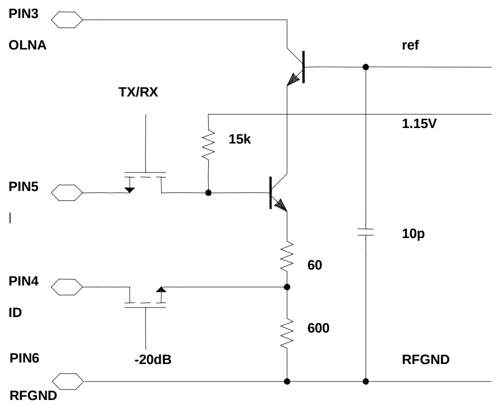
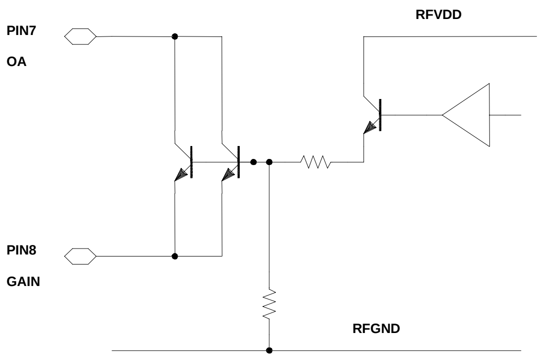
- Main Divider
  Programmable divider with swallow counter
  64 channels (channel width 25 kHz)
  2 selectable frequency bands:
  EU: f_{Center} = 433.9MHz, Divider Ratio: 17324 ..64.. 17387
  US: f_{Center} = 315.0MHz, Divider Ratio: 12568 ..64.. 12631
  Maximum divider input frequency: 270MHz

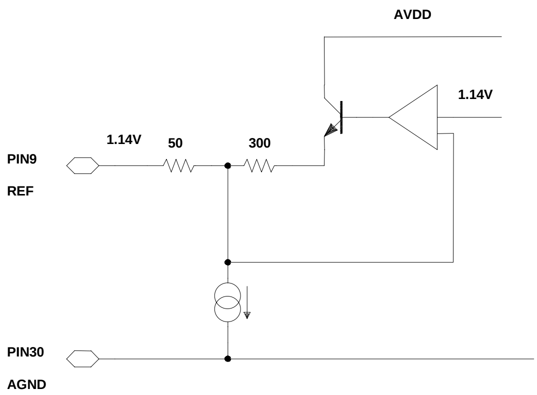
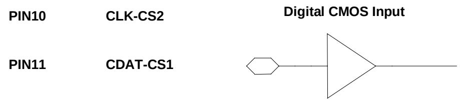
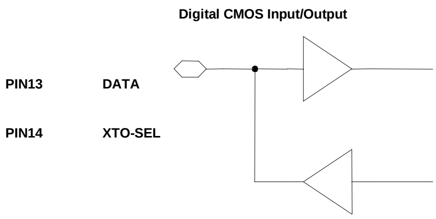
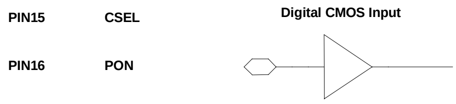
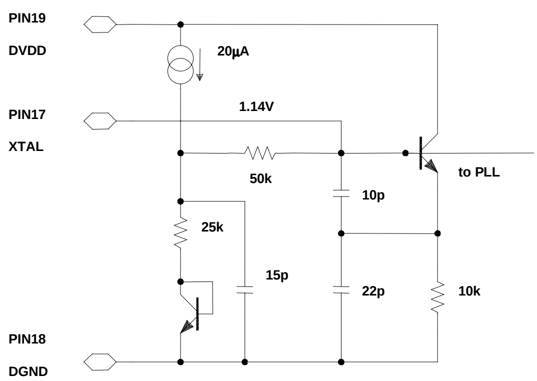
- Frequency / Phase Detector (PD)
  Frequency and Phase Detector with charge pump
  Selectable charge pump current (40 / 80 µA)
  Lock In Detector
  Lock Detect History Flag
  Lock-In-Time: about 4ms (for a 60 channel change)

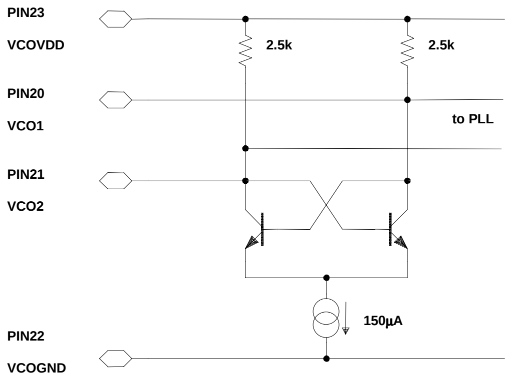
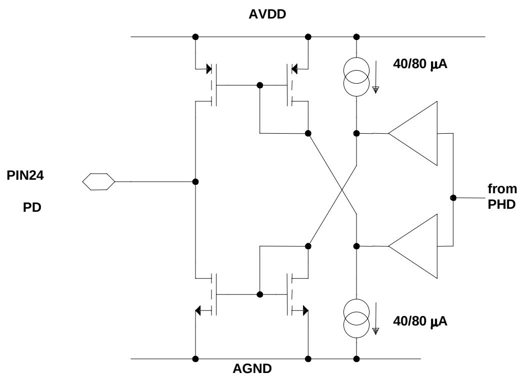
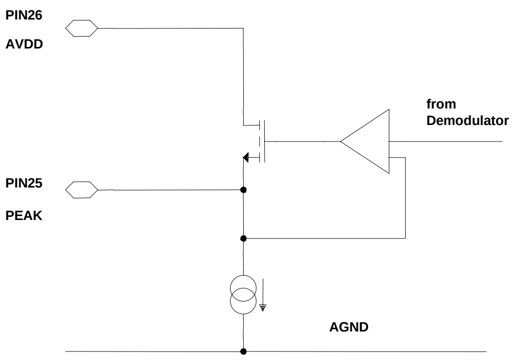
- Control Block
  Controls the functionality of the circuit for both µC and stand alone applications
  Selection of control mode by Pin CSEL (µC/stA)
  Stand alone mode: reduced functionality
  µC mode: controlled by 16 Bit words

- REF/LBAT
  Reference voltage for optional external LNA and Booster
  V_{REF} (ext.) = 1.14V typical [200µA load current]
  V_{TRH} (LBAT) = 2.30V typical
  V_{TRH} (LBAT [LBP high]) = typ. 2.45V
  V_{TRH} (LBAT [LBP high, LBPP high]) = typ. 2.60V typical

10 Pin by Pin description

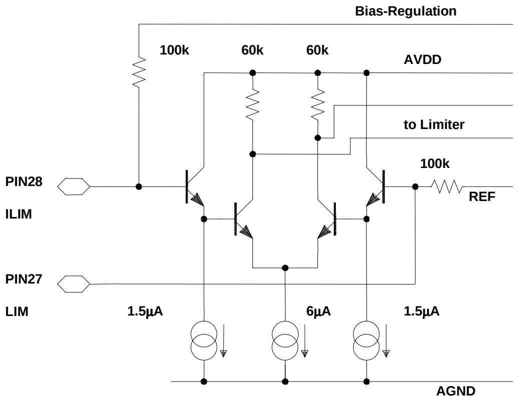
TQFP Pin	Symbol	Internal Equivalent Circuit	Function
1	**IMIX**		**Mixer Input** Single input differential amplifier stage with emitter degradation to improve the large signal behaviour Input impedance 5kΩ || 1.5pF Lower limit frequency will be determined by the internal decoupling capacitor Mixer gain about 27dB ESD Protection according note 1
2	**RFVDD**		**RF Supply** Positive supply voltage for LNA, Mixer, PAMP
3 **5** **4**	**OLNA** **I** **ID**		**LNA Output, LNA Input 2, LNA Input 1** Cascode Configuration with emitter degradation to improve the large signal behaviour Especially designed for loop antennas OLNA: open collector output ESD Protection according note 1 I: RF input with internal antenna switch to disconnect the LNA during TX mode Input Impedance 3.5kΩ || 1.5pF ESD Protection according note 1 ID: disconnectable emitter decoupling (-20dB switch) ESD Protection according note 2
6	**RFGND**		**RF Supply Ground** Negative supply voltage for LNA, PAMP
7 **8**	**OA** **GAIN**		**Power Amplifier Output, Gain Adjust** OA: open collector output ESD Protection according note 1 GAIN: output power adjustment by external components (e.g. R || C) to ground Maximum output power: direct connection to ground ESD Protection according note 2

TQFP Pin	Symbol	Internal Equivalent Circuit	Function
9	**REF**		**Reference Voltage Output** Suitable to bias external LNA or PAMP Typical output voltage 1.14V Maximum load current 200µA ESD Protection according note 2
10 **11** **12**	**CLK-CS2** **CDAT-CS1** **DEN-NSEL**		**CLK-CS2, CDAT-CS1, DEN-NSEL** Digital CMOS Input Function depends on chosen mode (µC- or StandAlone-mode) ESD Protection according note 2
13 **14**	**DATA** **XTO-SEL**		**DATA, XTO-SEL** Digital CMOS Input / Output Function depends on chosen mode (µC- or StandAlone-mode) ESD Protection according note 2
15 **16**	**CSEL** **PON**		**CSEL, PON** Digital CMOS Input CSEL low: µC Mode high: StandAlone Mode PON low: Power ON high: Power OFF ESD Protection according note 2
17	**XTAL**		**Crystal Oscillator Input** Single pin Colpitts oscillator Frequency range 8 .. 14 MHz ESD Protection according note 2
18	**DGND**		**Digital Supply Ground** Negative supply voltage for XTAL, Digital Blocks

TQFP Pin	Symbol	Internal Equivalent Circuit	Function
19	**DVDD**		**Digital Supply Voltage** Positive supply voltage for XTAL, Digital Blocks
20 **21**	**VCO1** **VCO2**		**Voltage Controlled Oscillator** Current controlled oscillator External LC tank circuit needed VCO operates at half of working frequency (internal frequency doubler) ESD Protection according note 1
22	**VCOGND**		**VCO Supply Ground** Negative supply voltage for VCO
23	**VCOVDD**		**VCO Supply Voltage** Positive supply voltage for VCO
24	**PD**		**Charge Pump Output** Selectable output current (40 / 80 µA) ESD Protection according note 2
25	**PEAK**		**Peak Detector Output** Needs to be connected to an external capacitor Peak voltage depends on input field strength Used internally as reference voltage for signal detector and signal strength comparators ESD Protection according note 2
26	**AVDD**		**Analog Supply Voltage** Positive supply voltage for IF Blocks, LPF, others

<table>
<tr><th>TQFP Pin</th><th>Symbol</th><th>Internal Equivalent Circuit</th><th>Function</th></tr>
<tr><td>27

28</td><td>LIM

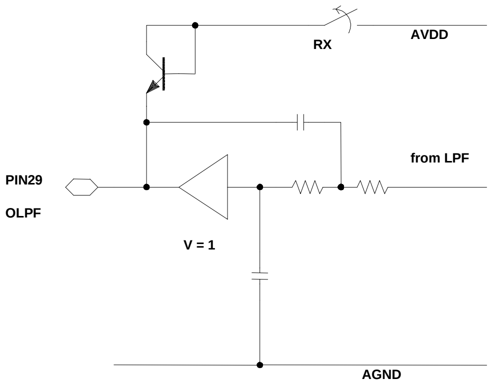
ILIM</td><td>
</td><td>Limiter Decoupling, Limiter Input

<u>LIM:</u> reference voltage for limiter
needs to be connected to ground

ESD Protection according note 2

<u>ILIM:</u> signal input for limiter
needs to be connected to LPF output by a capacitor (47 .. 150 nF)

Input voltage range 200µV ... 500mV

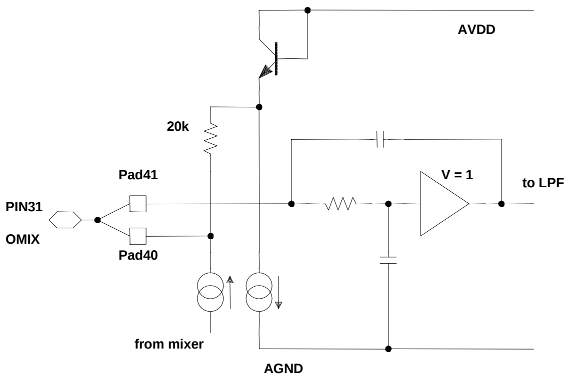
ESD Protection according note 2</td></tr>
<tr><td>29</td><td>OLPF</td><td>
</td><td>Low Pass Filter Output

Bessel filter 10^{th} order

LPF gain: about 1dB

During PowerOFF / TX mode the output will be clamped to near VDD

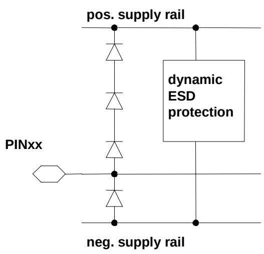
ESD Protection according note 2</td></tr>
<tr><td>30</td><td>AGND</td><td></td><td>Analog Supply Ground

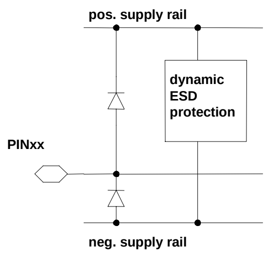
Negative supply voltage for IF Blocks, LPF, others</td></tr>
<tr><td>31</td><td>OMIX</td><td>
</td><td>Mixer Output (LPF input)

An external RC circuit can be used to adjust the mixer gain.

Pad 40 / 41 are connected in TQFP32 version. They need to be connected externally in case of using dice.

ESD Protection according note 2</td></tr>
<tr><td>32</td><td>MGND</td><td></td><td>Mixer Ground

Negative supply voltage for Mixer</td></tr>
<tr><td>-</td><td>-</td><td>Note 1


Note 2

</td><td>ESD Protection Notes</td></tr>
</table>

11 Description of Pin Functions (selection)

11.1 Control Pins

- PON

PON → GND : active
PON → VDD : power down
The LH edge (Power ON → Power OFF) will reset all registers to 'low'. After power ON all registers are still 'low'.

- CSEL

CSEL → GND : µC application (all functions controlled by a serial data word)
CSEL → VDD : stand alone application (different Pin functions: CDAT→CS1, CLK→CS2, DEN→NSEL, XTO→SEL)

11.2 Stand Alone Pin Functions

- CS1 / CS2

CS1 and CS2 are connected directly to the channel decoder to select one of 2^2 available channels.

CS2	CS1	Channel	$f(TX)_{EU}$	$f(TX)_{US}$
low	low	10	433.350MHz	314.450MHz
low	high	14	433.450MHz	314.550MHz
high	low	46	434.250MHz	315.350MHz
high	high	51	434.375MHz	315.475MHz

- SEL

Selects receiving or transmitting mode:
SEL → GND : receiving mode
SEL → VDD : transmitting mode
In case of RX mode the VCO frequency will be decreased automatically (equivalent 50kHz IF frequency). DATA will be wired to RxData or TxData respectively. It is not possible to read out other information like CMPx, LDET, LBAT.

- NSEL

Selects between the European and North American ISM band; connected to the N1 divider to adapt its divider ratio to the frequency range:
NSEL → GND : EU mode
NSEL → VDD : US mode

11.3 µC-Application Pin Functions

- CDAT

Serial data input for 16-Bit data words. (LSB first)

- CLK

Clock input for shift register.

- DEN

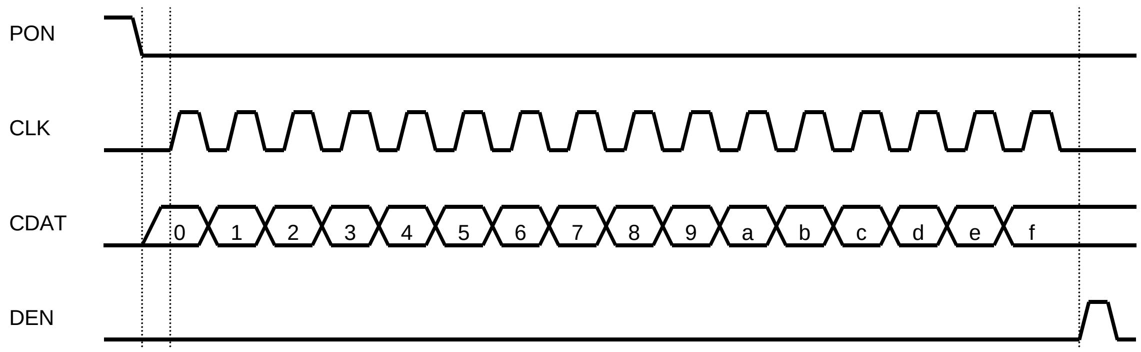
Enables to copy the data word from the input shift register into a 16-Bit parallel output storage register.

- XTO

XTO provides clock signals for external use. The frequency is programmable by the configuration control word. The default frequency is 25kHz.
50kHz, 100kHz, 200kHz, 400kHz, 800kHz, 1.6MHz and 0Hz are also available.
The settling time is about 40us.

12 Description of Control and Configuration Data Words (CCW)

12.1 Timing Diagram for CCW input



The figure shows how to input the CCW using the pins CLK, CDAT, DEN. The maximum clock frequency (CLK) should not exceed 1MHz. The CCW`s have to be sent with LSB first.

12.2 Control Data Word (all bits are low after PowerOn Reset)

Bit	Internal Name	Status	Description
0		low	Marks this data word as control word
		high	Marks this data word as configuration word
1	RXTX	low	Enables RX mode
		high	Enables TX mode
2	LNAGAIN	low	Enables maximum LNA gain
		high	Enables decreased LNA gain (-20dB)
3	DR	low	Enables 9600 bps data rate for data filter
		high	Enables 4800 bps data rate for data filter
4	BW	low	Enables 80 kHz bandwidth for LPF
		high	Enables 40 kHz bandwidth for LPF
5	CHPC	low	Enables 40uA charge pump current
		high	Enables 80uA charge pump current
6-9		1)	I/O multiplex control of RxData / TxData / LBAT / LDET /LDET_HIST / CMP1 / CMP2 / CMP3 / NREF / PN
a-f		2)	2^6 = maximum 64 channel decoder (channel space: 25kHz)

1) see also chapter 12.4 2) see also chapter 12.5

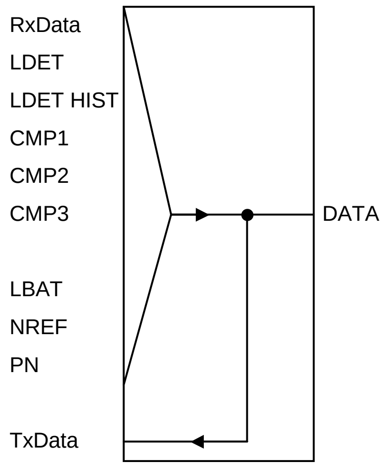
12.3 Configuration Data Word (optional, all bits are low after PowerOn Reset)

Bit	Internal Name	Status	Description
0			See description of control data word
1	LNADIS	low	Enables internal LNA
		high	Disables internal LNA
2	LDBP	low	Loop Detect Bypass off (default !)
		high	Loop Detect Bypass on (test mode only, Do not use!)
3	EUUS	low	Enables EU frequency range
		high	Enables US frequency range
4-6			Select the output frequency at CLK, default 25 kHz
7	COMP *)	high	Enables alternative DataComp threshold level (0.7*V_{PEAK})
8	LBP *)	high	Enables increased LBAT threshold level (approx. +150mV)
9	LBPP *)	high	Enables increased LBAT threshold level (approx. +150mV)
a	LDTC *)	high	Enables increased current in loopDetectTimer
b-f			Not used

*) Not guaranteed function, default low

12.4 Description of I/O Multiplexer

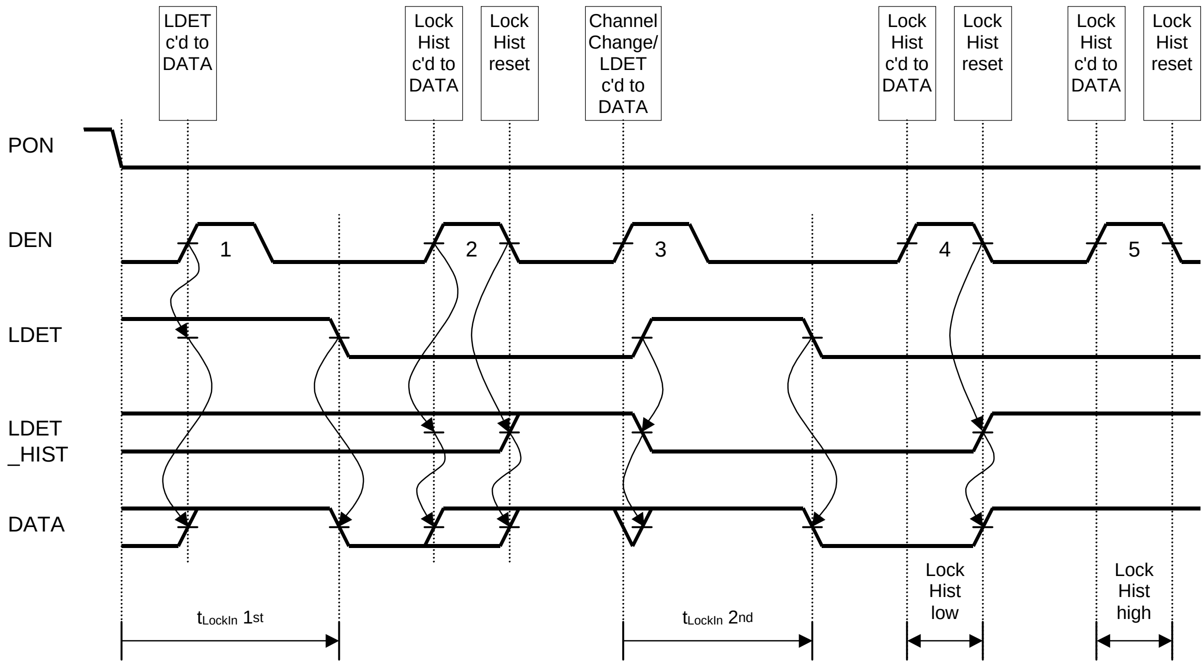
The I/O Multiplexer is available in µC mode only. It connects several internal signals to the external pin DATA. Only one input / output is available at one time.



- **RxData**: Pin DATA is connected to the internal output of the data comparator. The received information will be directly putted through to this pin. The data needs to be recovered.
- **TxData**: In case of a locked PLL the pin DATA controls directly the internal input of the power amplifier (if DATA = HIGH → amp. ON; if DATA = LOW → amp. OFF). The information which is put in will be sent without buffering.
  In case of an unlocked PLL the power amplifier will be OFF, independent of the logical status of pin DATA.
- **CMP1-3**: The pin DATA is connected to the internal output of one of the Peak Level comparators. This can be used to get an idea about the field strength of the input signal. The output of the comparators will be high if the input level is higher than the internal threshold. This information can be used to check the band for a 'free' channel or to control the LNA gain (e.g. the gain may be reduced by the LNAGAIN switch if the highest level is reached).
  CMP3: small input level
  CMP2: medium input level
  CMP1: high input level
  The voltage at the pin PEAK presents the input level as an analogue signal. It may be probed by a high ohmic OPAmp (MOS input stage).
- **LBAT**: The pin DATA is connected to the internal output of the LowBat comparator. It compares the actual (shifted) supply voltage with an internal reference voltage. The threshold of this comparator may be influenced by the control data word.
- **NREF**: DATA is connected to the internal reference divider output. The regular output frequency is 25kHz. This function has test purposes only. It isn`t needed for customer applications.
- **PN**: DATA is connected to the internal main divider output. The regular output frequency is 25kHz. This function has test purposes only. It isn`t needed for customer applications.
- **LDET**: DATA is connected to the Lock Detector output. This can be used to check if the system is ready to transmit or receive before starting a communication. To prevent unintended radiation the powerAmp is able to send only in case of a locked loop (LDET=low). It isn`t possible to permanently monitor LDET during a Rx or Tx process.
- **LDET_HIST**: This is a flag which permanently observes the status of LDET. Normally it is needed to check the PLL status to be sure that the SE6100 is ready to receive or transmit. If it is locked, the data transmission can be started. During the transmission the LDET status cannot be supervised. If the PLL will unlock for a short period during the transmission phase the data will be incomplete. Using the History flag the system can get the information if the data was completely sent or not (PLL locked or not during transmission).
  The LDET_Hist flag needs to be read out and resetted in the following way:
  The flag information is available at pin DATA only during the data enable (DEN) pulse. The L-H edge of DEN connects the flag register to DATA (LOW = locked during the last period; HIGH = unlocked during the last period). The H-L edge of DEN will reset the flag register to LOW. Now it is active and supervises the lock detector up to the next time it will read out.

The following draft should help to understand the function of the LDET / LDET_HIST. It can be also used to check the functionality.

1. Power On; Load control word hex0100 (LDET connected to DATA)
   wait for 1st lockIn (about 18ms)
2. Check&Reset of LDET_HIST (hex0300)
3. Force PLL to unlock by channel change, connect LDET to DATA (e.g. Channel 8, hex0104)
   wait for 2nd lockIn (about 4ms)
4. Check&Reset of LDET_HIST (hex0304):
   needs to be low during DEN pulse (meanwhile PLL unlocked)
5. Check&Reset of LDET_HIST (hex0304) again:
   needs to be high during DEN pulse (meanwhile PLL still locked)



12.5 Channel Programming

The channel information is a part of the control data word (LSB+10 … MSB)

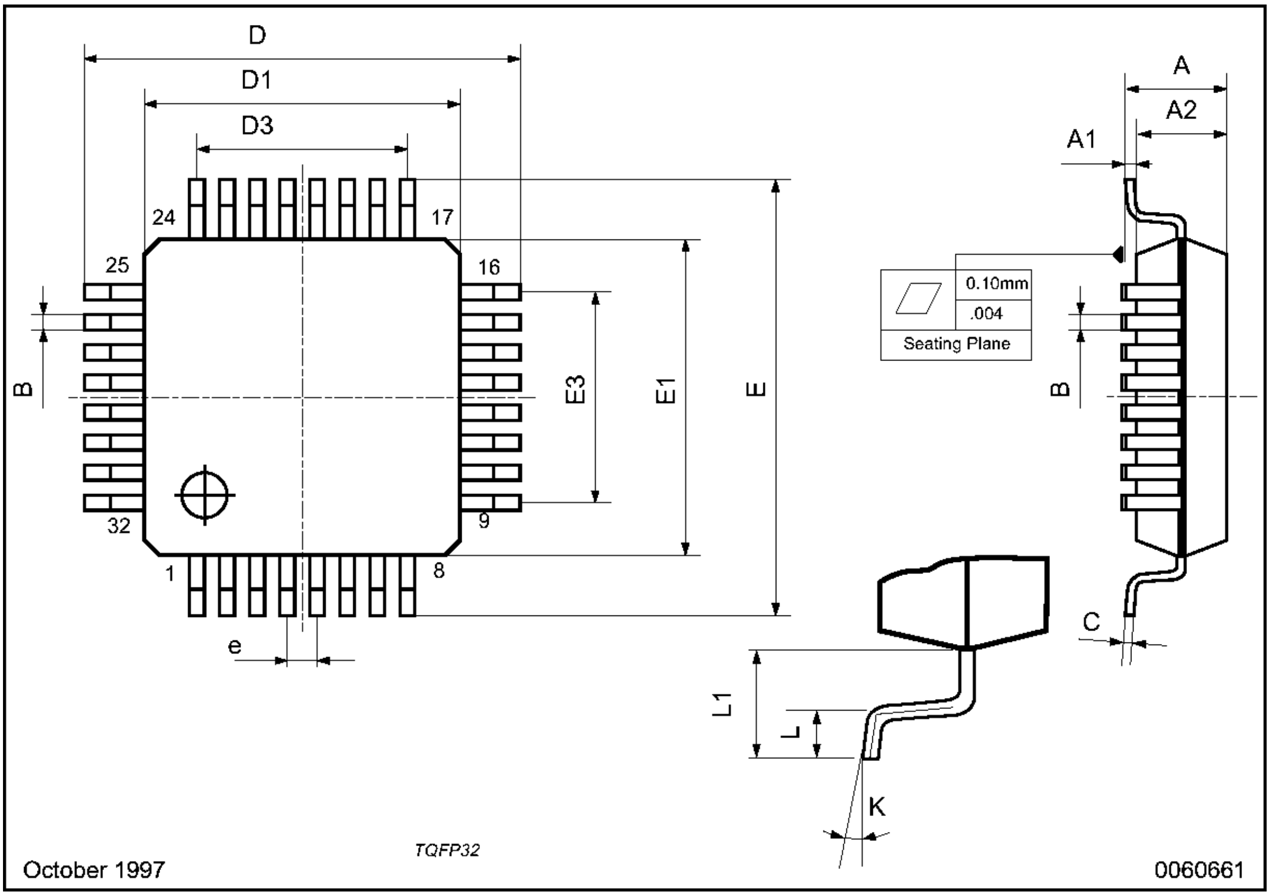
Channel	Binary Code	f_{EU}	f_{US}
0	000000	433.100MHz	314.200MHz
1	100000	433.125MHz	314.225MHz
2	010000	433.150MHz	314.250MHz
…	…	…	…
61	101111	434,625MHz	315.725MHz
62	011111	434.650MHz	315.750MHz
63	111111	434.675MHz	315.775MHz

12.6 Logic table of CCW`s (short description)

Control Data Word Description	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f	Remarks
Select Control Word	0																
Select Configuration Word	1																
RX - Mode	0	0															
TX - Mode	0	1															
LNA Gain normal	0		0														
LNA Gain -20dB	0		1														
DataRate=9600bps	0			0													
DataRate=4800bps	0			1													
BandWidth=50kHz	0				0												
BandWidth=25kHz	0				1												
ChargePumpCurrent=40uA	0					0											
ChargePumpCurrent=80uA	0					1											
RX-Data connected to DATA	0						0	0	0	0							
TX-Data connected to DATA	0						1	0	0	0							
LDET connected to DATA	0						0	1	0	0							
LDET_HIST connected to DATA	0						1	1	0	0							
CMP1 connected to DATA	0						0	0	1	0							high input level
CMP2 connected to DATA	0						1	0	1	0							medium input level
CMP3 connected to DATA	0						0	1	1	0							low input level
not used	0						1	1	1	0							
LBAT connected to DATA	0						0	0	0	1							
NREF connected to DATA	0						1	0	0	1							
PN connected to DATA	0						0	1	0	1							
Channel 0-63	0										l	x	x	x	x	m	LSB first
Configuration Data Word Description																	
Internal LNA enabled	1	0															
Internal LNA disabled	1	1															
Lock detect bypass off	1		0														
Lock detect bypass on	1		1														Test mode only !
EU frequency range	1			0													
US frequency range	1			1													
CLK 25 kHz	1				0	0	0										
CLK 50 kHz	1				1	0	0										
CLK 100 kHz	1				0	1	0										
CLK 200 kHz	1				1	1	0										
CLK 400 kHz	1				0	0	1										
CLK 800 kHz	1				1	0	1										
CLK 1.6 MHz	1				0	1	1										
no signal	1				1	1	1										
COMP Threshold=0.8*Vpeak	1							0									
COMP Threshold=0.7*Vpeak	1							1									
LBAT Threshold 2.30V	1								0	0							
LBAT Threshold 2.45V	1								1	0							LBP: high
LBAT Threshold 2.60V	1								1	1							LBP, LBPP: high

13 Package TQFP32

DIM.	mm			Inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.60			0.220	
e		0.80			0.031	
E		9.00			0.345	
E1		7.00			0.276	
E3		5.60			0.220	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 7°(max.)					
Weight: 0.20gr						



14 Application Notes

14.1 Typical SE 6100 application for 433 MHz

In the following figures is presented one of HKW`s currently used standard modules prepared for 433MHz applications. This circuit/module was also used as reference and test-circuit for various measurements documented in this data-sheet. Modules of type HK75/i can be purchased from HKW .

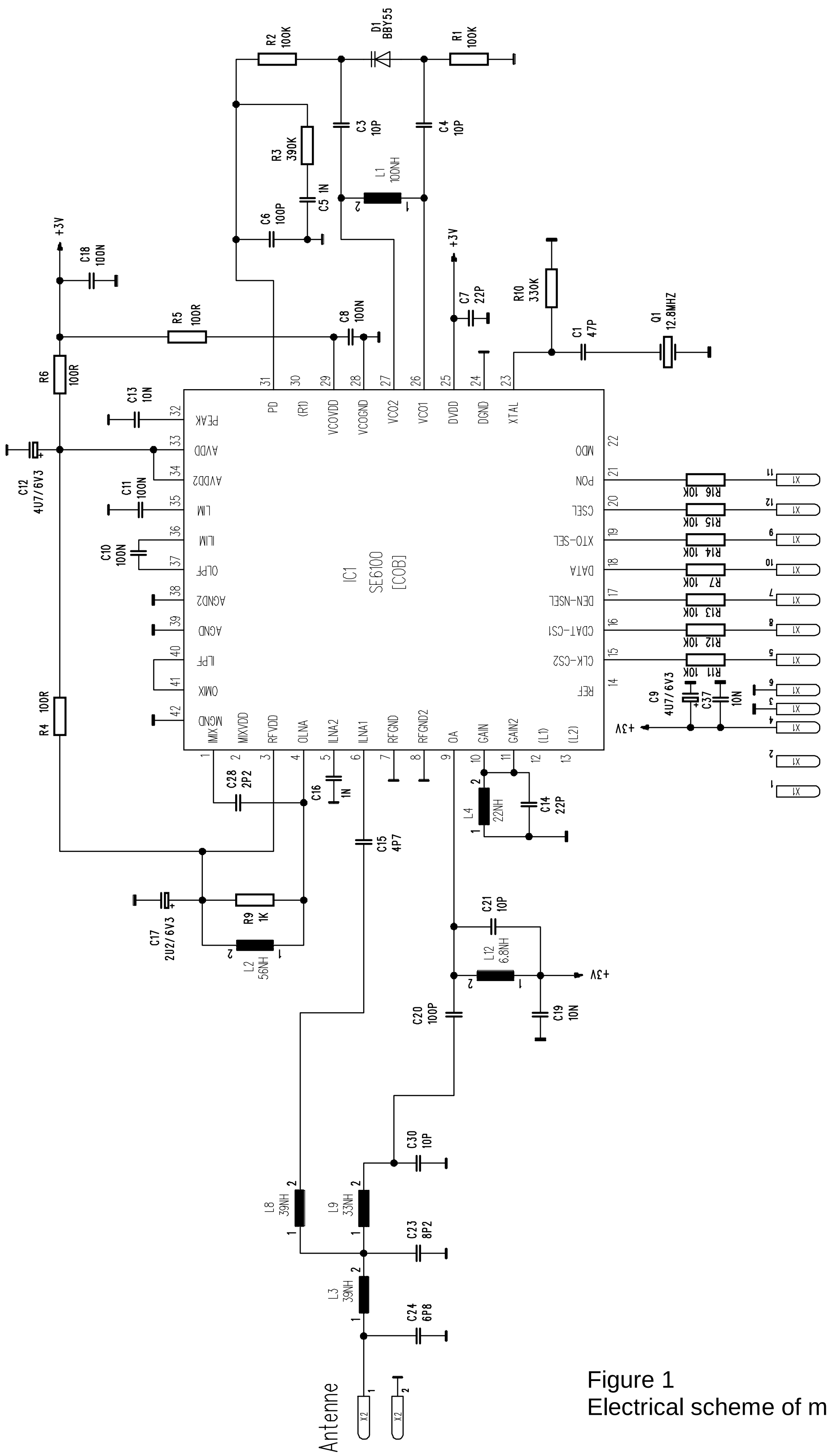
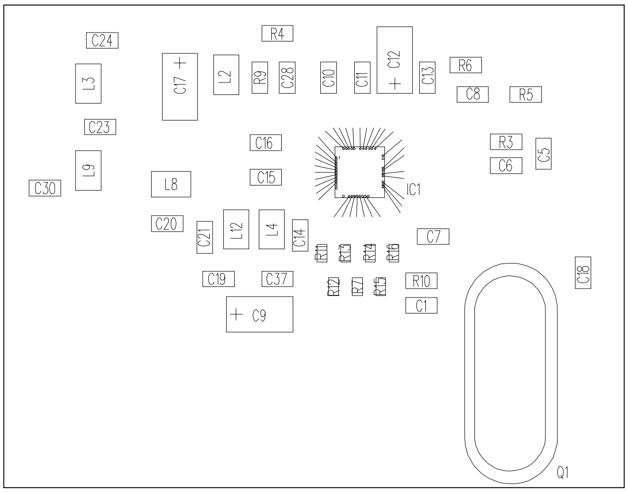


Figure 1
Electrical scheme of module HK 75/i



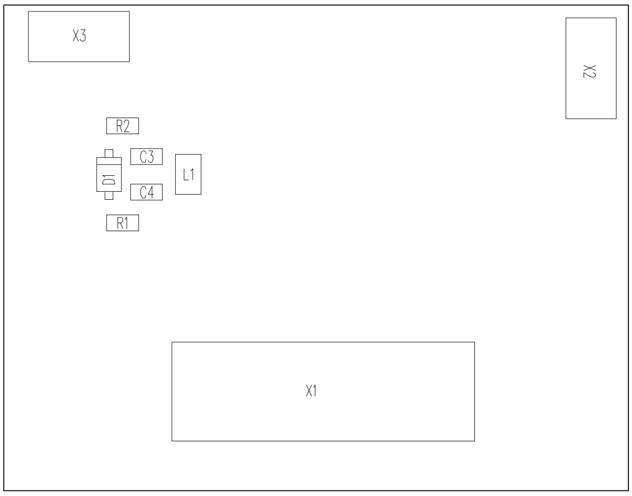
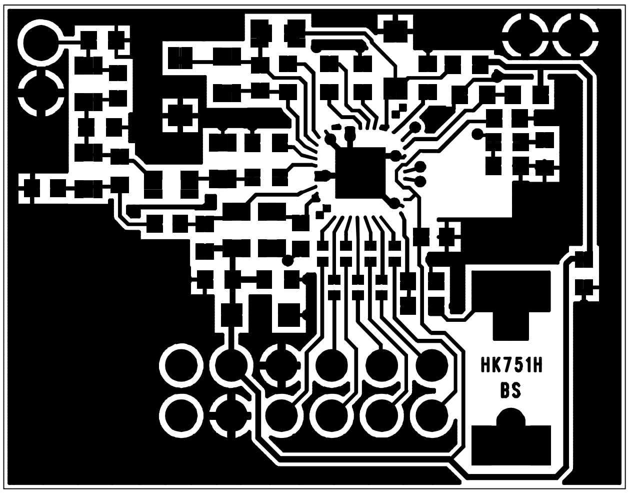


Figure 2
Component placement
(component side)

Figure 3
Component placement
(solder side)



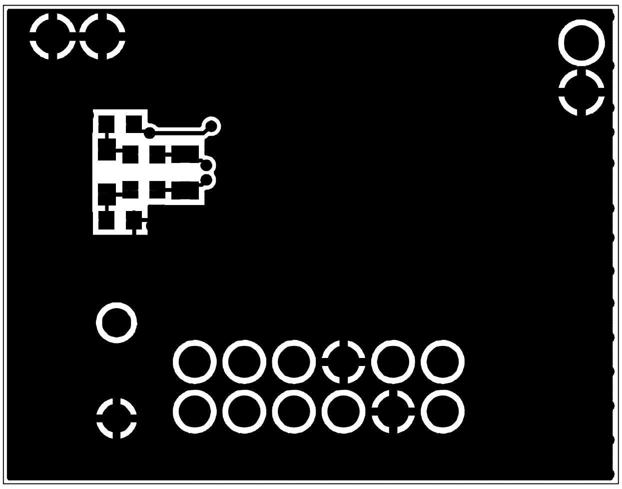


Figure 4
PCB layout (component side)

Figure 5
PCB layout (solder side)

Module HK75/i is realized on base of PCB-version HK 75/h.
The real dimension of this PCB is 31.70mm x 24.65mm .

14.2 Receiver Channel (µC mode only)

In case of bi-directional (half-duplex) communication the receiving device needs to be set one or two channels beside the transmitter channel (IF frequency 25 or 50 kHz respectively).
In case of stand-alone mode the VCO frequency will be decreased automatically (equivalent 50kHz IF frequency).

Note

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