SED1181

CMOS DOT MATRIX EXTENSION LCD DRIVER

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1.0 GENERAL DESCRIPTION

1.1 DESCRIPTION

The SED1181FLA is a segment (column) driver suitable for driving high-contrast, small-capacity dot matrix Liquid Crystal Displays (LCDs) with a duty range of static to 1/32. It is best suited for extending the segment drive capability of the SED1278, HD44780, HD66780, or low voltage 4-bit microcomputers.

1.2 FEATURES

- Display Duty cycle: Static to 1/32
- 64-bit High Voltage Output - Display Voltage Maximum of 25V
- Shift Right Method of Entering Data
- Cascadable Mode
- Easily configured with General-Purpose LCD Controllers
- 5 Volt Operation
- Low Power CMOS
- 80 Pin Flat Plastic Package

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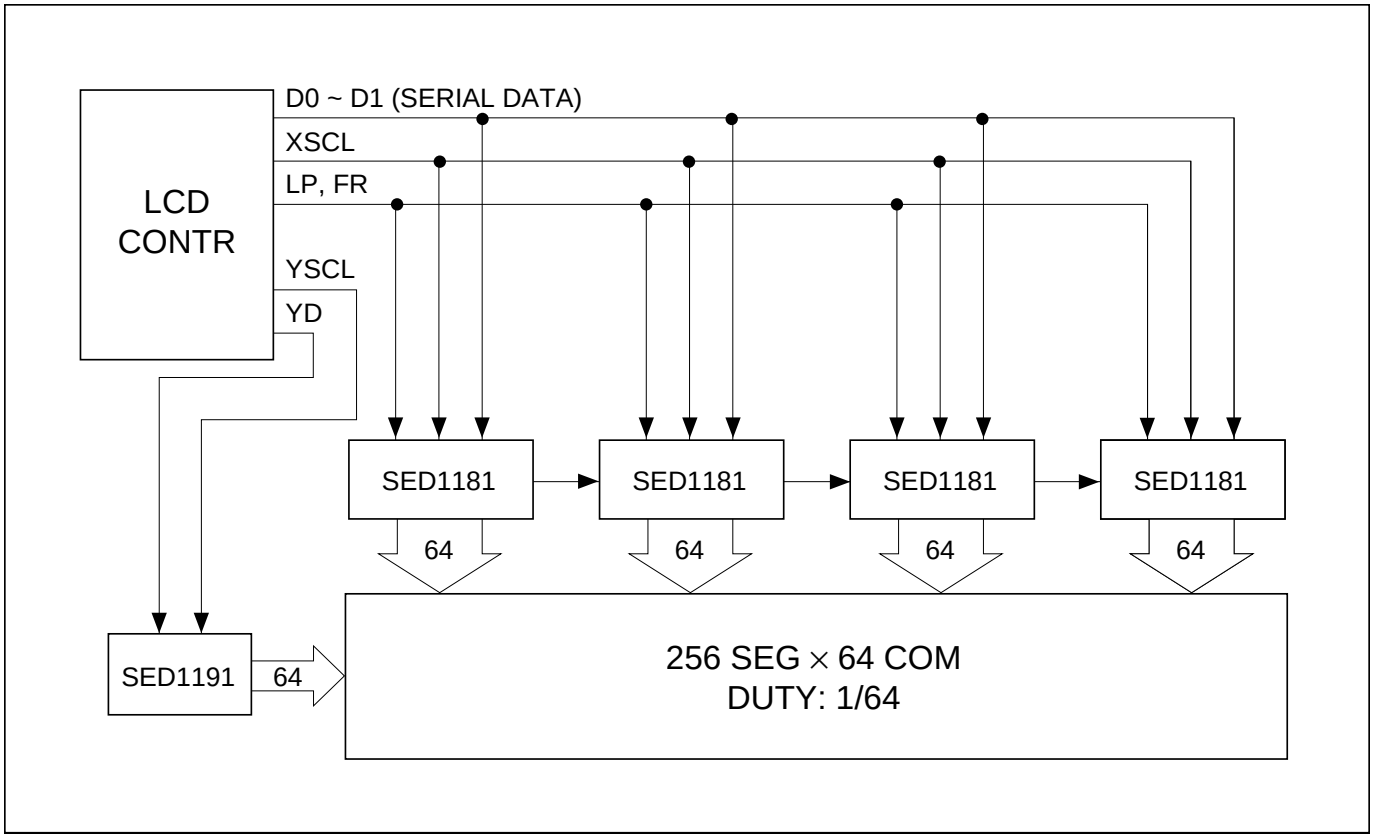
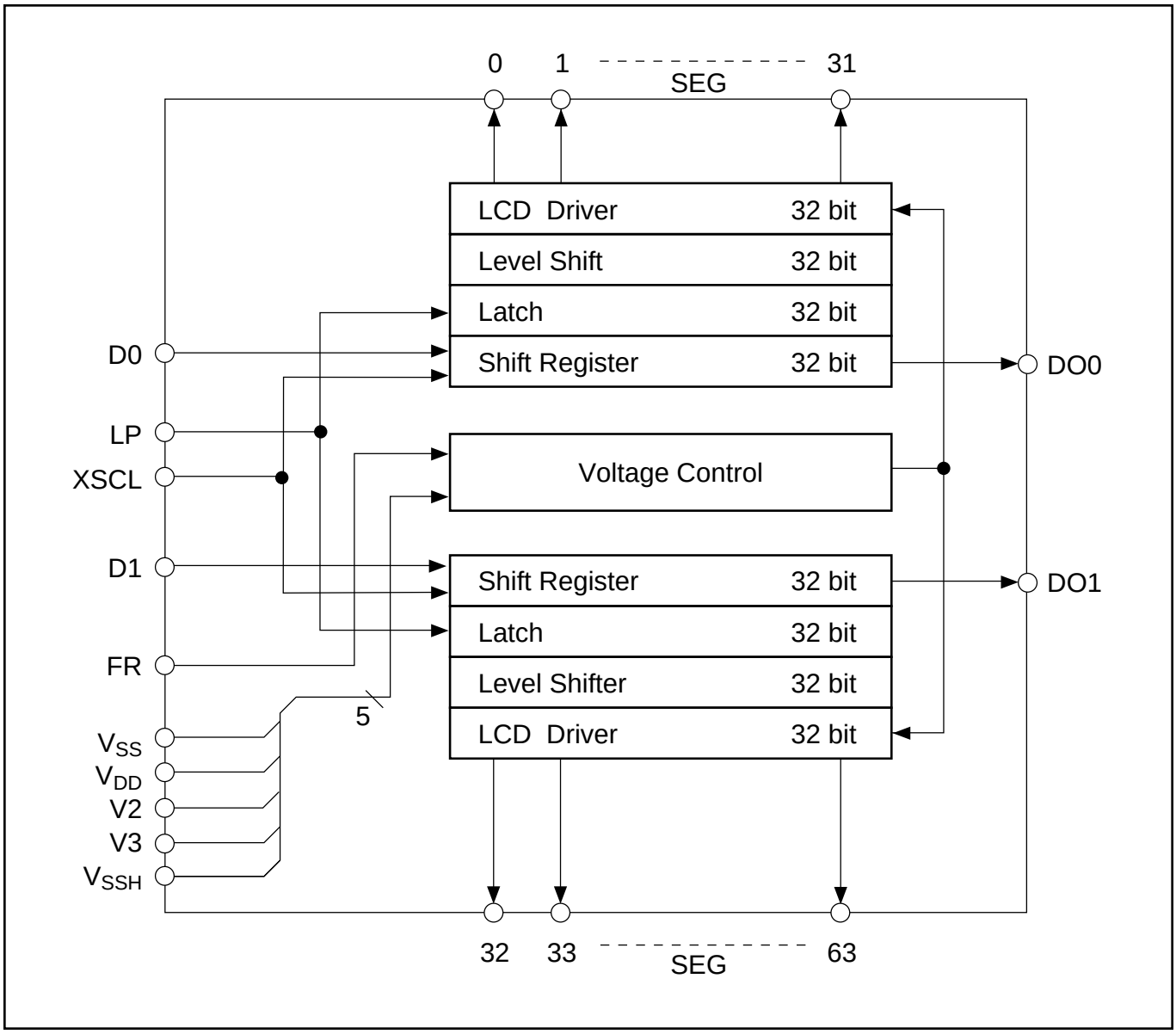
2.0 BLOCK DIAGRAMS

2.1 SYSTEM BLOCK DIAGRAM



2.2 BLOCK DIAGRAM



2.3 BLOCK FUNCTIONS

2.3.1 Shift Register

The SED1181F$_{LA}$ incorporates a 64-bit serial to parallel static shift register used to shift in segment data which is outputted via the parallel outputs, to each of the 64 latches.

The 64-bit shift register is separated into two 32-bit shift right registers. Each of the two shift registers have serial input, output and parallel output ports. The relationship between the data input pins (serial in) and the segment output pins (parallel out) is shown below:

D0	SEG0 to SEG31
D1	SEG32 to SEG63

Data is transferred on the falling edge of the shift clock, XSCL. Data in the shift register is not lost if the shift clock is stopped, allowing for data transfer with a high degree of flexibility.

Each first bit of data input to D0 or D1 is entered to the shift register element corresponding to SEG31 or DEG63, respectively, while the last bit of data is entered to the shift register element corresponding to SEG0 or SEG32.

2.3.2 Latch

A built-in 64-bit latch circuit latches display data which has already been subject to serial-parallel conversion by the shift register.

Display data is latched on the falling edge of the latch pulse LP. Latched data is then transferred to the LCD driver through the level shifter circuit.

2.3.3 Level Shifter

The level shifter is an interface circuit that converts the logic-level data into LCD level data. The LCD level data is then transferred to the LCD drivers.

2.3.4 LCD Driver

The LCD driver is a 64-bit segment driver. The segment driver generates LCD segment drive signals based on data from the level shifter and the frame signal (FR).

According to the frame signal FR and display data, each LCD segment drive signal is output as shown below.

The segment drive signal level changes on the falling edge of the latch pulse, LP.

D0, D1	FR	SEG0 – 63
H	L	V_{DD}
H	H	V_{SSH}
L	L	V2
L	H	V3

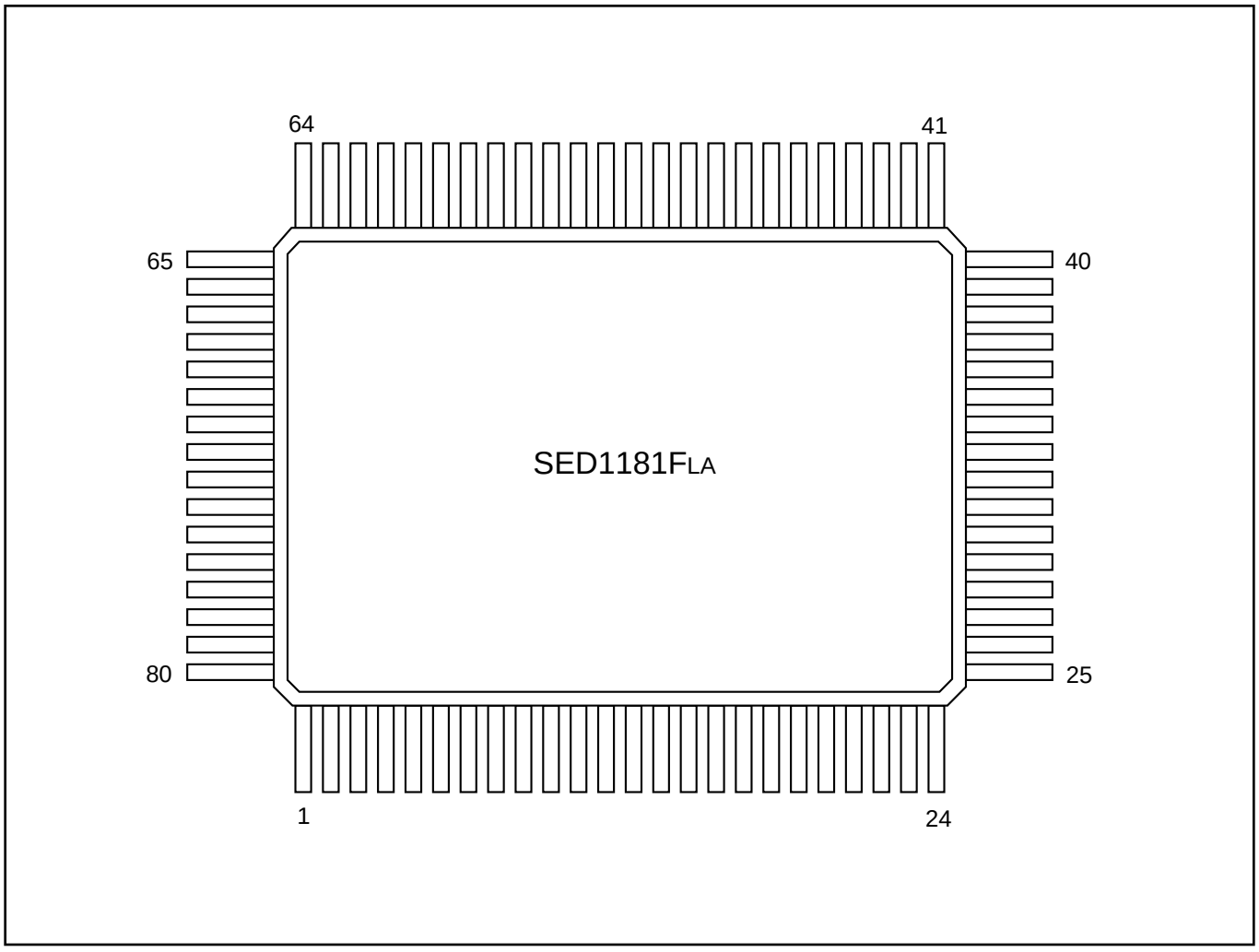
2.3.5 Voltage Control

The power control circuit selects an LCD drive voltage, supplied at pins VDD, V2, V3 and VSSH according to the frame signal (FR) status and supplies it to the 64-bit LCD driver. Depending on the frame signal FR, the LCD driver outputs LCD drive voltages as shown below:

FR	LCD ON Level	LCD OFF Level
L	V_{DD}	V2
H	V_{SSH}	V3

3.0 PIN CONFIGURATION

3.1 PIN CONFIGURATION



Pin		Pin		Pin		Pin	
Number	**Name**	**Number**	**Name**	**Number**	**Name**	**Number**	**Name**
1	SEG27	21	SEG7	41	SEG36	61	SEG56
2	SEG26	22	SEG6	42	SEG37	62	SEG57
3	SEG25	23	SEG5	43	SEG38	63	SEG58
4	SEG24	24	SEG4	44	SEG39	64	SEG59
5	SEG23	25	SEG3	45	SEG40	65	SEG60
6	SEG22	26	SEG2	46	SEG41	66	SEG61
7	SEG21	27	SEG1	47	SEG42	67	SEG62
8	SEG20	28	SEG0	48	SEG43	68	SEG63
9	SEG19	29	DO0	49	SEG44	69	V_{SSH}
10	SEG18	30	NC	50	SEG45	70	V_2
11	SEG17	31	NC	51	SEG46	71	V_3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	DO1
15	SEG13	35	LP	55	SEG50	75	NC
16	SEG12	36	FR	56	SEG51	76	NC
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG9	39	SEG34	59	SEG54	79	SEG29
20	SEG8	40	SEG35	60	SEG55	80	SEG28

3.2 PIN DESCRIPTION

Pin Name	I/O	Function	Quantity
SEG0~63*	O	Outputs to segment pins of LCD. (X side) Output level changes at each latch pulse LP falling-edge	64
XSCL	I	Shift clock for display. Falling edge (CL2)	1
LP	I	Latch pulse for display data. Falling edge (CL1)	1
FR	I	LCD frame signal (M)	1
DO0	O	Output serial display data input from D0.	1
DO1	O	Output serial display data input from D1.	1
D0, D1	O	Input serial display data (Reads data at XSCL falling-edge)	2
V_{DD}, V_{SS}	I	Power source for logic V_{DD} = (V_{CC}), V_{SS} : (GND)	2
V2, V3	I	Power source for LCD drive $V_{DD} > V2 > V3 > V_{SSH}$	3

*D0: Serial display data corresponds to SEG0 to SEG31.
D1: Serial display data corresponds to SEG32 to SEG63.

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4.0 ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 – 0.3	V
Supply voltage (2)	V_{SSH}	–15.0 – 0.3	V
Supply voltage (3)	V2, 3	–15.0 – 0.3	V
Input voltage	V_{IN}	V_{SS} – 0.3 – 0.3	V
Output voltage	V_O	V_{SS} – 0.3 – 0.3	V
Permissible power dissipation	P_D	250	mW
Operating temperature	T_{OPR}	–30 – 85	°C
Storage temperature	T_{STG}	–65 – 150	°C
Soldering temperature and time	T_{SOLDER}	260 / 10 (lead section)	°C/Sec.

Notes: (1) All voltages are given on the basis of V_{DD}=0V

(2) V2 and V3 shall always satisfy the conditions: $V_{DD} \geq V_2$, $V_3 \geq V_{SSH}$

(3) Exceeding the LSI's absolute maximum ratings could result in destruction of the device. In normal operation, the LSI should be used within the ranges shown in the electrical characteristics. If used with values exceeding the rated range, the LSI may operate erroneously and its reliability may be reduced.

(4) Moisture resistance of the flat package may be adversely affected when it is dipped in a solder bath. Therefore, avoid applying thermal stress to the resin portion of package during board manufacturing processes.

4.2 DC ELECTRICAL CHARACTERISTICS

Ta = –30 ~ 85°C and V_{SS} = –5.0V ± 10%

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage (1)	V_{SS}		–6.0	–5.0	–2.4	V
Supply voltage (2)	V2		V_{SSH}		V_{DD}	V
	V3		V_{SSH}		V_{DD}	V
	V_{SSH}	Recommended V_{SSH}	–12.0		–3.0	V
		Operable V_{SSH} *2	–12.0		–2.5	V
"H" level input voltage	V_{IH}		0.2 V_{SS}		V_{DD} + 0.3	V
"L" level input voltage	V_{IL}		V_{SS} – 0.3		0.8 V_{SS}	V
"H" level output voltage	V_{OH}	I_{OH} = –0.6mA	–0.4			V
"L" level output voltage	V_{OL}	I_{OL} = 0.6mA			V_{SS} + 0.4	V
Input leak current	I_{LI}	0V ≤ V_{IN} ≤ V_{SS}		0.05	2.0	µA
Output leak current	I_{LO}	0V ≤ V_{OUT} ≤ V_{SS}		0.05	5.0	µA
Transfer clock	XSCL				600	KHz
Frame signal cycle	FR			1/60		Sec
Input capacitance	C_{IN}	Ta = 25°C, f = 1.0MHz		5.0	8.0	PF
SEG output On resistance	R_{SEG}.	$\|\Delta V_{OH}\|$ = 0.1V, Ta = 25°C, V_{SSH} = –8.0V		3.0		KΩ
		V_{SSH} = –5.0V		5.0		
		V_{SSH} = –3.0V		16.0		
Idle current	I_Q	V_{SSH} = –12.0V, V_{SS} = –6.0V, V_{IN} = V_{DD}		0.05	30.0	µA
Logic system source Current during Operation	$I_{SS\ OP}$	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS} FR cycle = 16.7ms (Duty 50%) LP cycle = 520 XSCL = 400KHz (Duty 50%) All data input reversed for every bit All output pins are opened		250	300	µA
LCD system source Current during Operation	$I_{SSH\ OP}$	V_{SS} = –4.5V, V2 = –4.8V V_{SS} = –7.2V, V_{SSH} = –12.0V Other conditions are identical to those of $I_{SS\ OP}$.		8	10	µA

*1: Voltages are given on the basis of V_{DD} =0V.

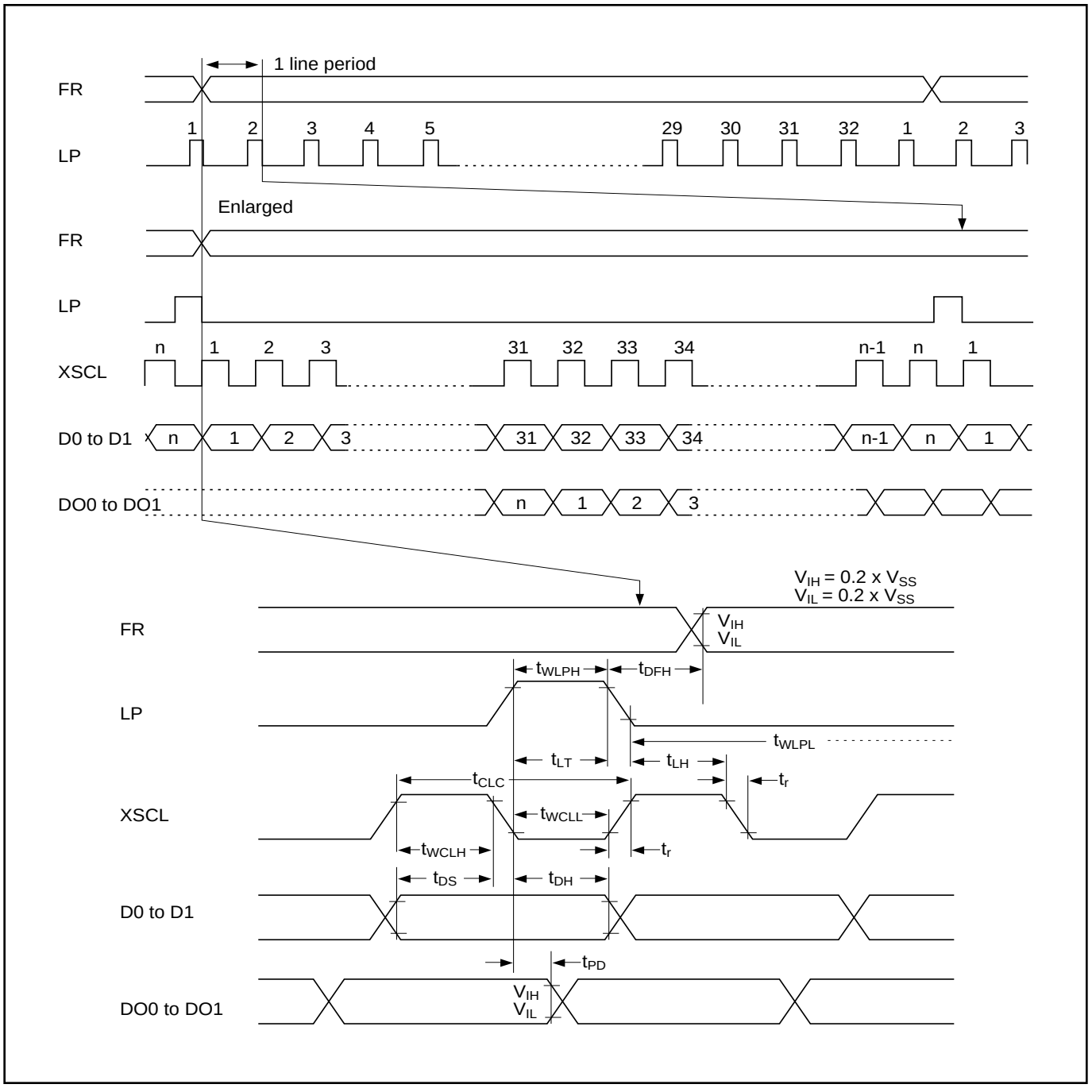
*2: Operable V_{SSH} indicates the range in which LSI is operable, although the driver output ON resistance becomes higher than that with recommended V_{SSH}. To determine the practical voltage, we recommend testing the driver with the liquid crystal panel to be used.

4.3 AC ELECTRICAL CHARACTERISTICS

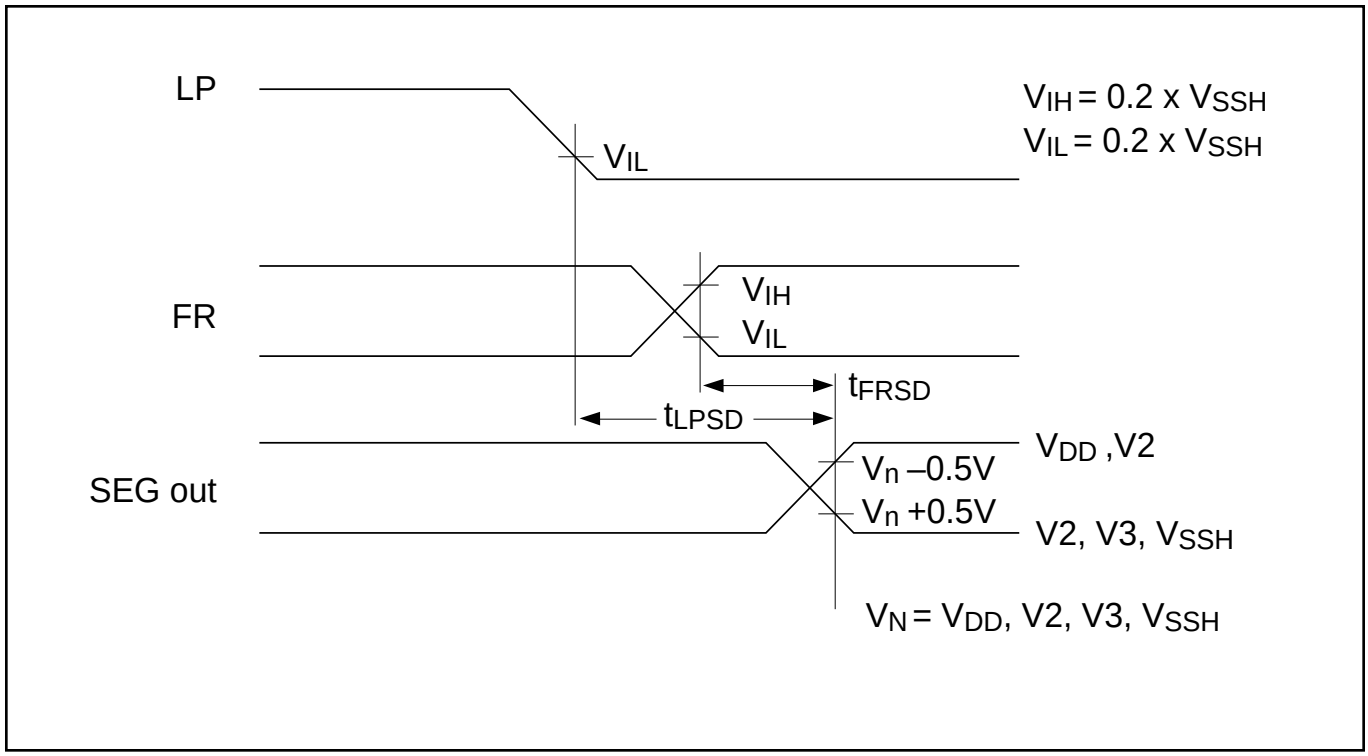
Ta = –30 – 85°C and V_{SS} = –5.0V ± 10%

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Shift clock cycle	t_{CLC}		1.65			µs
Shift clock “H” width	t_{WCLH}		450			ns
Shift clock “L” width	t_{WCLL}		600			ns
Data setup time	t_{DS}		100			ns
Data hold time	t_{DH}		30			ns
Latch pulse “H” width	t_{WLPH}		200			ns
Latch pulse “L” width	t_{WLPL}		600			ns
Latch timing	t_{LT}		200			ns
Latch hold time	t_{LH}		100			ns
Permissible frame signal delay	t_{DFR}		–500	0	500	ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
Serial data output delay	t_{PD}		20		250	ns

4.4 INPUT/OUTPUT SIGNAL TIMING CHARACTERISTICS



4.5 SEGMENT OUTPUT SIGNAL TIMING CHARACTERISTICS



Ta = –30 – 85°C and V_{SS} = –5.0 ± 10%

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
LP – SEG output delay time	t_{LPSD}	V_{SSH} = –3V – 12V			4.5	µs
FR – SEG output delay time	t_{FRSD}	CL = 100PF			4.5	µs

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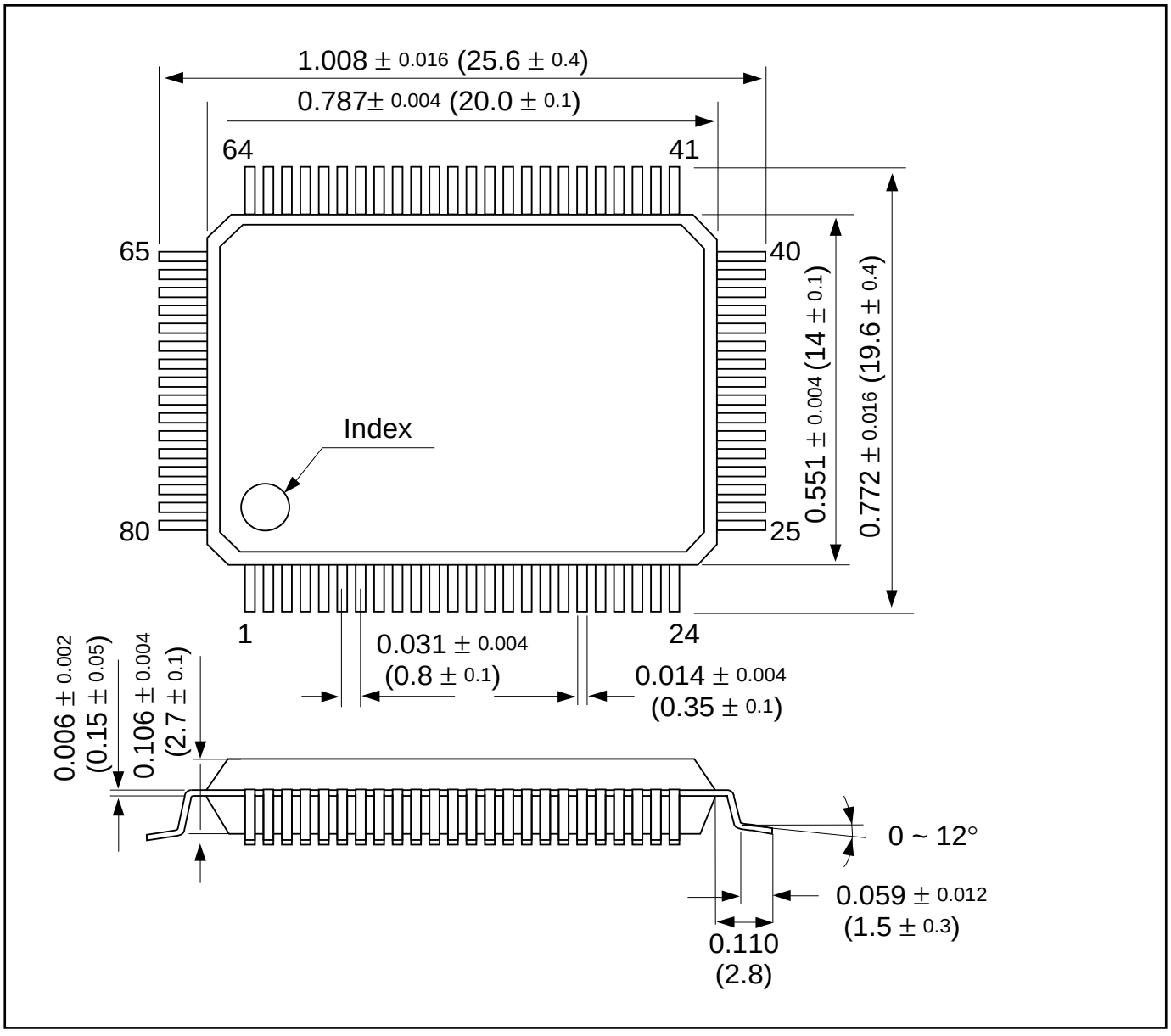
5.0 PACKAGE DIMENSIONS

80 Pin Flat Plastic Package (Thick Type)

Dimensions (Normal Bending)



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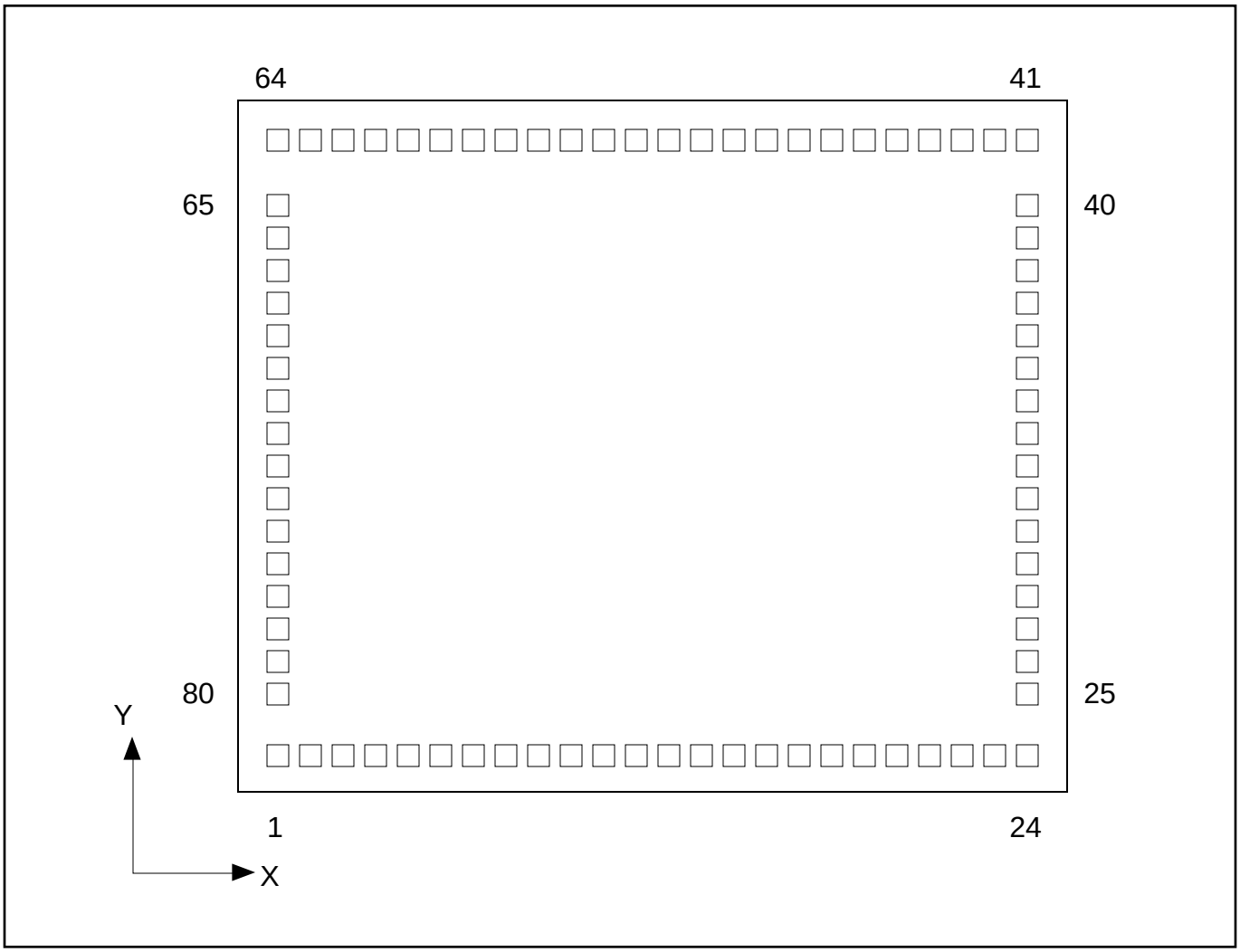
6.0 PAD LAYOUT

6.1 PAD LAYOUT



6.2 PAD COORDINATES

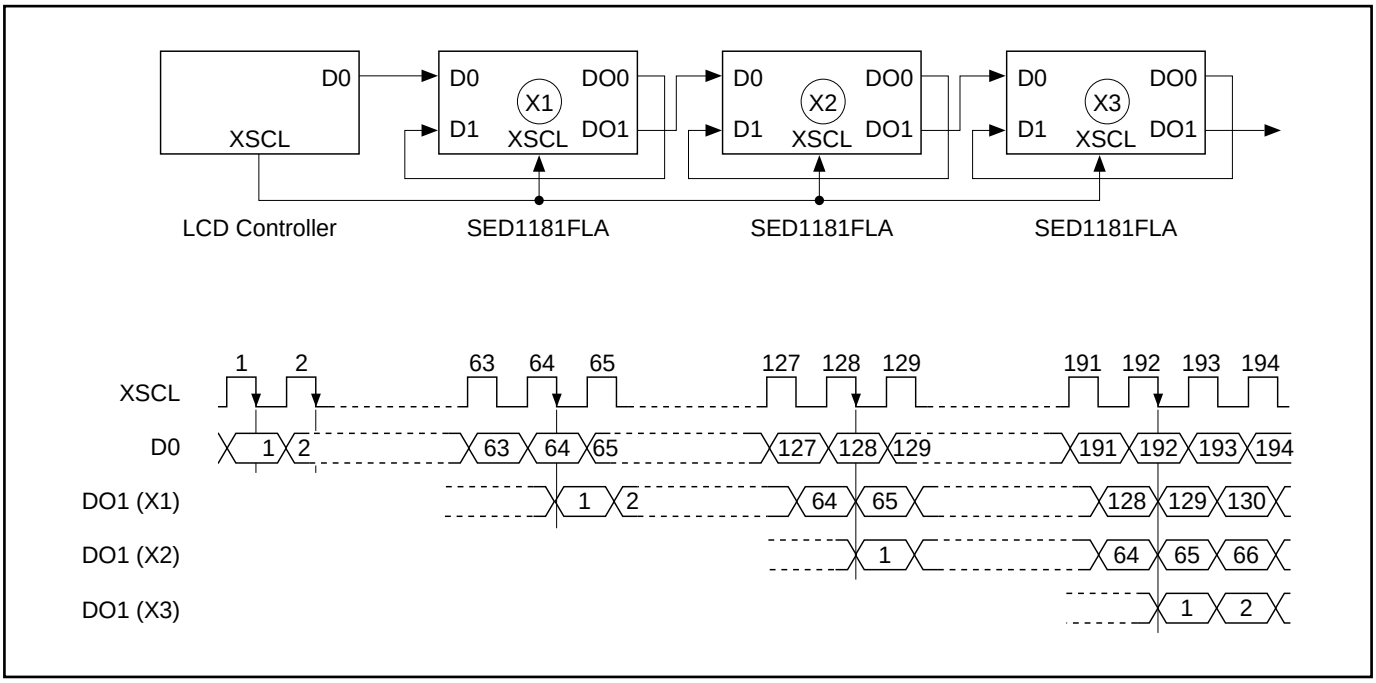
Pad		X (μm)	Y (μm)	Pad		X (μm)	Y (μm)	Pad		X (μm)	Y (μm)
Number	Name			Number	Name			Number	Name		
1	SEG27	155	155	28	SEG0	4690	916	55	SEG50	1947	3415
2	SEG26	423	155	29	DO0	4690	1107	56	SEG51	1756	3415
3	SEG25	614	155	30	NC	4690	1297	57	SEG52	1566	3415
4	SEG24	804	155	31	NC	4690	1488	58	SEG53	1375	3415
5	SEG23	995	155	32	D1	4690	1678	59	SEG54	1185	3415
6	SEG22	1185	155	33	D0	4690	1868	60	SEG55	995	3415
7	SEG21	1375	155	34	XSCL	4690	2059	61	SEG56	804	3415
8	SEG20	1566	155	35	LP	4690	2249	62	SEG57	614	3415
9	SEG19	1756	155	36	FR	4690	2440	63	SEG58	423	3415
10	SEG18	1947	155	37	SEG32	4690	2630	64	SEG59	155	3392
11	SEG17	2137	155	38	SEG33	4690	2820	65	SEG60	155	3201
12	SEG16	2327	155	39	SEG34	4690	3011	66	SEG61	155	3011
13	SEG15	2518	155	40	SEG35	4690	3201	67	SEG62	155	2820
14	SEG14	2708	155	41	SEG36	4690	3392	68	SEG63	155	2630
15	SEG13	2899	155	42	SEG37	4422	3415	69	V_{SSH}	155	2440
16	SEG12	3089	155	43	SEG38	4231	3415	70	V_2	155	2249
17	SEG11	3279	155	44	SEG39	4041	3415	71	V_3	155	2059
18	SEG10	3470	155	45	SEG40	3851	3415	72	V_{SS}	155	1868
19	SEG9	3660	155	46	SEG41	3660	3415	73	V_{DD}	155	1676
20	SEG8	3851	155	47	SEG42	3470	3415	74	DO1	155	1488
21	SEG7	4041	155	48	SEG43	3279	3415	75	NC	155	1297
22	SEG6	4231	155	49	SEG44	3089	3415	76	NC	155	1107
23	SEG5	4422	155	50	SEG45	2899	3415	77	SEG31	155	916
24	SEG4	4690	155	51	SEG46	2708	3415	78	SEG30	155	726
25	SEG3	4690	345	52	SEG47	2516	3415	79	SEG29	155	536
26	SEG2	4690	536	53	SEG48	2327	3415	80	SEG28	155	345
27	SEG1	4690	726	54	SEG49	2137	3415				

7.0 ADDITIONAL DESCRIPTION

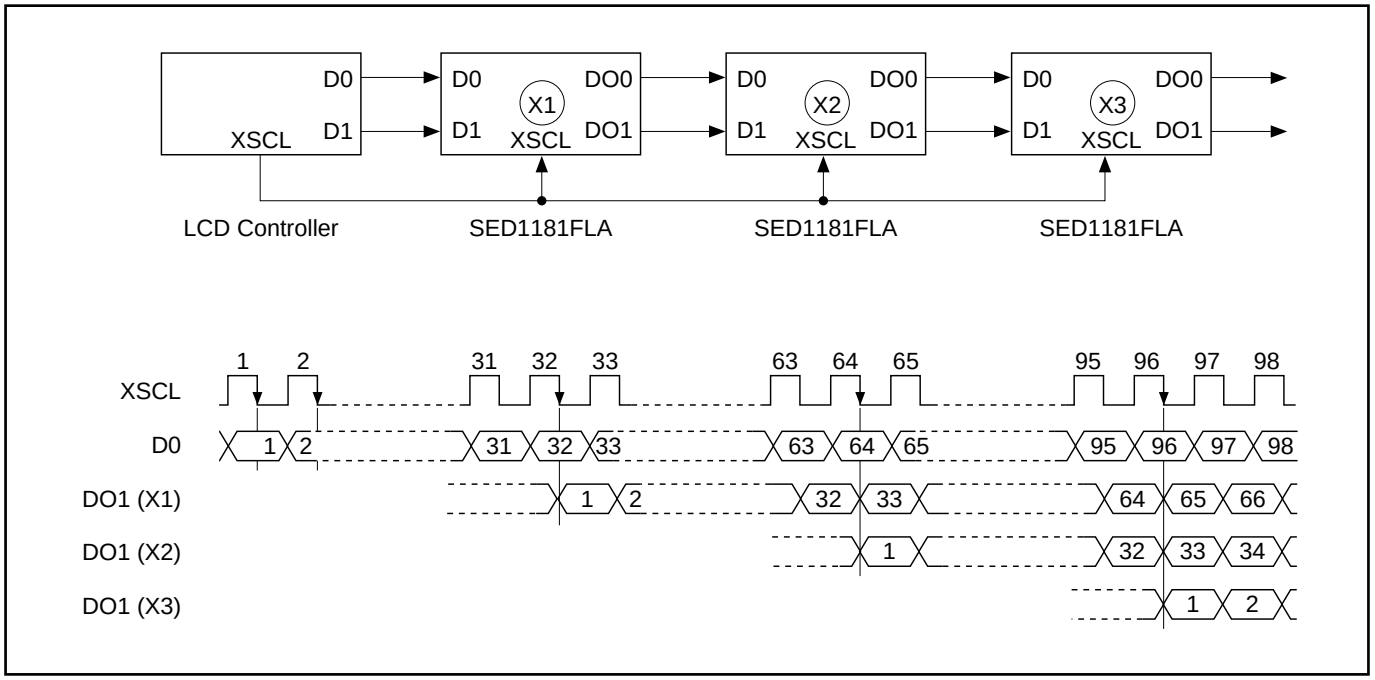
7.1 CASCADING THE SED1181F$_{LA}$

Two or more SED1181F$_{LA}$'s can be used in a cascaded configuration according to the display capacity requirements of the LCD panel.

The following figure shows a configuration example of three SED1181F$_{LA}$'s with the upper and lower shift registers serially connected.



Lower and upper shift registers of SED1181F$_{LA}$ are used independently.



On the falling edge of the shift clock, XSCL, a one-bit shift right is performed. Segment display data at D0 and D1 is shifted into the LSB registers and the data residing in the MSB registers (which is apparent at DO0 and DO1) will be overwritten by the preceding register's data.

7.2 POWER SOURCE FOR LCD DRIVE

7.2.1 Voltage Ratio

To ensure a high display quality, constant voltages, the ratio of which are precisely set, should be applied to LCD drive power pins.

The voltage ratio must be set according to the LCD drive duty ratio.

Example of Bias:

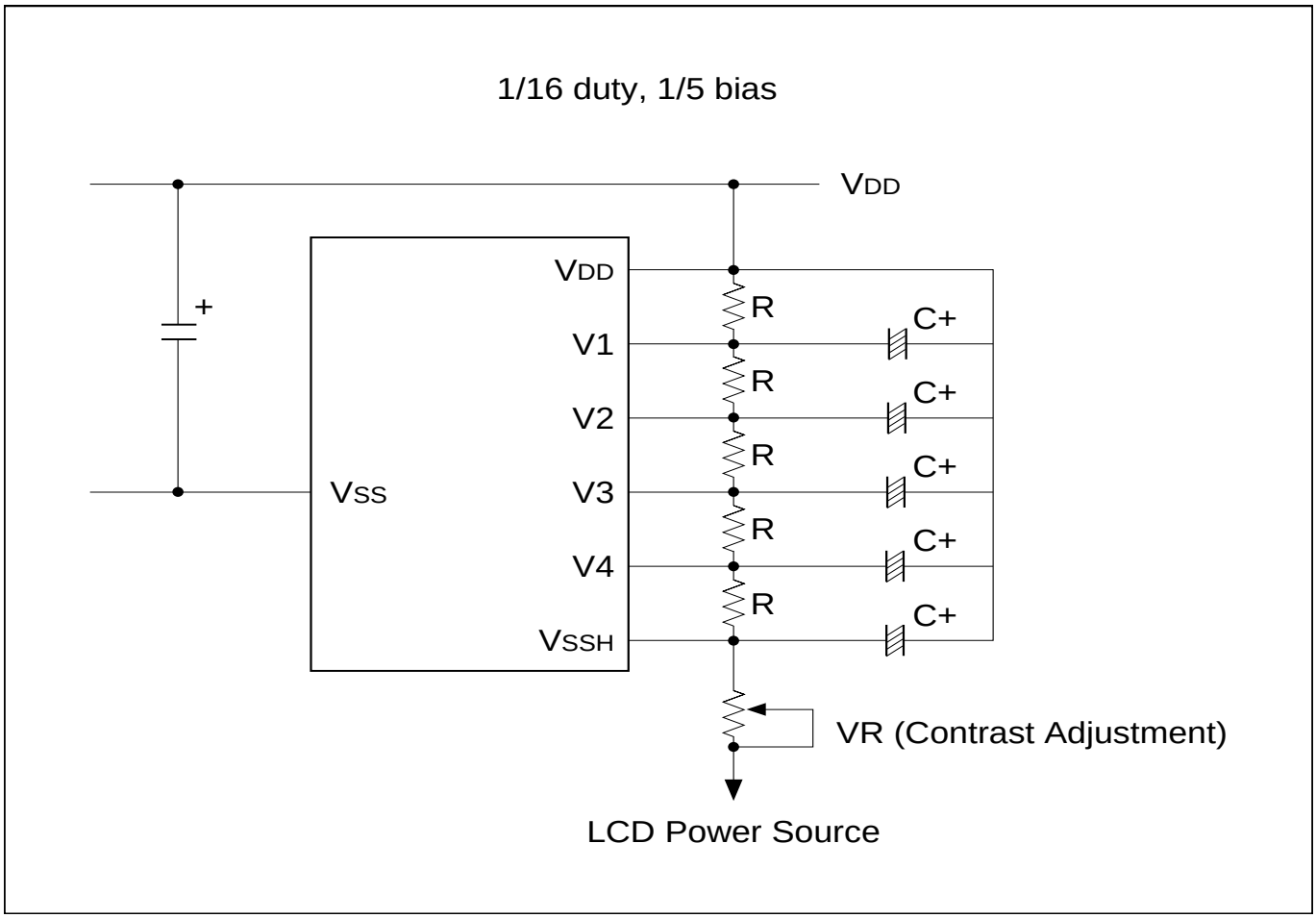
	Duty	**1/3**	**1/8**	**1/16**
Power	**Bias**	**1/3**	**1/4**	**1/5**
V_{DD}		V_{DD}	V_{DD}	V_{DD}
V1 *1		1/3 x V_{SSH}	1/4 × V_{SSH}	1/5 × V_{SSH}
V2		2/3 x V_{SSH}	2/4 × V_{SSH}	2/5 × V_{SSH}
V3		1/3 x V_{SSH}	2/4 × V_{SSH}	3/5 × V_{SSH}
V4 *1		2/3 x V_{SSH}	3/4 × V_{SSH}	4/5 × V_{SSH}
V_{SSH}		V_{SSH}	V_{SSH}	V_{SSH}

7.2.2 Power Supply to LCD by Voltage Divider

To obtain the voltage levels for V_{DD}, V_1, V_2, V_3 and V_{SSH}, it would be simplest to use a voltage divider made of resistors such as that shown on the next page. Since the optimum drive voltage for LCD's varies with the ambient temperature, a compensator (variable resistor VR) may be required in series with this divider.

Resistor values are determined in consideration of liquid crystal power consumption.

The next figure shows a typical voltage divider configuration used to supply power to the LCD.



Note: Set the LCD power source conditions so that V_{SSH} does not exceed its maximum rating when V_R is short-circuited.

The following describes distortion correction of the LCD drive signal waveform. The liquid crystal material of the LCD has inherent capacitive load characteristics. Therefore, when the LCD drive signal level changes, a large charge or discharge current flows and the drive signal waveform is distorted, resulting in poor display quality, e.g. reduced luminance and half-tones. To avoid this, voltage divider resistance and power supply impedance are lowered. However, this increases the current flowing through the voltage divider, resulting in increased power consumption by the module.

The resistor value of the voltage divider cannot always be determined according to the LCD load capacity; other LCD characteristics must also be considered.

Waveform distortion can be reduced by setting resistor value R smaller and connecting a proper value capacitor C to each resistor as shown in the figure above. Use such capacitors if necessary.

7.2.3 Precautions Concerning Power ON/OFF

The SED1181F$_{LA}$ requires two separate power sources. The logic system power supply and LCD system power supply. In addition, up to six levels of LCD drive voltage may be required, making the power supply system complex. Therefore, if a high voltage is applied to the LCD drive system with the logic system power supply placed in a floating or off status, excessive current will flow through the LSI possibly destroying it.

When the power is turned on or off, the following sequence of events must be observed:

Power On: In the sequence $V_{SS} \rightarrow V_{SSH}$ or simultaneously

Power Off: In the sequence $V_{SSH} \rightarrow V_{SS}$ or simultaneously

Note: To protect against excessive current, connect a 100 Ω (approximate) resistor in series with the V_{SSH} source and the LSI's.

7.3 CONFIGURATION EXAMPLE OF A DOT-MATRIX LCD MODULE

Using the SED1181F$_{LA}$ (X driver) and the SED1191F (Y driver), a dot matrix LCD module with medium pixel capacity and graphics capability can be easily configured.

Section 8.1 shows a configuration example of a 32x256 dot matrix LCD panel module.

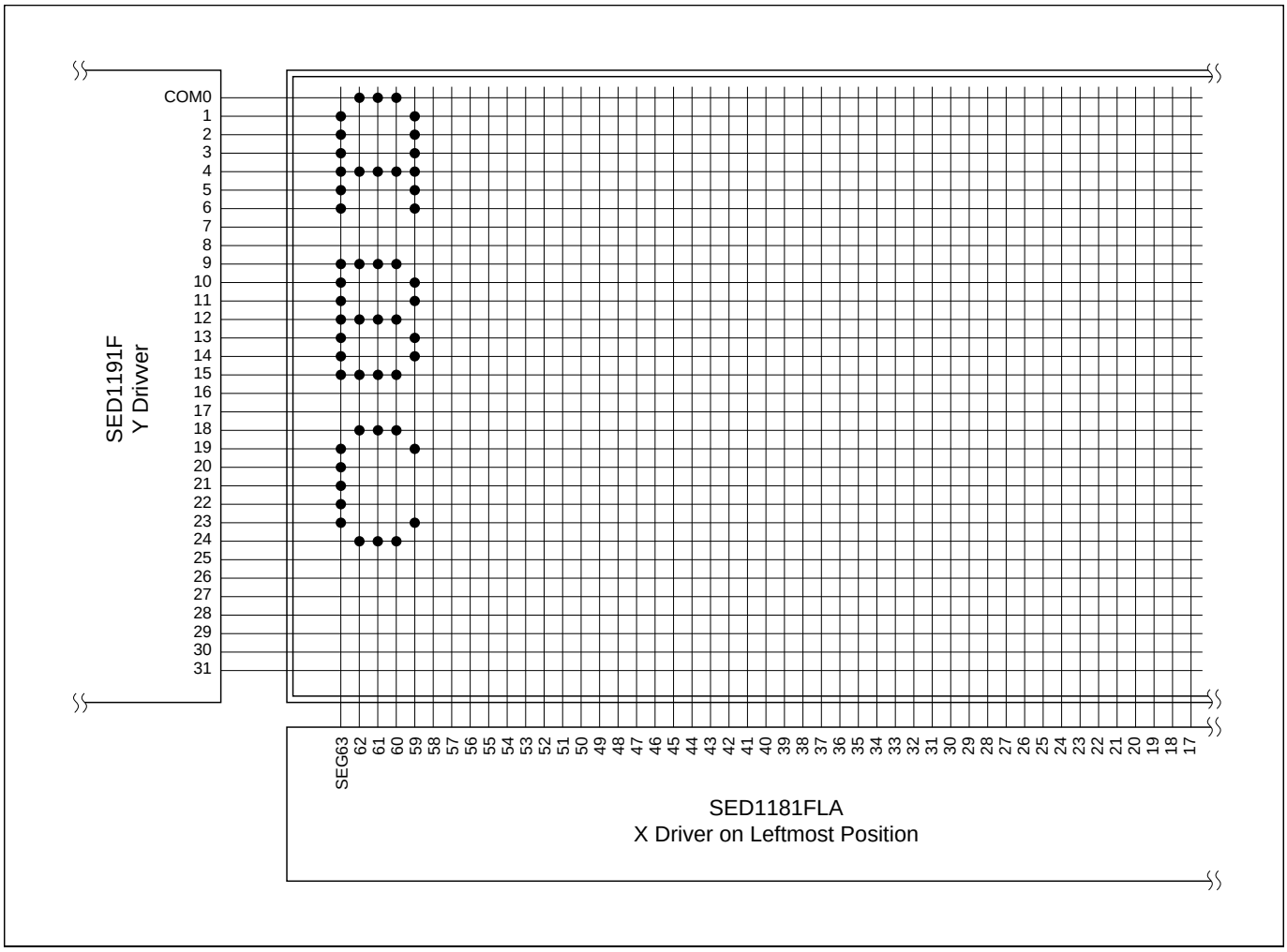
Moreover, the SED1181F$_{LA}$ is suitable for extending display the capability of a controller driver such as the SED1278F.

The SED1278F, in conjunction with the SED1181F$_{LA}$ in a slave configuration, can display up to 80 characters (400 segment drivers).

A configuration example is shown in Section 8.2.

7.4 LCD DISPLAY EXAMPLE AND LCD DRIVE FRAME SIGNAL

7.4.1 LCD Graphic Display Example at 1/32 Duty



7.4.2 Example of LCD Drive Signal

In general, there are two types of LCD drive systems, 1-frame AC drive type (hereafter referred to as A type) and 2-frame AC drive type (B type). The SED1181F$_{LA}$ can be used for both A and B types by changing the period of the frame signal FR.

As an example, Section 8.5 below shows a drive signal for the B type at 1/16 duty and 1/5 bias using the voltage averaging method.

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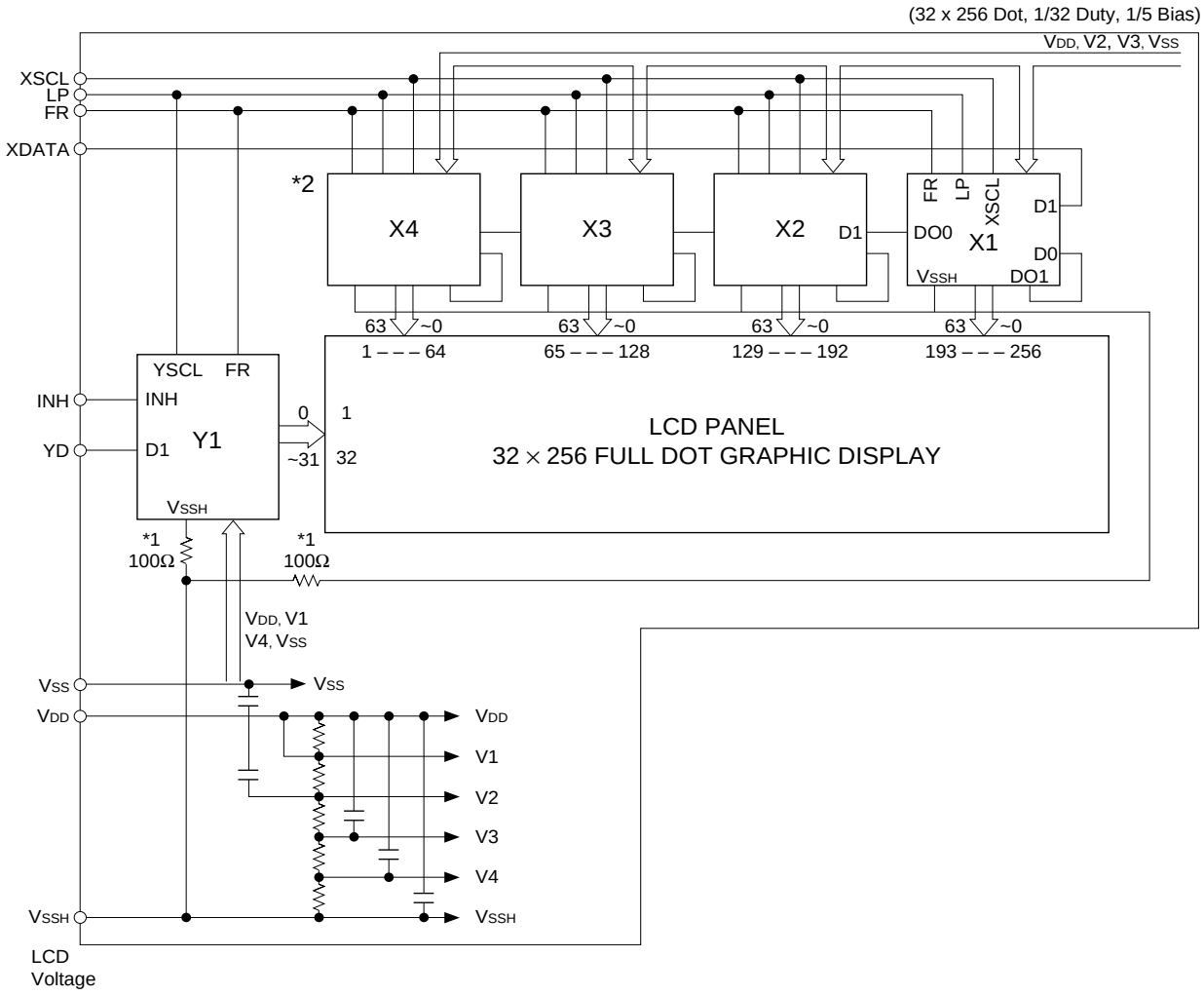
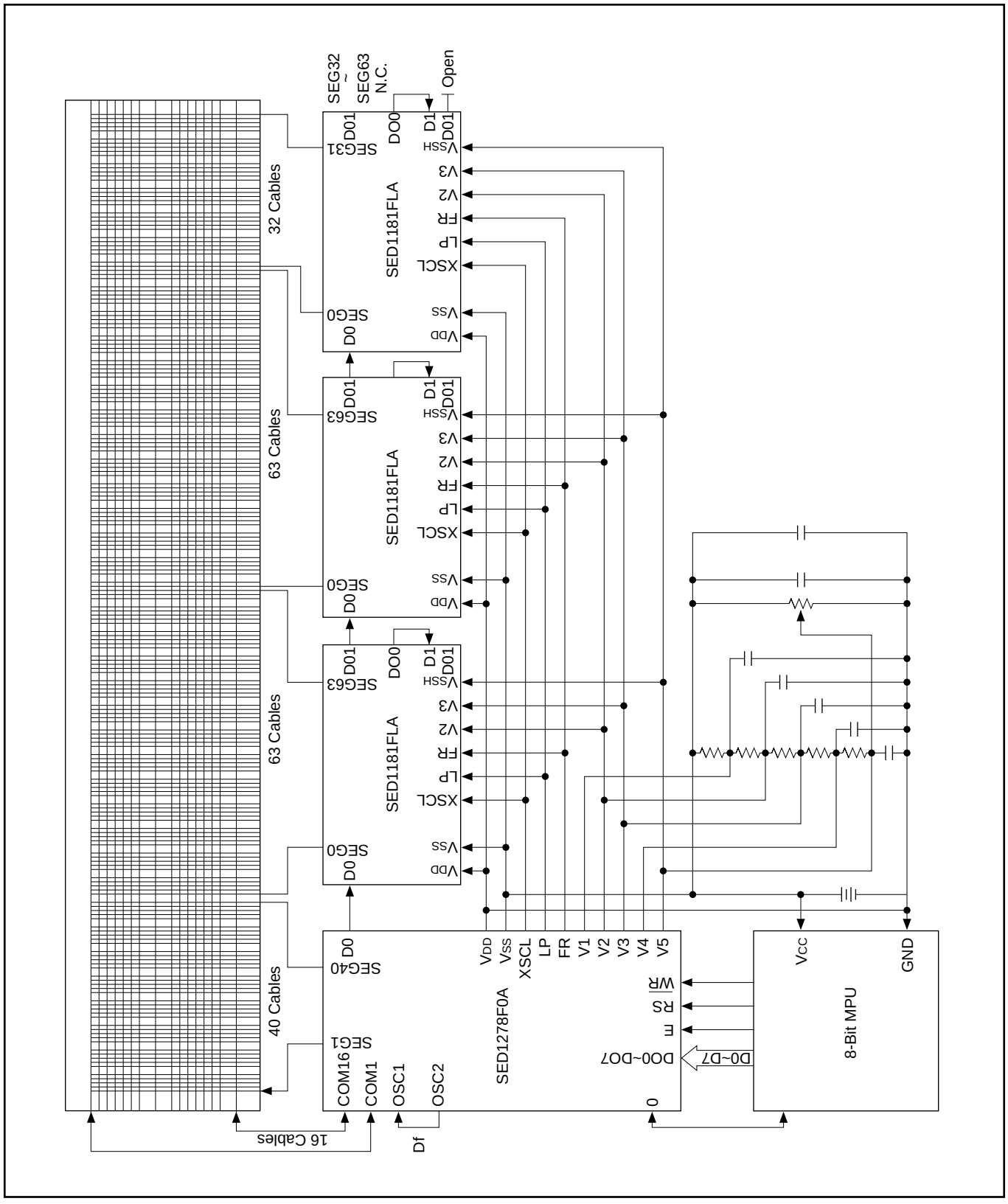
8.0 REFERENCE DRAWINGS

8.1 EXAMPLE OF LCD MODULE CONFIGURATION

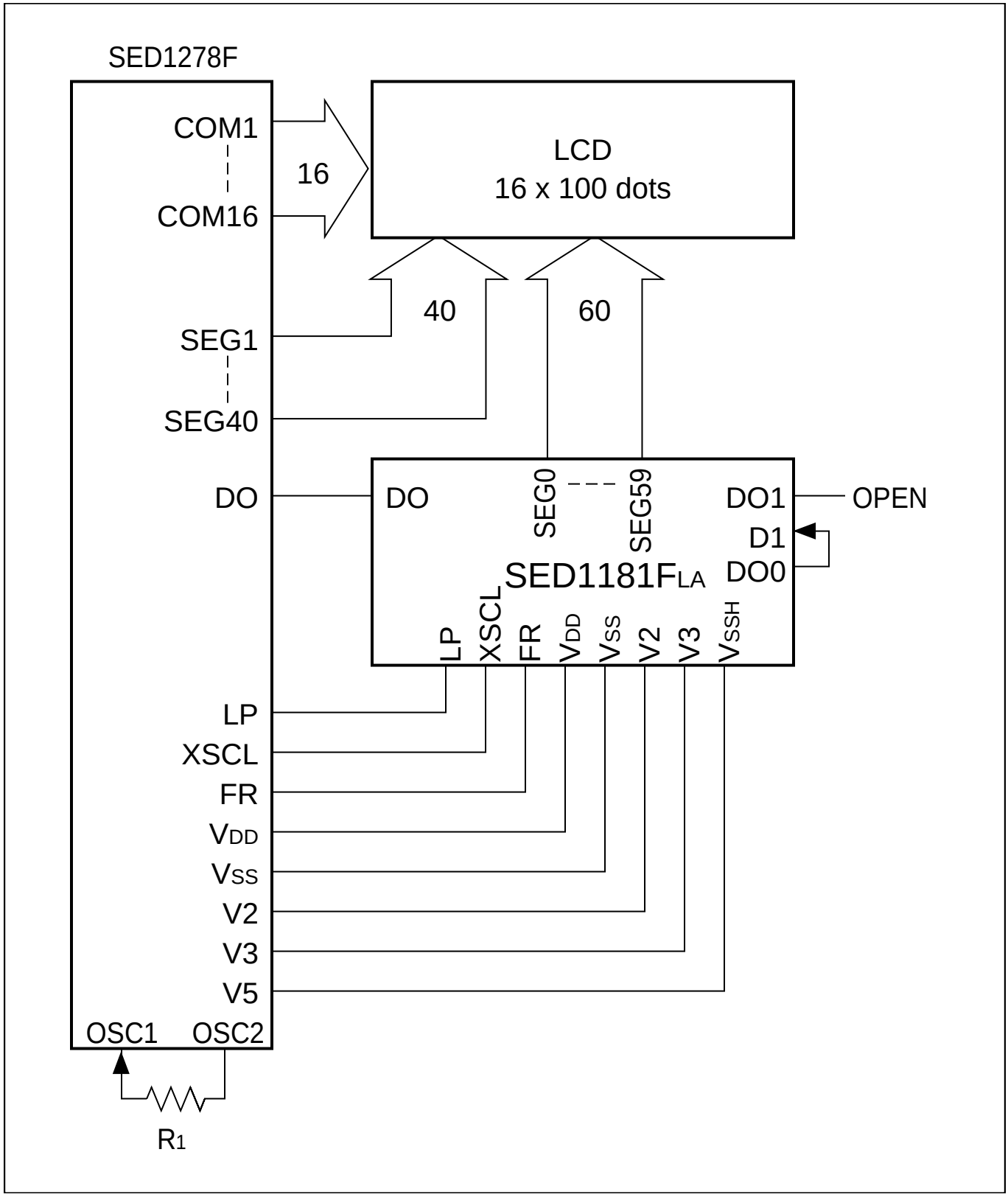


*1 Use to protect against excessive current.
*2 Use a bypass capacitor near the V_{SS} and V_{SSH} pins of each driver device to improve noise immunity.

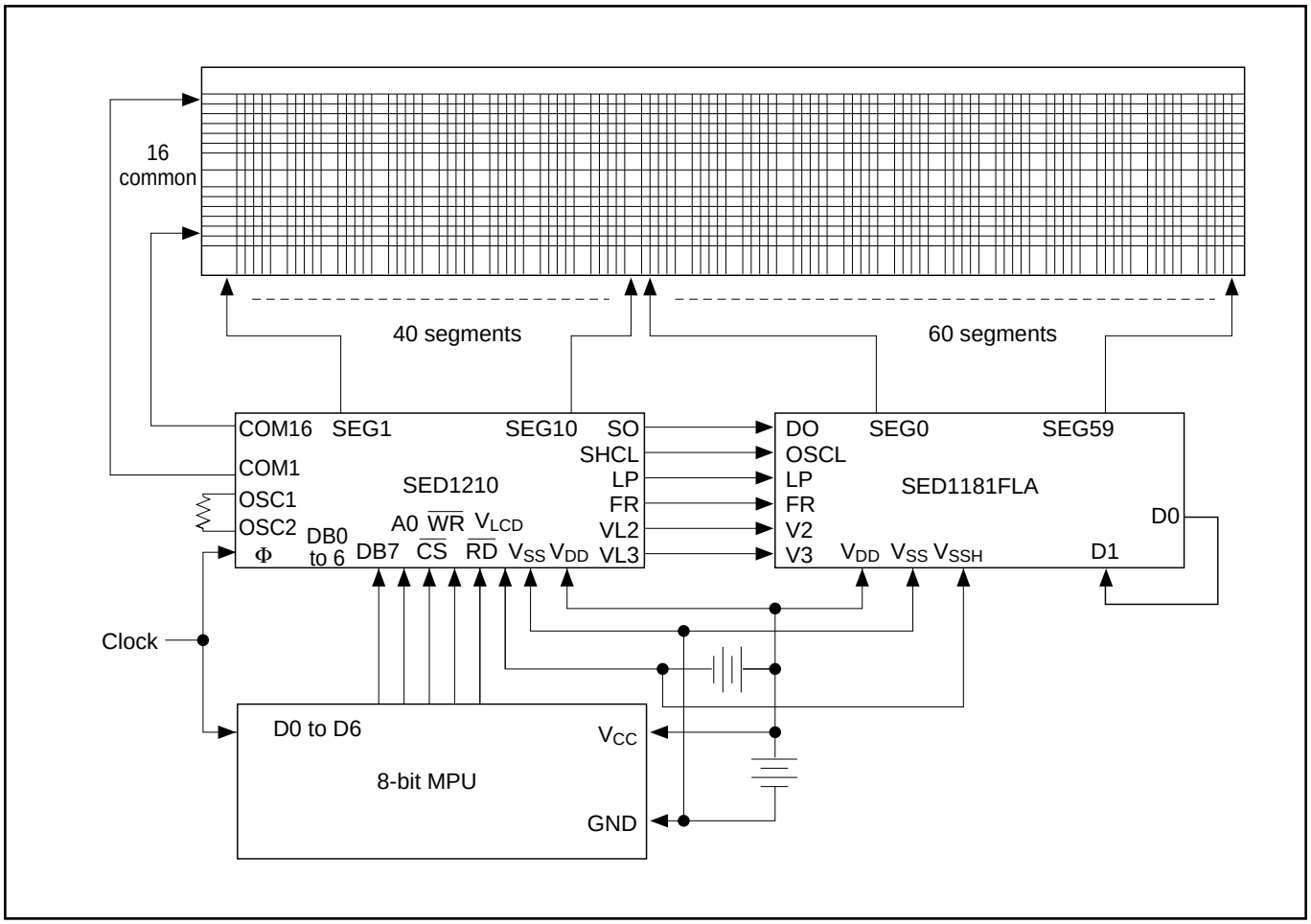
8.2 CONNECTION WITH SED1278F (1)



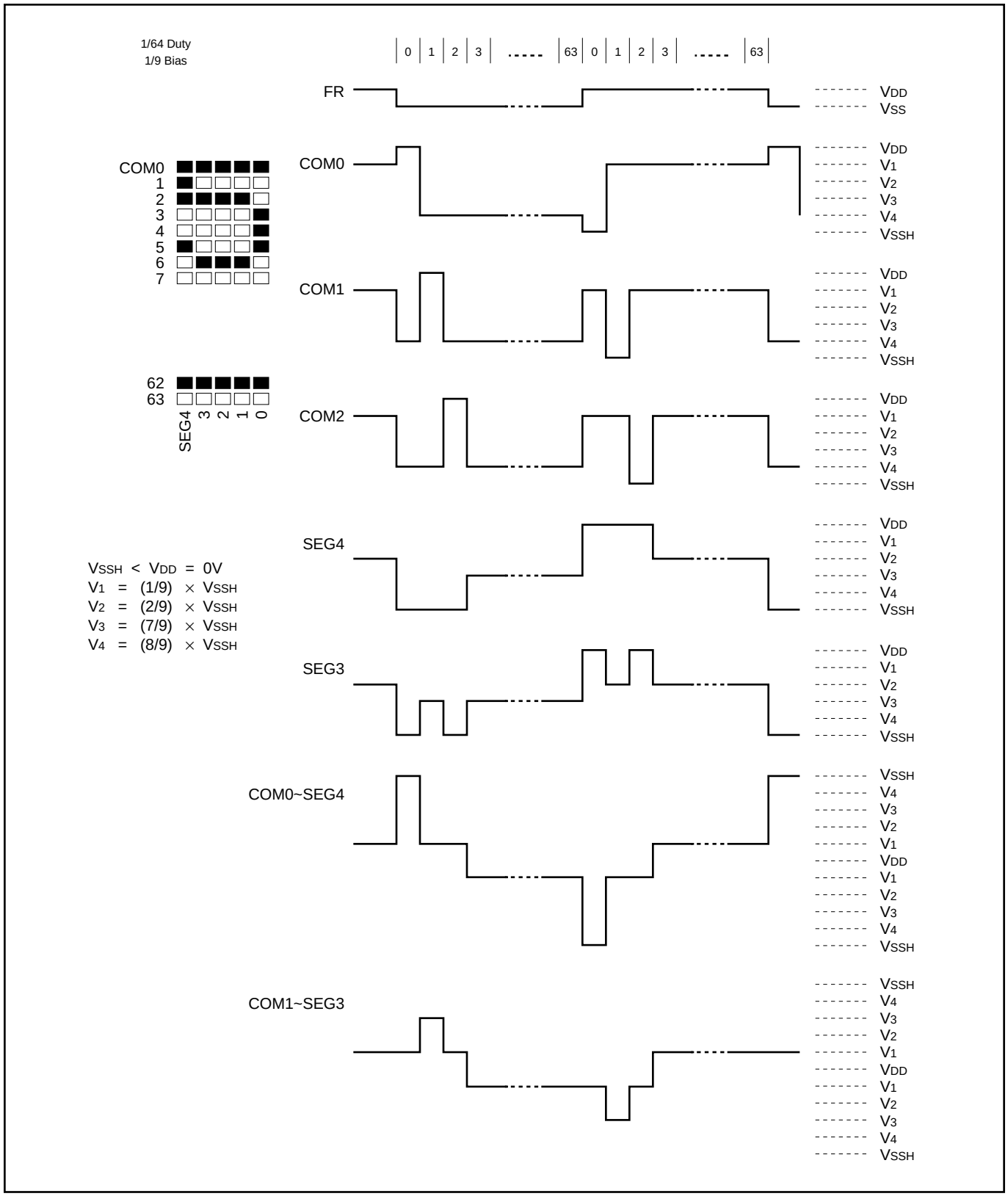
8.3 EXAMPLE OF 12 CHARACTERS, 4 LINES, 1/16 DUTY CYCLE



8.4 EXAMPLE OF 20 CHARACTERS, 2 LINES, 1/16 DUTY CYCLE



8.5 B-TYPE LCD DRIVE WAVEFORMS



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