SED17A0T

CMOS LCD SEGMENT DRIVER

■ DESCRIPTION

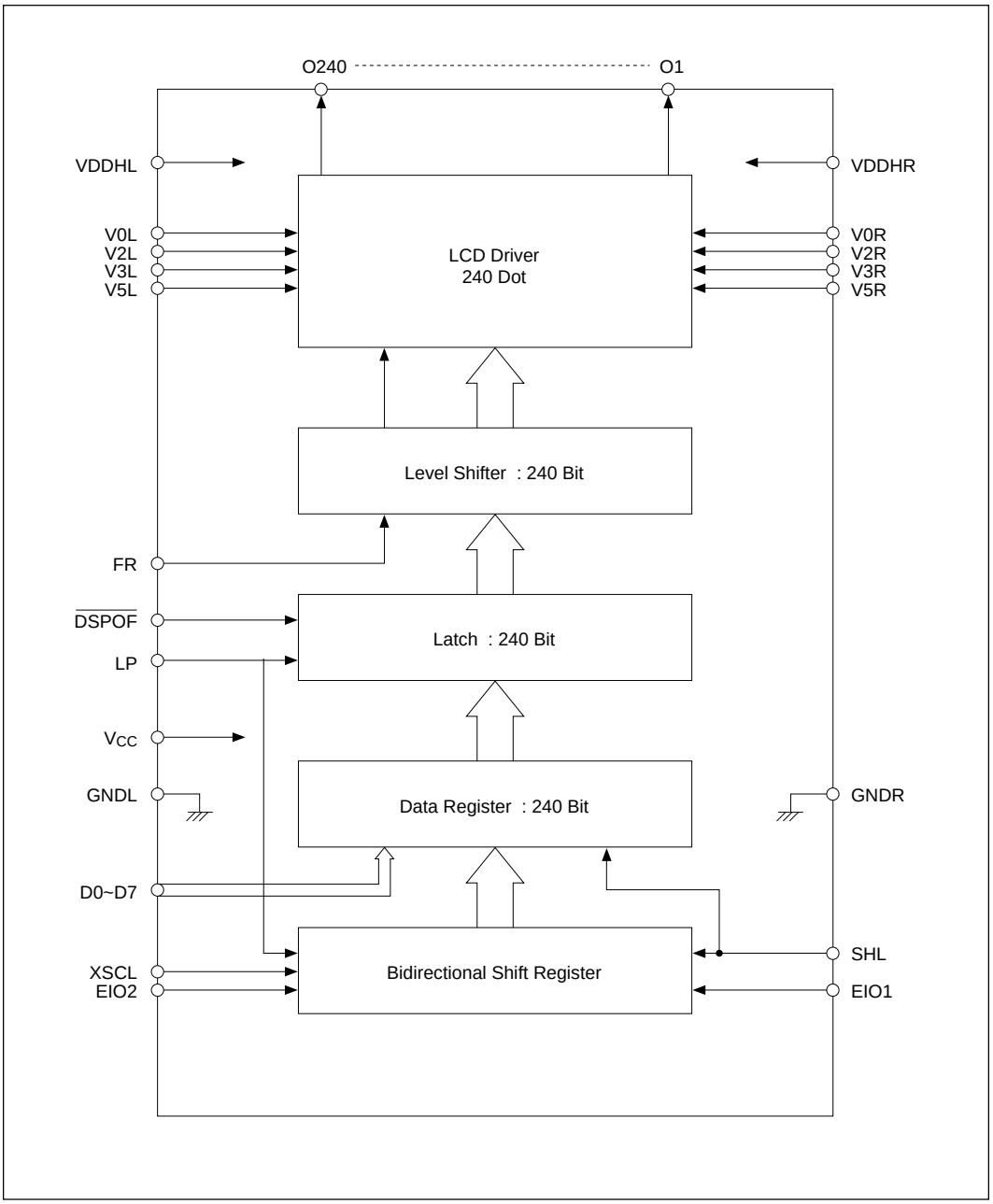
The SED17A0T is a segment LCD driver for dot-matrix STN liquid crystal display (LCDs). It incorporates 240 segment (column) driver outputs and is designed for use in conjunction with the SED1753 common (row) driver.

Contributing to making clearer LCD picture quality, this IC employs the high-speed enable chain method and is slim-chip configuration which is more advantageous for miniaturization of the LCD panel. SED17A0T is also capable of low-voltage and high-speed logic operations and fits to a wide range of applications.

■ FEATURES

- Number of LCD drive output segments 240
- Low voltage operation ..... 2.7V min.
- High duty drive ..... 1/500 (an example)
- Wide LCD drive voltage range ..... +8 to +42V (V_{DD} = 3 to 5.5V)
- High speed and low power consumption data transfer is possible by adoption of the 8-bit bus enable chain method:
  Shift clock frequencies: ..... 30.0MHz (5V±10%)
  20.0MHz (3.0V)
  18.0MHz (2.7V)
- Slim-chip configuration
- Non-bias display-off function
- Pin-selection of the output shift direction is available
- Offset bias regulation of LCD power for respective V_{DDH} and GND levels is possible
- Logic operation power supply ..... 2.7 to 5.5V
- Shipped status ..... TCP SED17A0T**
- This IC is not radiation resistant

■ **BLOCK DIAGRAM**



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Numbers of Pins</th></tr>
<tr><td>O 1 ~
O 240</td><td>O</td><td>LCD driveing segment (column) output
The output varies at the falling edge of LP .</td><td>240</td></tr>
<tr><td>D0 ~ D7</td><td>I</td><td>Display data input terminals</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>For input of the shift clock signals of the display data
(Falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>For input of the latch pulse signals of the display data
(Falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O
Set to I or O is determined by the SHL input level.
The output is reset by the LP input and when 240 bit
equivalent data are recieved, it falls to “L” automatically</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift durection selection, and EIO terminal I/O control
signal input
When data are input to terminals D0, D1, ...D7
in order of F0, F1, ...F7 first, and in the order of
L0, L1, outputs are as follows is as follows:
F (First), L (Last)
<table>
<tr><th>SHL</th><th colspan="7">Output</th><th colspan="2">EIO</th></tr>
<tr><td></td><td>0240</td><td>0239</td><td>0238</td><td></td><td>03</td><td>02</td><td>01</td><td>EIO1</td><td>EIO2</td></tr>
<tr><td>L</td><td>F7</td><td>F6</td><td>F5</td><td>....</td><td>L2</td><td>L1</td><td>L0</td><td>O</td><td>I</td></tr>
<tr><td>H</td><td>L0</td><td>L1</td><td>L2</td><td>....</td><td>F5</td><td>F6</td><td>F7</td><td>I</td><td>O</td></tr>
</table>
Note: The relation between the data and segment output are determined independently from the number of the shift clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>For input of alternating current LCD drive signals</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL,
GNDR</td><td>Power
supply</td><td>Logic operation power supply : GND: 0 V V_{CC}: +3, +5 V</td><td>3</td></tr>
<tr><td>V_{DDHL}, V_{DDHR}
V_{OL}, V_{OR}
V_{2L}, V_{2R}
V_{3L}, V_{3R}
V_{5L}, V_{5R}</td><td>Power
supply</td><td>LCD drive circuit power supply V_{DDH}
“ V0
“ V2
“ V3
“ V5</td><td>GND: 0 V, V_{DDH}: 14 –42V
$V_{DDH} \geq V_0 \geq V_2 \geq 7/9\ V_0$
$2/9\ V_0 \geq V_3 \geq V_5 \geq$ GND</td><td>10</td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>For forced bias fixed input
“L” level output is forcefully made to V5 level.
* When using this function, comvined use with SED1703
is not applicable</td><td>1</td></tr>
<tr><td></td><td></td><td>Total</td><td>268</td></tr>
</table>

■ FUNCTION OF EACH BLOCK

● Enable Shift Register

The enable shift register is a bidirectional shift register of which the shift direction is being selected by the SHL input and the shift register output is used to store data bus signals into the data register.

When the enable signal is in disabled state, the internal clock signal and the data bus are fixed to "L", thus going into a power saving mode.

When using multiple number of segment drivers, make cascade connection of EIO terminals of respective drivers to connect the EIO terminal of the top driver to "GND".

Since the enable control circuit automatically senses completion of receiving 240 bit equivalent data to transfer the enable signal automatically, control signal of a separate control LSI is not needed.

● Data Register

This register works to make series or parallel conversion of data bus signals according to the enable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independently from the number of shift clock inputs.

● Latch

It takes in the content of the data register at the falling edge trigger to transfer the output to the level shifter.

● Level Shifter

This is a level interface circuit to convert the voltage level of signals from the logic operation level to LCD drive level.

● LCD Driver

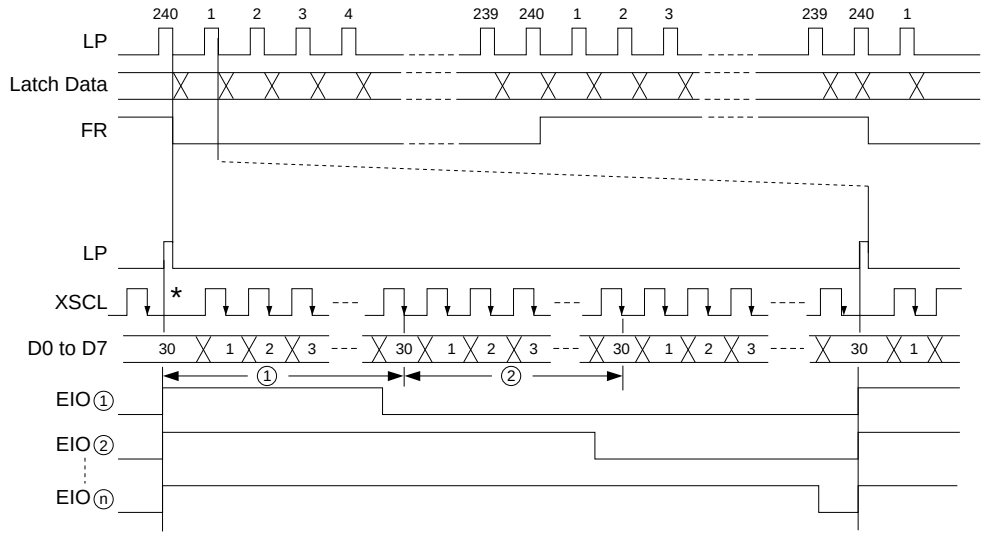
It outputs the LCD driving voltage.

Given below are the relations between data bus signals, alternating current signal FR levels and segment output voltages.

$\overline{\text{DSPOF}}$	Data Bus Signal	FR	Driver Output Voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_5

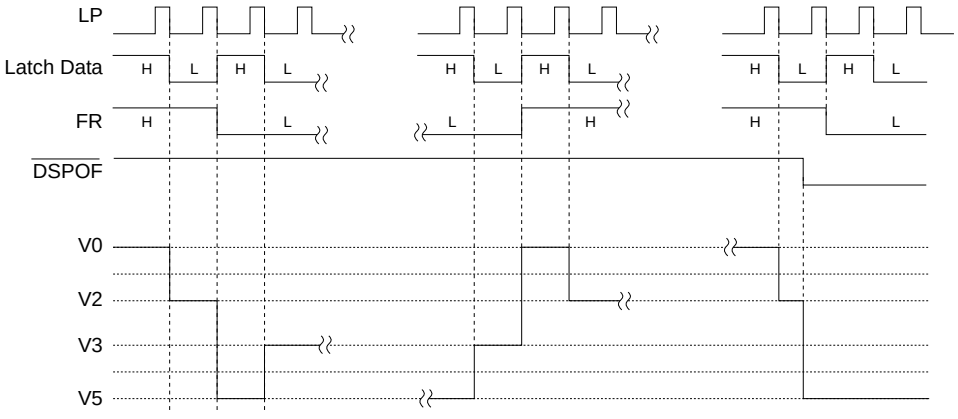
■ TIMING DIAGRAM

In case of 1/240 Duty (an example)



① to ⓝ stands for the cascade numbers of the driver.

* When making high speed data transfer, it becomes necessary to secure a longer XSCL cycle when determining the LP pulse insertion timing in order to maintain the specified value of LP → XSCL (t_{LH}).



■ ELECTRICAL CHARACTERISTICS

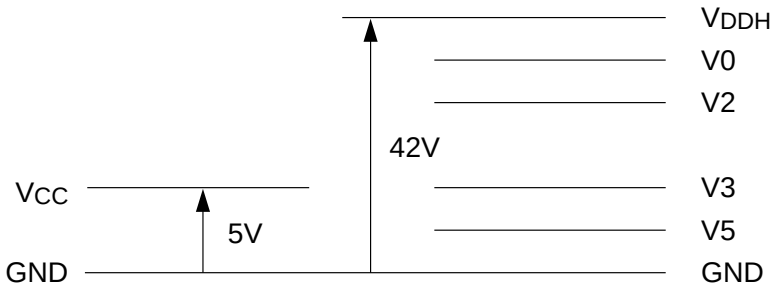
● Absolute Maximum Ratings

Parameters	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	–0.3 to V_{DDH} +0.3	V
Input voltage	V_I	–0.3 to V_{CC} +0.3	V
Output voltage	V_O	–0.3 V_{CC} +0.3	V
EIO output current	I_{O1}	20	mA
Working temperature	Topr	–30 to +85	°C
Storage temperature	Tstg	–55 to +100	°C

Note 1: All the voltage ratings are based on GND = 0V.

Note 2: The storage temperature 1 is applicable to independent chips and the storage temperature 2 is applicable to the TCP modular state.

Note 3: V_0, V_2, V_3 and V_5 should always be in the order of $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND.



Note 4: If the logic operation power goes into a floating state or if V_{CC} drops to 2.6V or below while the LCD driving power is being applied, the LSI may be damaged. Therefore, keep from occurrence of the aforementioned status.
Specifically, pay close attention to the power supply sequence at times of turning the system power on and off.

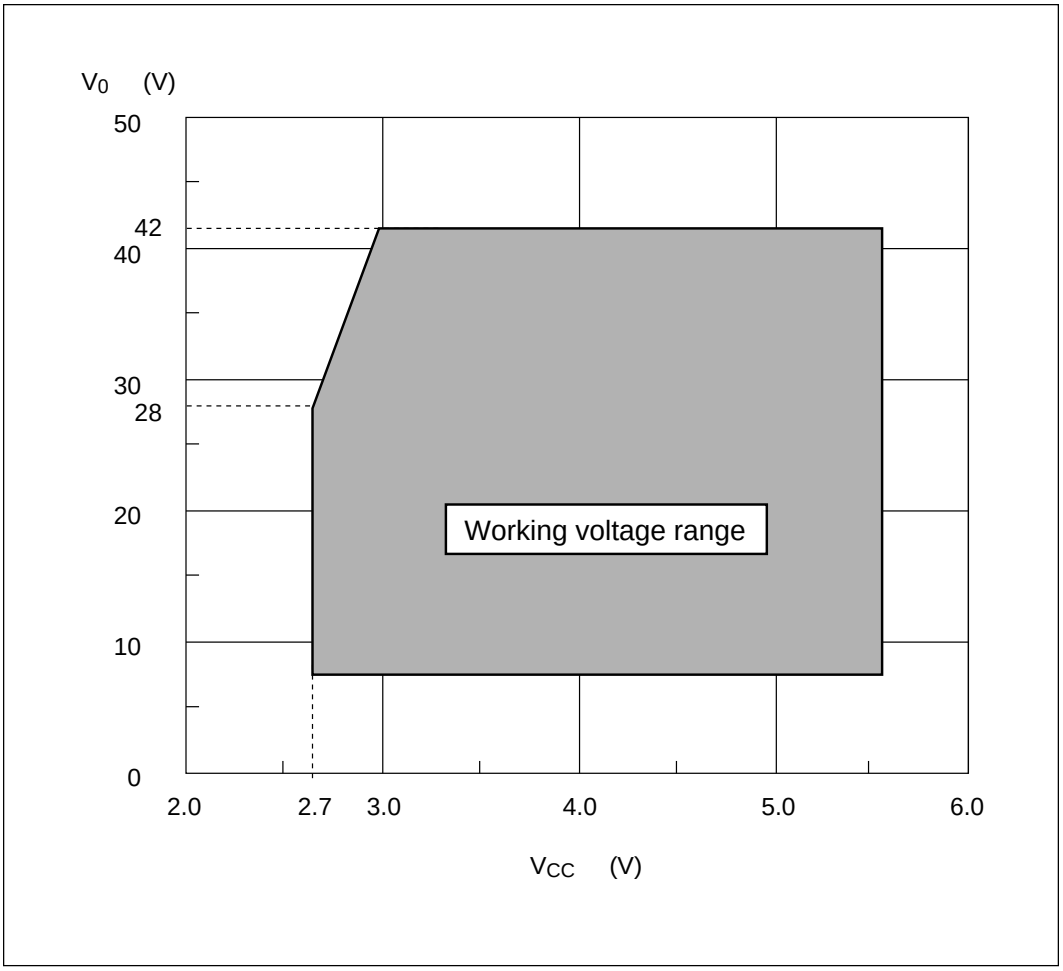
- **DC Characteristics**

Unless otherwise specified, GND = V5 = 0V, V_{CC} = +5.0V ± 10%, Ta = –30 to 85°C

Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
Supply voltage (1)	V_{CC}	—	V_{CC}	2.7	—	5.5	V
Recommended working voltage	V0	—	V0L, VDDHL	14.0	—	40.0	V
Workable voltage	V0	Function only	V0R, VDDHL	8.0	—	42.0	V
Supply voltage (2)	V_2	Recommended value	V2L, V2R	7/9 V_0	—	V_0	V
Supply voltage (3)	V_3	Recommended value	V3L, V3R	GND	—	2/9 V_0	V
High level input voltage	V_{IH}	V_{DD}= 2.7~5.5V	EIO1, EIO2, FR D0–D7, XSCL SHL, LP, DSPOF	0.8 V_{CC}	—	—	V
Low level input voltage	V_{IL}			—	—	0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC} = 2.7 – 5.5V, I_{OH} = –0.6mA	EIO1, EIO2	V_{CC}–0.4	—	—	V
Low level output voltage	V_{OL}	V_{CC} = 2.7 – 5.5V, I_{OL} = 0.6mA		—	—	0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	D0–D7, LP, FR XSCL, SHL DSPOF	—	—	2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ GND	EIO1, EIO2	—	—	5.0	µA
Static current	IGND	V_0 = 14.0 ~ 42.0V, V_{IH} = GND, V_{IL} = GND	GND	—	—	25	µA
Output resistance	R_{SEG}	ΔV_{ON} = 0.5V, Recommended condition, V_0 = +36.0V, 1/24, O0–O240		—	0.80	1.1	KΩ
		V_0 = +26.0V, 1/20		—	0.85	1.2	
In-chip deviation of output resistance	ΔR_{SEG}	ΔV_{ON} = 0.5V, V_0 = +36.0V, 1/24, 01–0240		—	—	95	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} = 5.38MHz, f_{LP} = 33.6KHZ, f_{FR} = 70Hz, input data: Checkered indication, no-load	V_{CC}	—	0.75	1.7	mA
		V_{CC} = +3.0V, Other conditons are the same as those when V_{CC} + 5V.		—	0.3	0.9	
Mean working current consumption (2)	I_O	V_O = +30.0V, V_{CC} = +5.0V, V3 = +4.0V, V_2 = +26.0V, V5 = +0.0V, Other conditions are the same as those in the I_{CC} column	V_0	—	0.25	1.4	mA
Input terminal capacity	CI	Freq. = 1 Mhz, Ta = 25°C, Independent chips	D0~D7, LP, FR XSCL,SHL, DSPOF	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

- **Working Voltage Range V_{CC} – V_0**

  The V_0 voltage should be set up within the V_{CC} – V_0 working voltage range given below.



- **AC Characteristics**
  - **Input Timing Characteristics**

Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	*2	33	—	ns
XSCL high level pulse duration	t_{WCH}	All timing signals are based on 20% and 80% of V_{CC}	9	—	ns
XSCL low level pulse duration	t_{WCL}		9	—	ns
Data setup time	t_{DS}		5	—	ns
Data hold time	t_{DH}		5	—	ns
XSCL → LP rise time	t_{LD}		–0	—	ns
LP → XSCL fall time	t_{LH}		25	—	ns
LP high level pulse duration	t_{WLH}	*1	15	—	ns
FR delay allowance	t_{DF}		-300	+300	ns
EIO setup time	t_{SUE}		5	—	ns
Input signal variation time	t_{r1}, t_{f1}	*3	—	50	ns
DSPOF signal variation time	fr_2, tf_2		—	100	ns

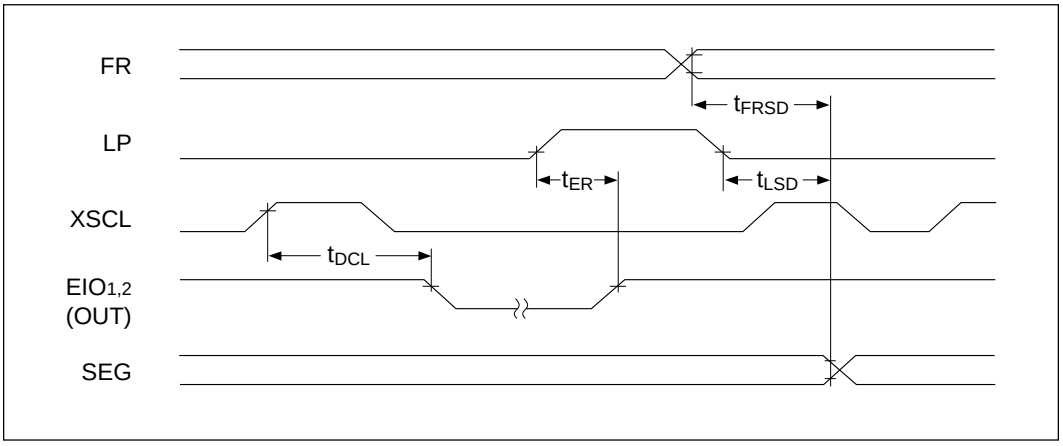
Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	V_{CC} = 3.0 to 4.5V	50	—	ns
		*2	55	—	ns
XSCL high level pulse duration	t_{WCH}	All timing signals are based on 20% and 80% of V_{CC}	15	—	ns
XSCL low level pulse duration	t_{WCL}		15	—	ns
Data setup time	t_{DS}		10	—	ns
Data hold time	t_{DH}		10	—	ns
XSCL → LP rise time	t_{LD}		–0	—	ns
LP → XSCL fall time	t_{LH}		30	—	ns
LP high level pulse duration	t_{WLH}	*1	25	—	ns
FR delay allowance	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		10	—	ns
Input signal variation time	t_r, t_f	*3	—	50	ns
DSPOF signal variation time	fr_2, tf_2		—	100	ns

Notes: *1. The "t_{WLH}" specifies the time when the LP is set at "H" and, at the same time, when XSCL is at "L", when LP is being input while XSCL is at "L".

*2. High speed operation of the shift clocks (XSCL) should only be made under a condition of $t_r + t_f \leq (t_C - t_{WCL} - t_{WCH})$.

*3. When the making high speed data transfer using conditions shift clocks, $t_r + t_f$ of the LP signals should be up to ($t_C + t_{WCH} - t_{LD} - t_{WLH} - t_{LH}$) at the maximum.

○ **Output Timing Characteristics**



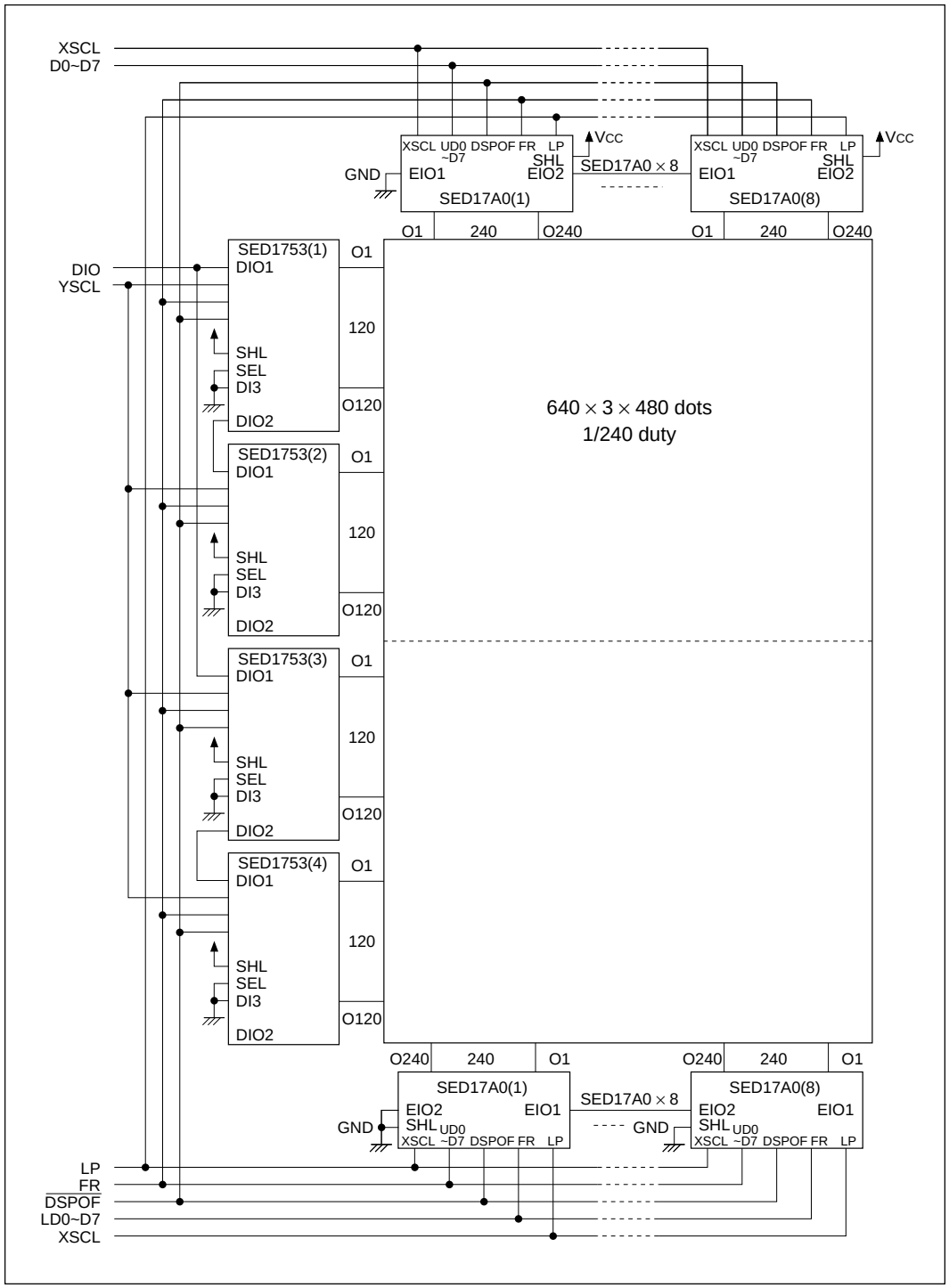
V_{CC} = +5.0V ± 10%, V_0 = +14.0 to +42.0V

Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EI0)	—	50	ns
EIO output delay time	t_{DCL}		—	25	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (0 n)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	400	ns

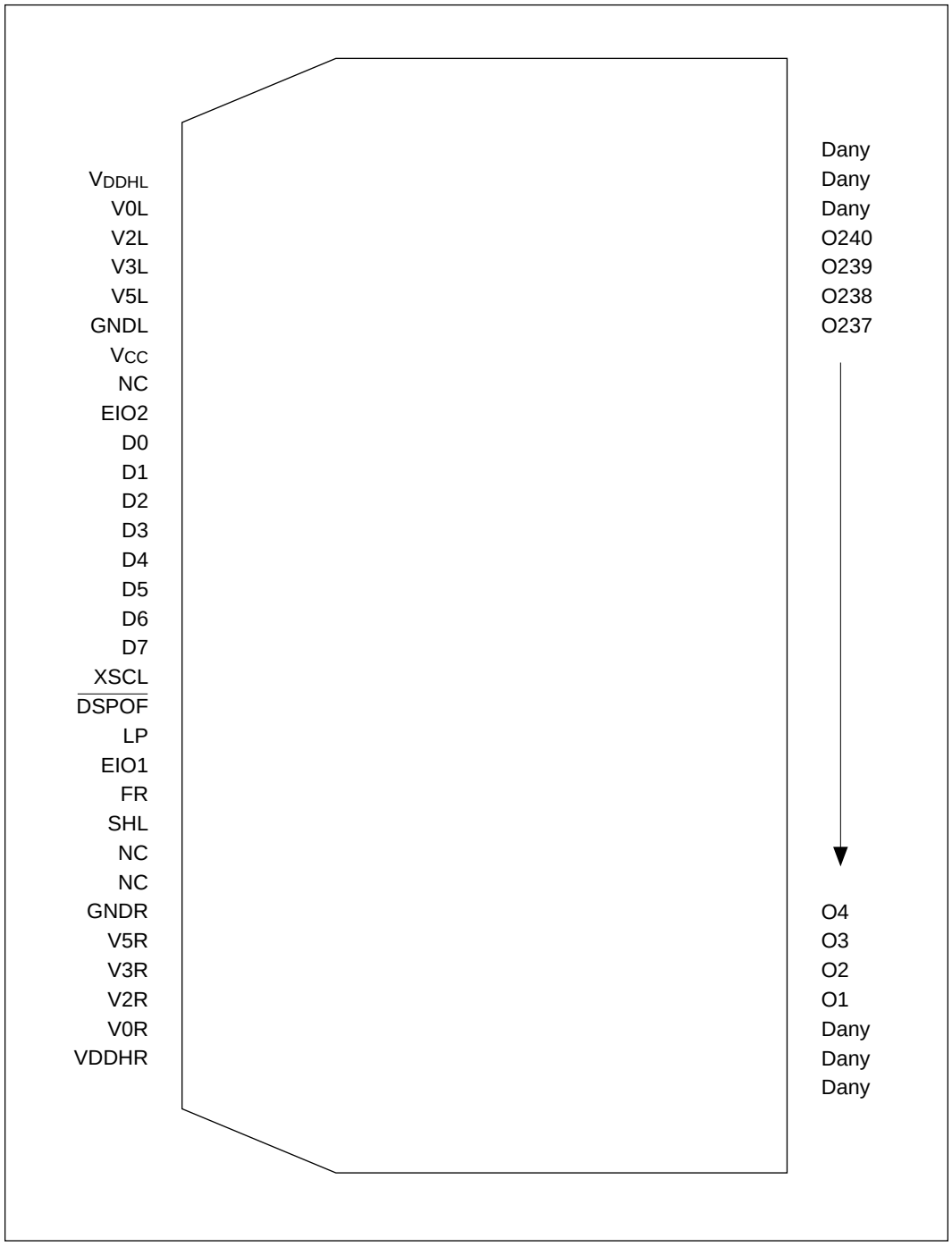
V_{CC} = +2.7 to 4.5V, V_0 = +14.0 to +28.0V

Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EI0)	—	80	ns
EIO output delay time	t_{DCL}		—	50	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (0 n)	—	400	ns
FR → SEG output delay time	t_{FRSD}		—	800	ns

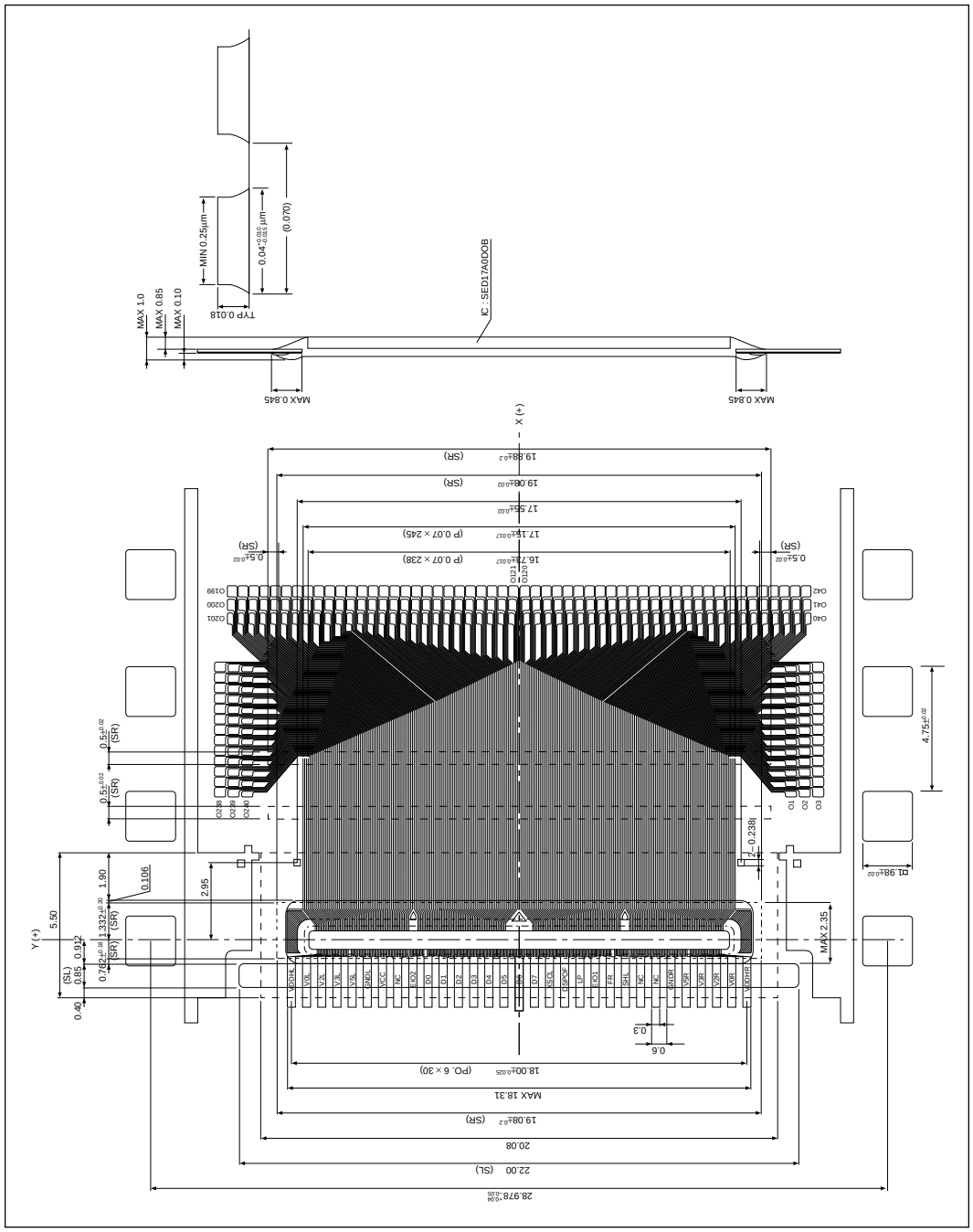
■ **A CONNECTION EXAMPLE**



■ **TCP PIN ARRANGEMENT EXAMPLE (FOR REFERENCE)**



■ PACKAGE DIMENSIONS



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