SED1681

80-BIT EXPANSION LCD DRIVER

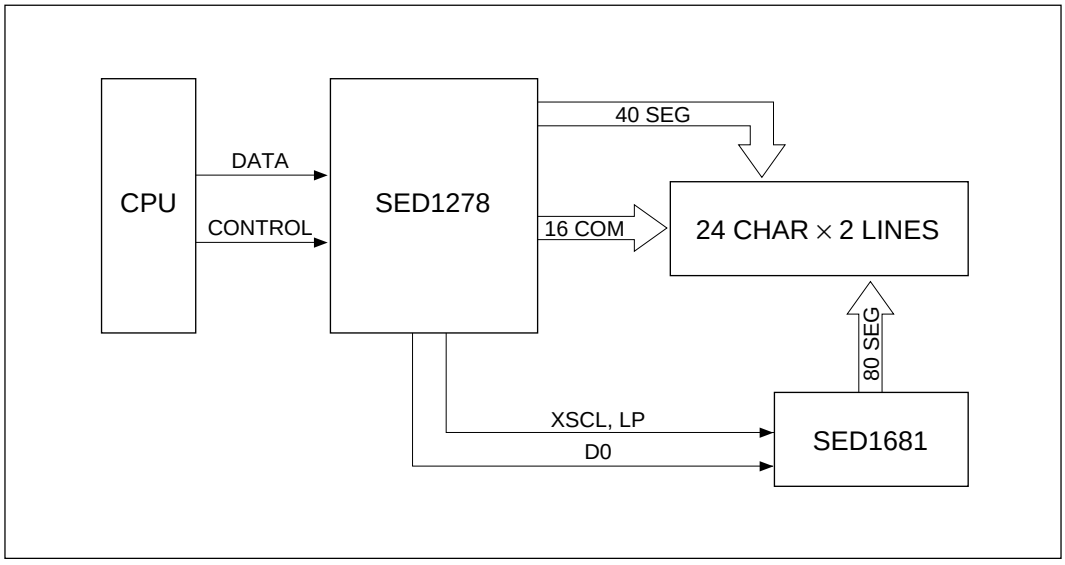
■ DESCRIPTION

The SED1681 is an 80-bit expansion segment (column) driver suitable for driving high-contrast, small-capacity dot matrix liquid crystal displays with a duty from 1/8 to 1/32. It is best suited for expanding the segment drive capability of LCD controllers such as the SED1278F, or a 4-bit microcomputer.

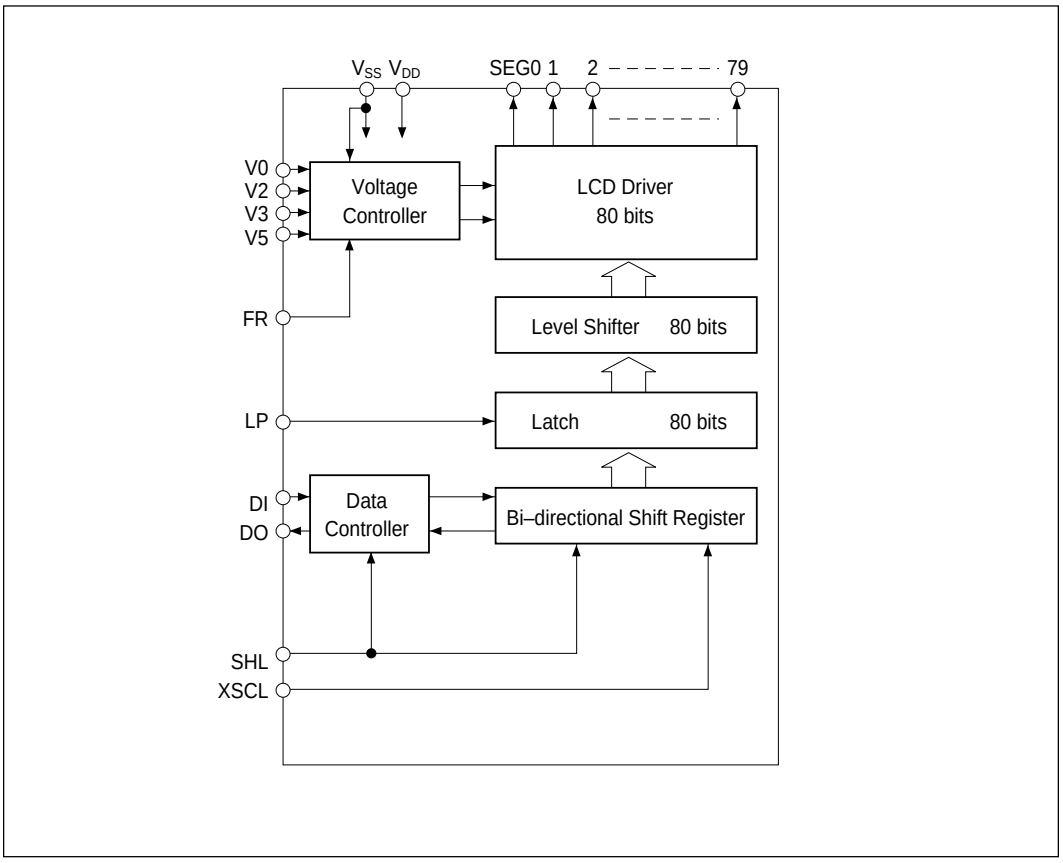
■ FEATURES

- Low-power CMOS technology
- 80-bit segment (column) driver
- Serial input data
- Duty cycle ..... 1/8 to 1/32
- Suitable for use with a wide range of LCD controllers
- Capable of a serial cascade connection
- Wide range of LCD voltage ..... –3.0V to –12V
- Supply voltage ..... 2.4V to 6.0V
- Package ..... QFP5-100 pin (F_{0A})
  DIE: Al pad chip (D_{0A})

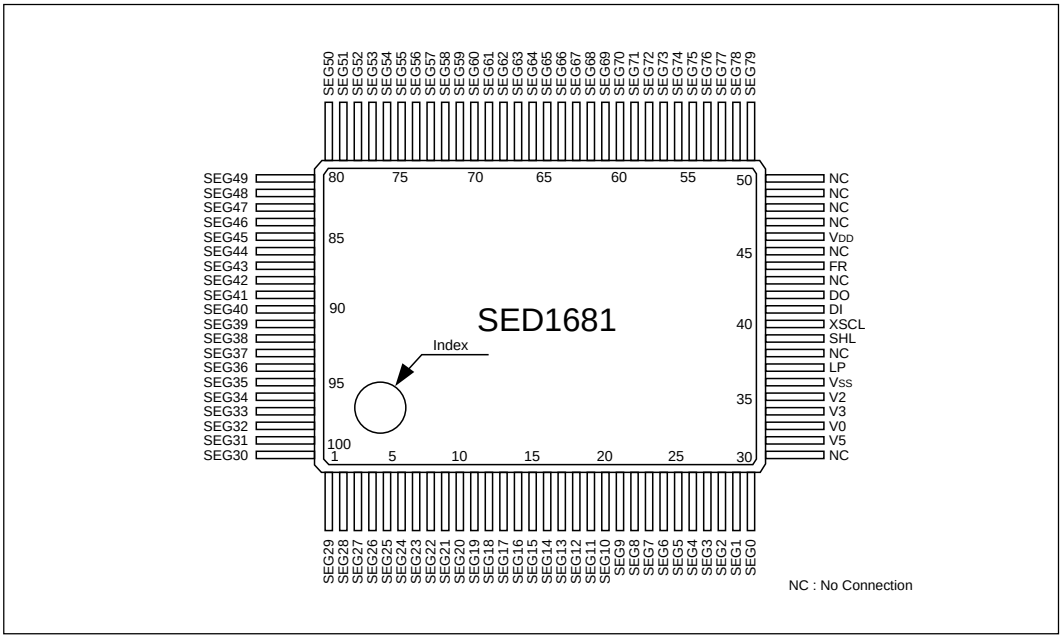
■ SYSTEM BLOCK DIAGRAM



■ **BLOCK DIAGRAM**



■ PINOUT



■ PIN DESCRIPTION

Pin/Pad		Input/ Output	Description
Number	Name		
1 to 30, 51 to 100	SEG0 to SEG79	O	Liquid crystal segment drive outputs Segment outputs change on the falling edge of the LP input signal.
40	XSCL	I	Shift clock input Shift register data is shifted on the falling edge of this signal.
37	LP	I	Display data strobe. Data from the shift register is strobed on to the display data latch on the falling edge of this signal.
41	DI	I	Serial data input
42	DO	O	Serial data output
39	SHL	I	Shift direction select This pin selects the data shift direction from bit 0 towards bit 79 or in reverse.
44	FR	I	Liquid crystal frame signal input
46	V_{DD}	—	Logic power supply
36	V_{SS}	—	Ground
32 to 35	V_0, V_2, V_3, V_5	—	LCD drive voltage supply inputs These voltages should satisfy the following conditions: $V_{DD} \geq V_0$, $V_{DD} \geq V_2 \geq 1/2 \times V_5$, $1/2 \times V_5 \geq V_3 \geq V_5$
31, 38, 43, 45, 47 to 50	NC	—	No connection

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to 0.3	V
Supply voltage (2)	V_5	–15.0 to 0.3	V
Supply voltage (3)	V_0, V_2, V_3	–15.0 to 0.3	V
Input voltage	V_{IN}	V_{SS} –0.3 to 0.3	V
Output voltage	V_O	V_{SS} –0.3 to 0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature, time	T_{sol}	260°C, 10 sec (at lead)	—

Notes:

1. All voltages are based on V_{DD} = 0V.

2. Never use wave soldering to mount packages, or any other method that applies excessive thermal stress to a package, as this will reduce its heat dissipation capacity.

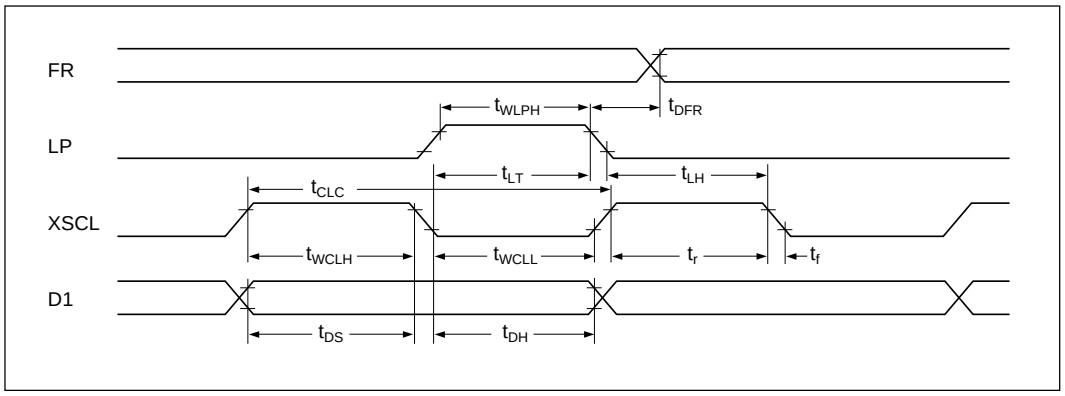
● **DC Electrical Characteristics**

(Unless otherwise specified, V_{DD} = V0 = 0 V, V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Supply voltage (1)	V_{SS}		V_{SS}	–6.0	–5.0	–2.4	V
Recommended operating voltage	V_5		V_5	–12.0	—	–3.0	V
Permitted operating voltage	V_5	Operational limits *1	V_5	–12.0	—	–2.5	V
Supply voltage (2)	V_2	Recommended value	V_2	1/2 × V_5	—	V_{DD}	V
Supply voltage (3)	V_3	Recommended value	V_3	V_5	—	1/2 × V_5	V
High-level input voltage	V_{IH}		DI, XSCL LP, SHL, FR	0.2xV_{SS}	—	V_{DD}	V
Low-level input voltage	V_{IL}			V_{SS}	—	0.8xV_{SS}	V
High-level output voltage	V_{OH}	I_{OH} = –0.6 mA	DO	–0.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{SS}	SHL, FR XSCL, LP	—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{SS}	DO	—	0.05	5.0	µA
Quiescent current	I_Q	V_5 = –12.0 V V_{SS} = –6.0 V, V_{IH} = V_{CC}	V_{DD}	—	0.05	30	µA
Output resistance	R_{SEG}	ΔVON = 0.1 V, T_a = 25°C, V_5 = –8.0V	SEG0 to SEG79	—	1.5	3.0	kΩ
		ΔVON = 0.1 V, T_a = 25°C, V_5 = –5.0V		—	3.0	8.0	
		ΔVON = 0.1 V, T_a = 25°C, V_5 = –3.0V		—	10.0	50.0	
Supply current (1)	$I_{SS\ OP}$	V_{SS} = –5.0 V, V_{IH} = V_{DD} V_{IL} = V_{SS}, LP = 520 µs, f_{XSCL} = 400 kHz., FR = 16.7 ms, all data inputs are alternate I and O data, all output open.	V_{SS}	—	250	350	µA
Supply current (2)	$I_{5\ OP}$	V_{SS} = –4.5V, V_2 = –4.8V V_3 = –7.2 V, V_{SSH} = –12.0 V; Other conditions as for $I_{SS\ OP}$	V_5	—	10	16	µA
Input pin capacitance	C_{IN}	T_a = 25°C	SHL, FR XSCL, LP	—	5	8	pF

*1. This parameter specifies the range of V5 over which operation is possible. The driver ON-resistance for the particular LCD panel being used may result in V5 exceeding the recommended operating range. The V5 operating voltage should be determined experimentally and component changes made, if necessary, to ensure operation within the recommended range

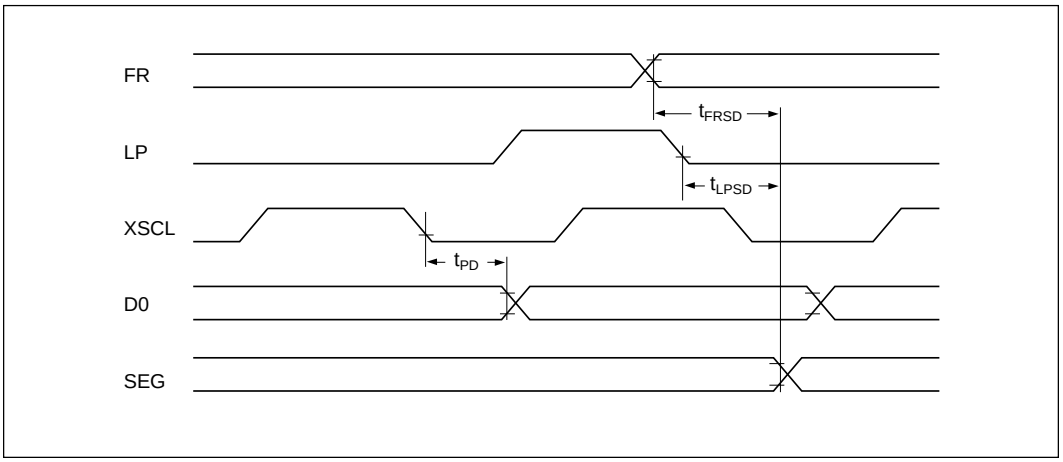
- **AC Electrical Characteristics**
  - **Input Timing**



(V_{SS} = –6.0 V to –2.4 V, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Shift clock period	t_{CLC}		1.0	—	—	µs
Shift clock High-level pulse width	t_{WCLH}		450	—	—	ns
Shift clock Low-level pulse width	t_{WCLL}		450	—	—	ns
Data setup time	t_{DS}		140	—	—	ns
Data hold time	t_{DH}		100	—	—	ns
Latch pulse High-level pulse width	t_{WLPH}		200	—	—	ns
Shift clock to latch pulse interval	t_{LT}		200	—	—	ns
Latch hold time	t_{LH}		100	—	—	ns
Frame signal delay time	t_{DFR}		–500	—	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns

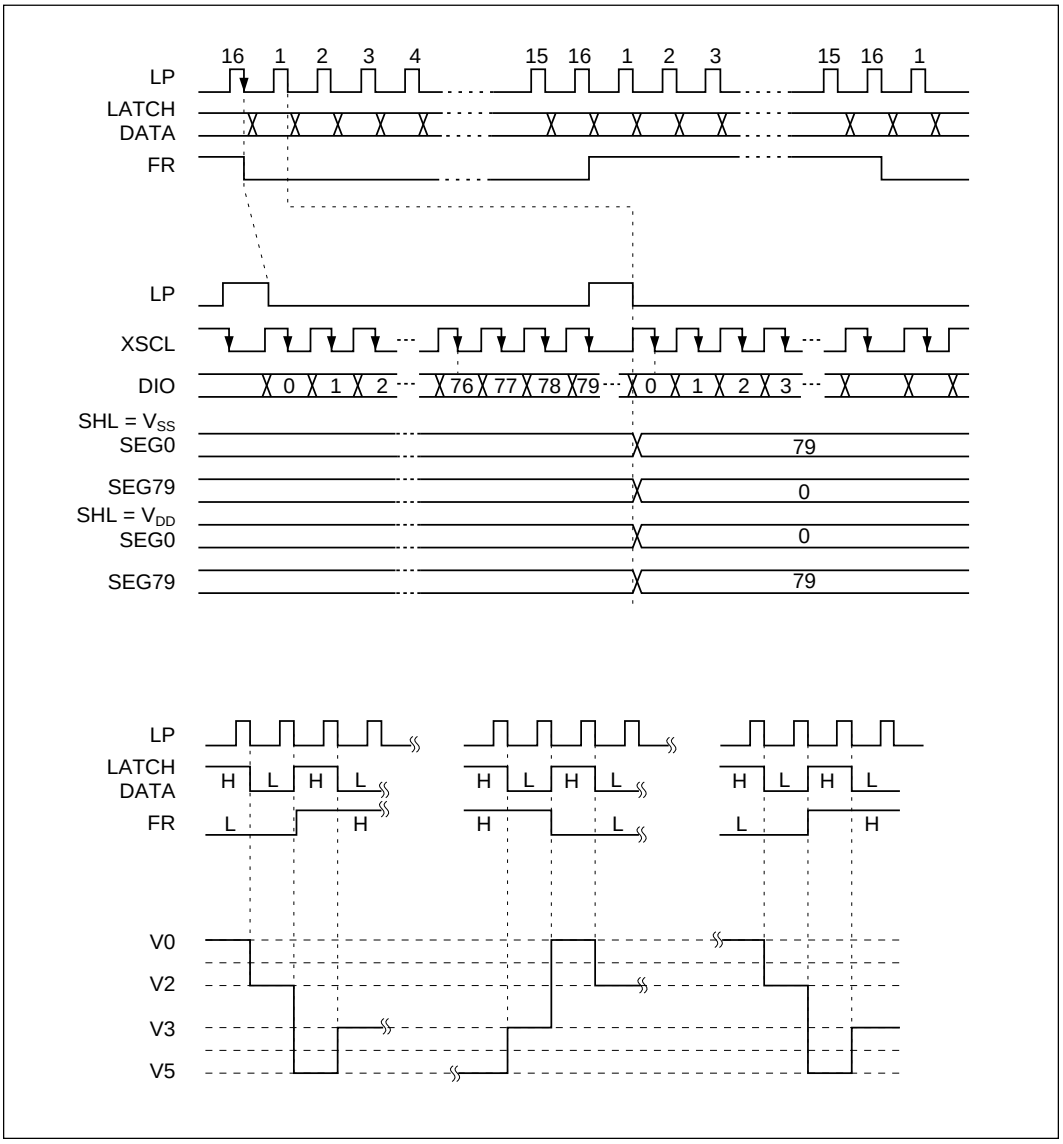
○ **Output Timing**



(V_{SS} = –6.0 V to –2.4 V, V_5 = –12.0 V to –3.0 V, T_a = –20 to 75°C)

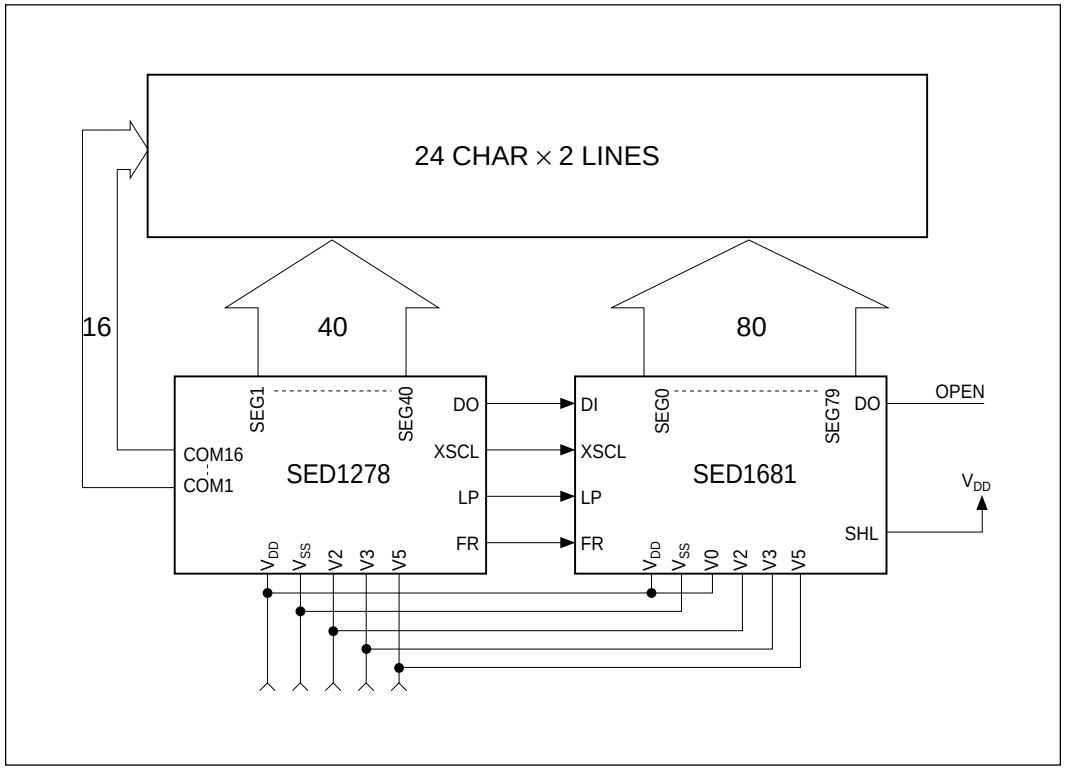
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Serial data output delay time	t_{PD}	C_L= 15 pF	—	—	250	ns
LP-SEG output delay time	t_{LPSD}	C_L= 100 pF	—	—	4.5	µs
FR-SEG output delay time	t_{FRSD}		—	—	4.5	µs

● **Timing Chart**

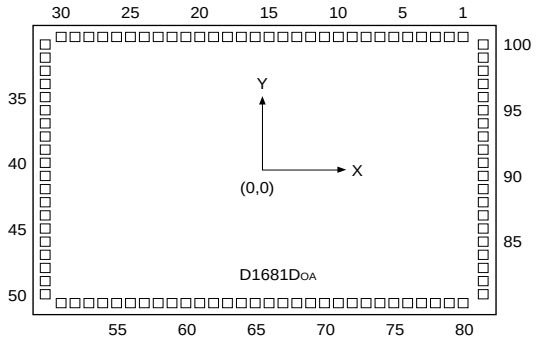


■ EXAMPLE OF APPLICATION

● SED1278



■ PAD LAYOUT



Chip Specification	Dimension (mm)
Chip size	5.59 × 3.50
Pad pitch	0.160 min.
Chip thickness	0.40 ±0.025
Pad size	0.10 × 0.10

● **PAD COORDINATES**

Unit = μm

Pad		X (μm)	Y (μm)	Pad		X (μm)	Y (μm)	Pad		X (μm)	Y (μm)
Number	Name			Number	Name			Number	Name		
1	SEG29	–2461	–1588	35	V_2	2632	–881	69	SEG61	–560	1588
2	SEG28	–2261	–1588	36	V_{SS}	2632	–721	70	SEG60	–720	1588
3	SEG27	–2069	–1588	37	LP	2632	–561	71	SEG59	–880	1588
4	SEG26	–1885	–1588	38	NC	2632	–401	72	SEG58	–1040	1588
5	SEG25	–1709	–1588	39	SHL	2632	–241	73	SEG57	–1203	1588
6	SEG24	–1538	–1588	40	XSCL	2632	–81	74	SEG56	–1366	1588
7	SEG23	–1366	–1588	41	DI	2632	79	75	SEG55	–1538	1588
8	SEG22	–1203	–1588	42	DO	2632	239	76	SEG54	–1709	1588
9	SEG21	–1040	–1588	43	NC	2632	399	77	SEG53	–1885	1588
10	SEG20	–880	–1588	44	FR	2632	559	78	SEG52	–2069	1588
11	SEG19	–720	–1588	45	NC	2632	719	79	SEG51	–2261	1588
12	SEG18	–560	–1588	46	V_{DD}	2632	879	80	SEG50	–2461	1588
13	SEG17	–400	–1588	47	NC	2632	1039	81	SEG49	–2632	1546
14	SEG16	–240	–1588	48	NC	2632	1204	82	SEG48	–2632	1372
15	SEG15	–80	–1588	49	NC	2632	1372	83	SEG47	–2632	1204
16	SEG14	80	–1588	50	NC	2632	1546	84	SEG46	–2632	1039
17	SEG13	240	–1588	51	SEG79	2461	1588	85	SEG45	–2632	879
18	SEG12	400	–1588	52	SEG78	2261	1588	86	SEG44	–2632	719
19	SEG11	560	–1588	53	SEG77	2069	1588	87	SEG43	–2632	559
20	SEG10	720	–1588	54	SEG76	1885	1588	88	SEG42	–2632	399
21	SEG9	880	–1588	55	SEG75	1709	1588	89	SEG41	–2632	239
22	SEG8	1040	–1588	56	SEG74	1538	1588	90	SEG40	–2632	79
23	SEG7	1203	–1588	57	SEG73	1366	1588	91	SEG39	–2632	–81
24	SEG6	1366	–1588	58	SEG72	1203	1588	92	SEG38	–2632	–241
25	SEG5	1538	–1588	59	SEG71	1040	1588	93	SEG37	–2632	–401
26	SEG4	1709	–1588	60	SEG70	880	1588	94	SEG36	–2632	–561
27	SEG3	1885	–1588	61	SEG69	720	1588	95	SEG35	–2632	–721
28	SEG2	2069	–1588	62	SEG68	560	1588	96	SEG34	–2632	–881
29	SEG1	2261	–1588	63	SEG67	400	1588	97	SEG33	–2632	–1041
30	SEG0	2461	–1588	64	SEG66	240	1588	98	SEG32	–2632	–1206
31	NC	2632	–1548	65	SEG65	80	1588	99	SEG31	–2632	–1374
32	V_5	2632	–1374	66	SEG64	–80	1588	100	SEG30	–2632	–1548
33	V_0	2632	–1206	67	SEG63	–240	1588				
34	V_3	2632	–1040	68	SEG62	–400	1588				

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