

SED1341

CMOS VIDEO – LCD INTERFACE (VLI)

■ DESCRIPTION

The SED1341 is a VLI (video-LCD interface) for converting previously separated video signals, intended for a CRT display, into signals compatible with dot-matrix liquid-crystal displays (LCDs). When sync and data separators are added, composite video signals can also be processed. Using the SED1341, a compact LCD monitor can replace a monochrome CRT display without including additional software or hardware.

The frame-buffer memory controlled by the VLI accurately matches the high-frequency video signals to the low-frequency operation of the LCD unit. A screen alignment function for the adjustment of the display position makes it easy to implement an LCD module that is compatible with CRT display.

Individual selection of the video data screen and LCD panel sizes and a vertical double line display mode allow the SED1341 to interface LCDs with the video outputs of a variety of personal computers (PCs).

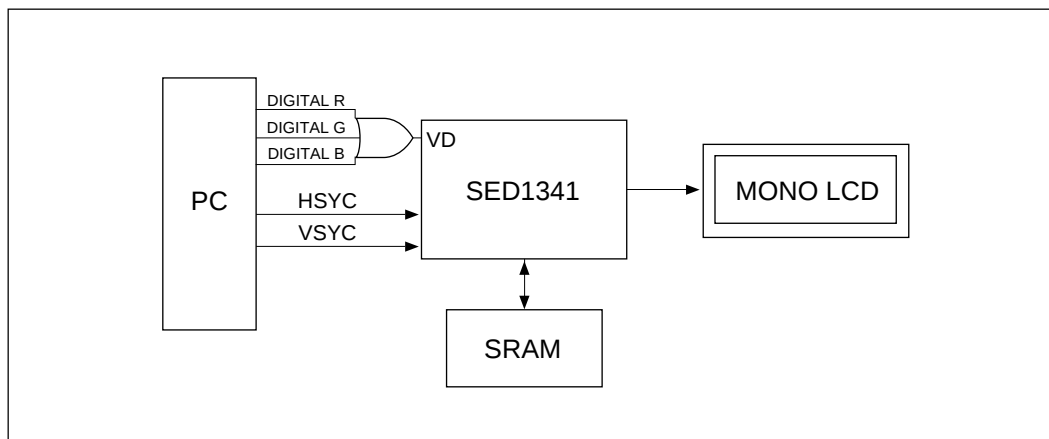
■ FEATURES

- Low-power CMOS technology
- TTL-compatible signal input
- Built-in PLL to generate dot clock
- Screen alignment adjustment via 4-bit bus or hardware
- Horizontal and vertical back porch register
- Internal oscillator to optimize the frame frequency to match the LCD timing
- Supports vertical flyback time
- Supports single panel and dual panel
- Supports 4-bit, 8-bit dual panel and 8-bit single panel
- Supports 40KB SRAM frame buffer
- Supports screen size from 640×200 to 720×400
- Duty cycle 1/100 to 1/496
- Power-on clear function
- Single power supply $5V \pm 5\%$
- Package QFP5-80 pin (FoE)

■ AVAILABLE MODELS

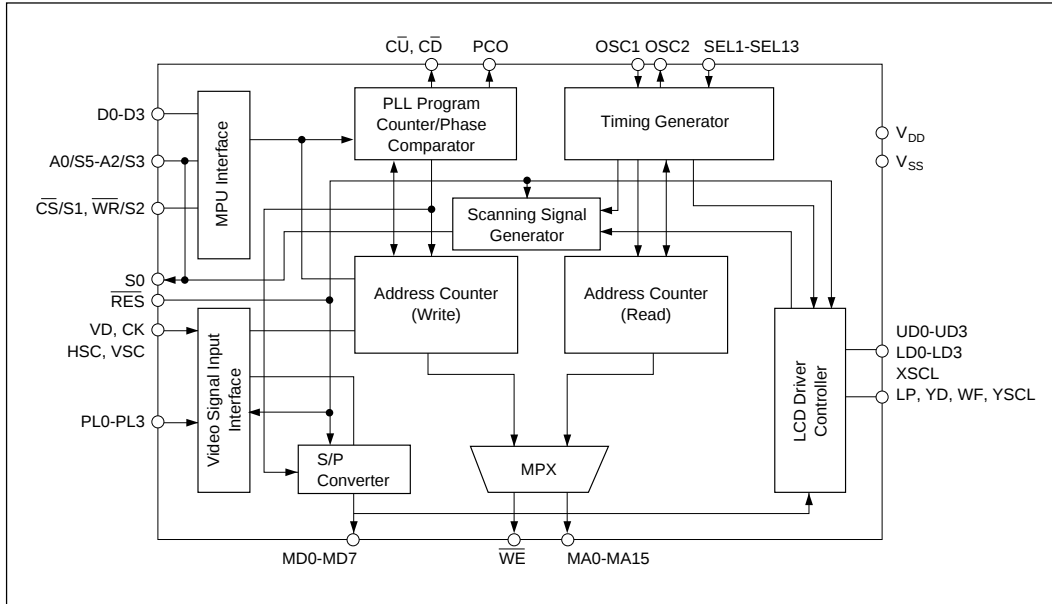
SED1341Foc and SED1341FoE. See the functional comparison table at the end of this data sheet.

■ SYSTEM BLOCK DIAGRAM

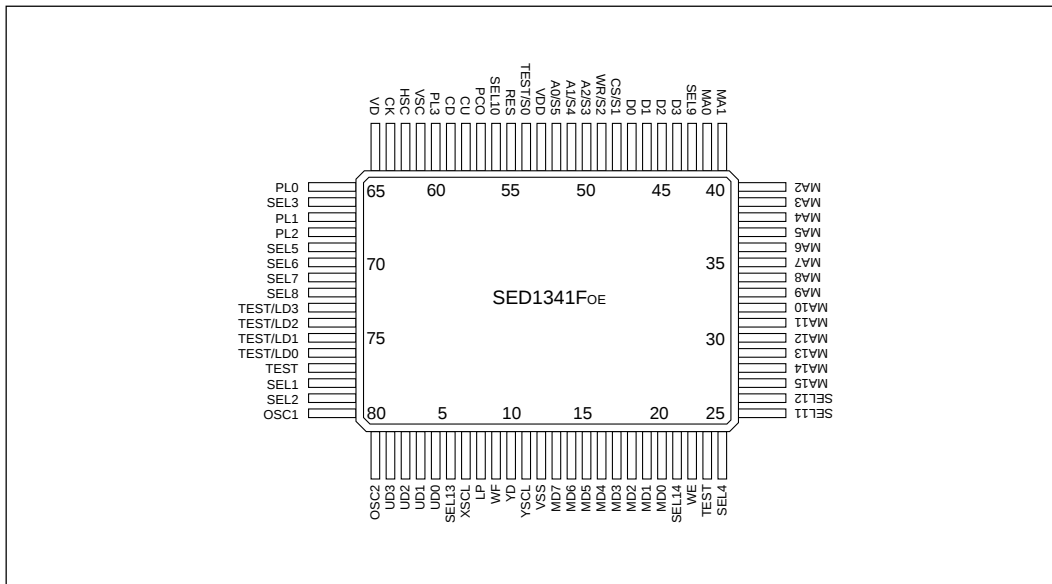


SED1341

■ BLOCK DIAGRAM



■ SED1341F0c/SED1341F0E Pin Comparison



■ PINOUT

Pin		Pin		Pin		Pin	
Number	Name	Number	Name	Number	Name	Number	Name
1	OSC2	21	SEL14	41	MA1	61	VSC
2	UD3	22	$\overline{WE}$	42	MA0	62	HSC
3	UD2	23	TEST	43	SEL9	63	CK
4	UD1	24	SEL4	44	D3	64	VD
5	UD0	25	SEL11	45	D2	65	PL0
6	SEL13	26	SEL12	46	D1	66	SEL3
7	XSCL	27	MA15	47	D0	67	PL1
8	LP	28	MA14	48	$\overline{CS}/S1$	68	PL2
9	WF	29	MA13	49	$\overline{WR}/S2$	69	SEL5
10	YD	30	MA12	50	A2/S3	70	SEL6
11	YSCL	31	MA11	51	A1/S4	71	SEL7
12	V _{SS}	32	MA10	52	A0/S5	72	SEL8
13	MD7	33	MA9	53	V _{DD}	73	TEST/LD3
14	MD6	34	MA8	54	TEST/S0	74	TEST/LD2
15	MD5	35	MA7	55	$\overline{RES}$	75	TEST/LD1
16	MD4	36	MA6	56	SEL10	76	TEST/LD0
17	MD3	37	MA5	57	PCO	77	TEST
18	MD2	38	MA4	58	$\overline{CU}$	78	SEL1
19	MD1	39	MA3	59	$\overline{CD}$	79	SEL2
20	MD0	40	MA2	60	PL3	80	OSC1

Note: TEST pins must be left open as they are wired to individual IC chips inside the package.

PIN DESCRIPTION

Pin		Description	
Name	Number		
V _{DD}	53	Supply voltage (+5V)	
V _{SS}	12	GND	
OSC1	80	Oscillator pin (input)	
OSC2	1	Oscillator pin (output)	
UD0 to UD3	5 to 2	X-driver data bus output (upper)	
TEST/LD0 to TEST/LD3	76 to 73	X-driver data bus output (lower)	
XSCL	7	X-driver shift clock output	
LP	8	Latch pulse output	
WF	9	AC waveform output for LCD	
YD	10	Row scanning start data output for Y-driver	
YSCL	11	Y-driver shift clock output	
VD	64	Video data input	
CK	63	Dot clock input	
HSC	62	Horizontal sync signal input	
VSC	61	Vertical sync signal input	
MA0 to MA15	42 to 27	Address bus output to frame buffer memory	
MD0 to MD7	20 to 13	Data bus I/O to frame buffer memory	
WE	22	Write enable signal output	
D0 to D3	47 to 44	Data input for screen position input	
		SEL5 = LOW	SEL5 = HIGH
TEST/S0	54	TEST	Scan signal output for digital switch
A0/S5 to A2/S3	52 to 50	Address bus input	Scan signal output for digital switch
CS/S1	48	Chip select input	Scan signal output for digital switch
WR/S2	49	Write signal input	Scan signal output for digital switch
RES	55	Reset signal input	
SEL1	78	LCD drive mode select input (single/dual)	
SEL2	79	LCD panel line number select input	
SEL3	66	LCD panel line number select input	
SEL4	24	LCD panel line length select input	
SEL5	69	Screen alignment method select input (SW/MPU) (disable/enable)	
SEL6	70	LCD panel vertical flyback time select input	
SEL7	71	Latch pulse output timing select input (edge/level)	
SEL8	72	X-driver interface data bus select input (4-bit, 4 × 2-bit, 8-bit)	
SEL9	43	LCD panel vertical flyback line number select input	
SEL10	56	Video data vertical line number select input	
SEL11	25	Video data vertical line number select input	
SEL12	26	Video data line length select input	
SEL13	6	Vertical doubleline display select input (enable/disable)	
SEL14	21	Horizontal back porch range select input (normal/high)	
PL0	65	Polarity select input for video signal VD	
PL1	67	Polarity select input for video signal HSC	
PL2	68	Polarity select input for video signal VSC	
PL3	60	Polarity select input for video signal CK	
PCO	57	Program counter output from PLL section	
C _U , C _D	58, 59	Phase comparator output from PLL section	

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	−0.3 to 7.0	V
Input voltage	V _I	−0.3 to V _{DD} +0.3	V
Output voltage	V _O	−0.3 to V _{DD} +0.3	V
I/O voltage	V _{I/O}	−0.3 to V _{DD} +0.3	V
Output current	I _O	−10 to 10	mA
Power dissipation	P _D	250	mW
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	−65 to 150	°C
Soldering temperature and time	T _{sol}	260°C, 10s (at lead)	—

● RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V _{DD}		4.75	5.00	5.25	V
Supply voltage	V _{SS}		—	0	—	V

● DC CHARACTERISTICS

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Oscillation Frequency	f _{osc}	f _{ck} = 14.3MHz (640×200)	f _{ck} /3.6	4.5	f _{ck} /2.28	MHz
		f _{ck} = 16MHz (640×350)	f _{ck} /3.6	7	and	MHz
		f _{ck} = 21MHz (640×400)	f _{ck} /3.6	9	11.2	MHz
		f _{ck} = 24MHz (640×480)	f _{ck} =3.6	10		MHz
Average Operating Current Consumption	I _{opr}	f _{ck} = 32MHz f _{osc} = 12MHz	—	—	40	mA
High Level Input Voltage 1	V _{IH1}	*1	2.0	—	V _{DD} +0.3	V
Low Level Input Voltage 1	V _{IL1}		−0.3	—	0.8	V
High Level Input Voltage 2	V _{IH2}	*2	4.0	—	V _{DD} +0.3	V
Low Level Input Voltage 2	V _{IL2}		−0.3	—	0.8	V
High Level Input Voltage 3	V _{IH3}	*3	3.0	—	V _{DD} +0.3	V
Low Level Input Voltage 3	V _{IL3}		−0.3	—	0.6	V
High Level Output Voltage	V _{OH}	I _{OH} = −2mA *4	4.35	—	—	V
Low Level Output Voltage	V _{OL}	I _{OL} = 6mA *4	—	—	0.4	V
Input Current Leakage	I _{L1}	V _I = 0V to V _{DD}	−1	—	1	mA
I/O Current Leakage	I _{L/I/O}	V _{I/O} = 0V to V _{DD}	−1	—	1	mA

Notes:

*1. VD, CK, HSC, VSC, MD0 to MD7, A0 to A2, CS, WR, SEL9, SEL10

*2. PL0 to PL3, SEL1 to SEL8, SEL11 to SEL13, D0 to D3

*3. RES

*4. Except OSC2 Pin

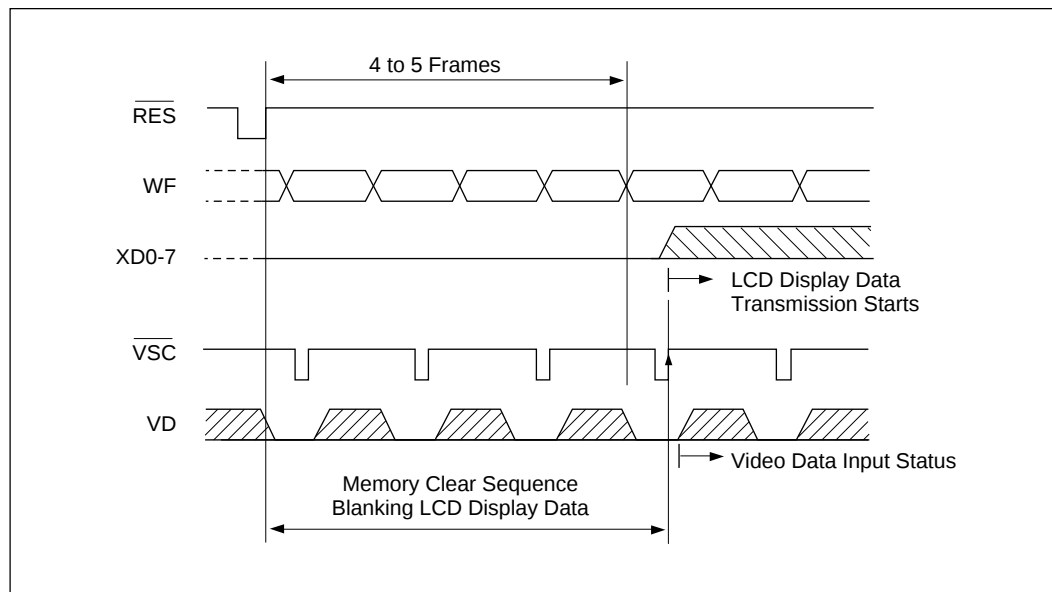
● Power-On Clear Function

VLI has an internal power-on clear function which prevents unusual display after power-on and random data display of buffer memory outside the display area.

The reset input makes the power-on clear function enable, and VLI performs as follows:

- Clearing the frame buffer memory
- Blanking the LCD display data

When the vertical sync signal, $\overline{\text{VSC}}$, is input after the four to five-frame time following the reset release, the power-on clear function is released, and ordinary display operation starts.

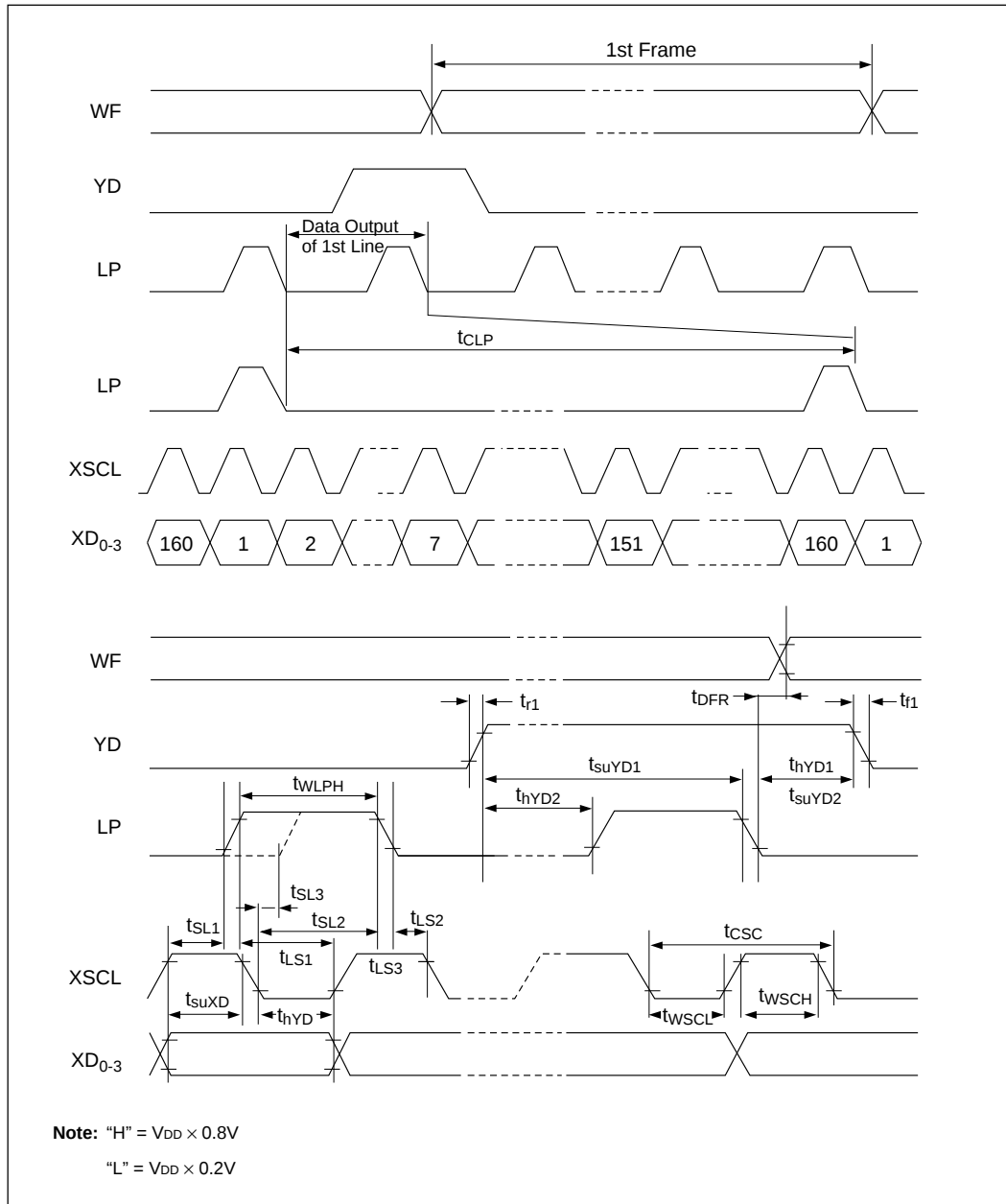


Power-on Waveforms

No video data, VD, is input during the memory clear sequence.

LCD-associated signals, such as shift clock, XSCL, and latch pulse LP are output during reset input.

- AC CHARACTERISTICS
 - LCD Interface Timing Chart



Output Signal Reference Level

○ Oscillation, Output Rise Time, Output Fall Time

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Oscillation	t ₁		2.28•tcck and 89.2	—	3.6•tcck	ns
Output Rise Time	tr ₁	C=150pF	—	—	50	ns
Output Fall Time	tf ₁	C=150pF	—	—	50	ns

Note: tcck is a cycle time of dot clock (tcck = 1/fck)

○ X Driver

(VDD = 5V±5%, VSS = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min*	Typ	Max	Unit
XSCL Cycle Time	tcsc	SEL8 = "H"	2t ₁	—	—	ns
		SEL8 = "L"	4t ₁			
XSCL "H" Pulse Width	twSCH	SEL8 = "H"	t ₁ –20	—	—	ns
		SEL8 = "L"	2t ₁ –20			
XSCL "L" Pulse Width	twSCL	SEL8 = "H"	t ₁ –20	—	—	ns
		SEL8 = "L"	2t ₁ –20			
UD0–3, UD0–3 Setup Time before XSCL	tsUXD	SEL8 = "H"	t ₁ –30	—	—	ns
		SEL8 = "L"	2t ₁ –30			
UD0–3, UD0–3 Setup Time after XSCL		SEL8 = "H"	t ₁ –30	—	—	ns
		SEL8 = "L"	2t ₁ –30			
XSCL to LP Time	tSL1	SEL7 = "H"	SEL8 = "H"	0.5t ₁ –30	—	ns
			SEL8 = "L"	t ₁ –30		
XSCL to LP Time	tSL2		SEL8 = "H"	t ₁ –20		
			SEL8 = "L"	2t ₁ –20		
LP to XSCL Time	tLS1		SEL8 = "H"	1.5t ₁ –50		
			SEL8 = "L"	3t ₁ –50		
LP to XSCL Time	tLS2		SEL8 = "H"	t ₁ –20		
			SEL8 = "L"	2t ₁ –20		
XSCL to LP Time	tSL3	SEL7 = "L"	SEL8 = "H"	0.5t ₁ –40	—	ns
			SEL8 = "L"	t ₁ –40		
LP to XSCL Time	tLS3		SEL8 = "H"	0.5t ₁ –40		
			SEL8 = "L"	t ₁ –40		
LP Cycle Time	tCLP	SEL1 = "H"		320t ₁	—	ns
		SEL1 = "L"		640t ₁		
LP "H" Pulse Width	twLPW	SEL7 = "H"	SEL8 = "H"	1.5t ₁ –50	—	ns
			SEL8 = "L"	3t ₁ –50		
		SEL7 = "L"	SEL8 = "H"	t ₁ –40		
			SEL8 = "L"	2t ₁ –40		
WF Output Delay Time After LP1, LP2	tdFR	—		—	100	ns

*t₁ is an oscillation frequency of X'tal oscillation circuit (t₁ = 1/fosc)

○ **Y Driver**

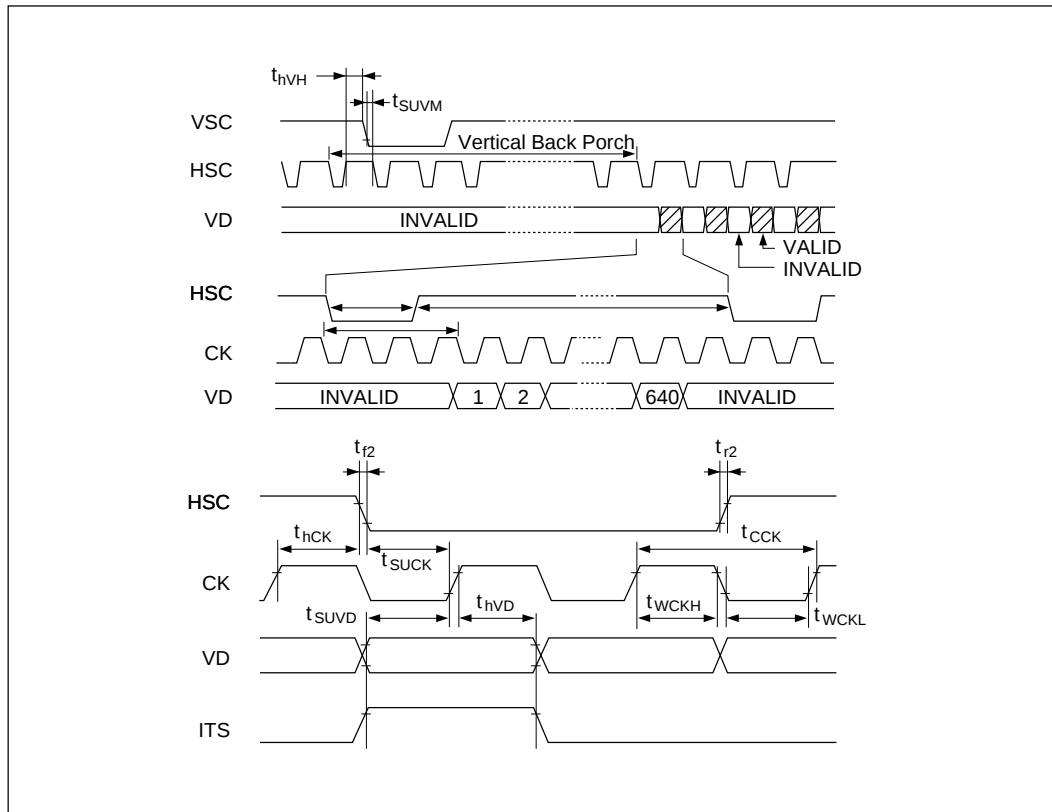
($V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0$ to 70°C)

Parameter	Symbol	Condition		Min*	Typ	Max	Unit				
YD Setup Time before LP, YSCL	tsUYD1	SEL7 = "H"	SEL1 = "H"	142t1-100	—	—	ns				
			SEL1 = "L"	302t1-100							
YD Hold Time after LP, YSCL	thYD1		SEL1 = "H"	18t1-100	—	—	ns				
			SEL1 = "L"	18t1-10							
YD Setup Time before LP, YSCL	tsUYD2	SEL7 = "L"	SEL1 = "H"	SEL8 = "H"	141.5t1-100	—	—	ns			
				SEL8 = "L"	141t1-100						
			SEL1 = "L"	SEL8 = "H"	301.5t1-100				—	—	ns
				SEL8 = "L"	301t1-100						
YD Hold Time after LP, YSCL	thYD2		SEL1 = "H"	SEL8 = "H"	17.5t1-100	—	—	ns			
				SEL8 = "L"	17t1-100						
			SEL1 = "L"	SEL8 = "H"	17.5t1-100				—	—	ns
				SEL8 = "L"	17t1-100						

*t1 is an oscillation frequency of X'tal oscillation circuit ($t1 = 1/f_{osc}$)

○ **Video Signal Interface**

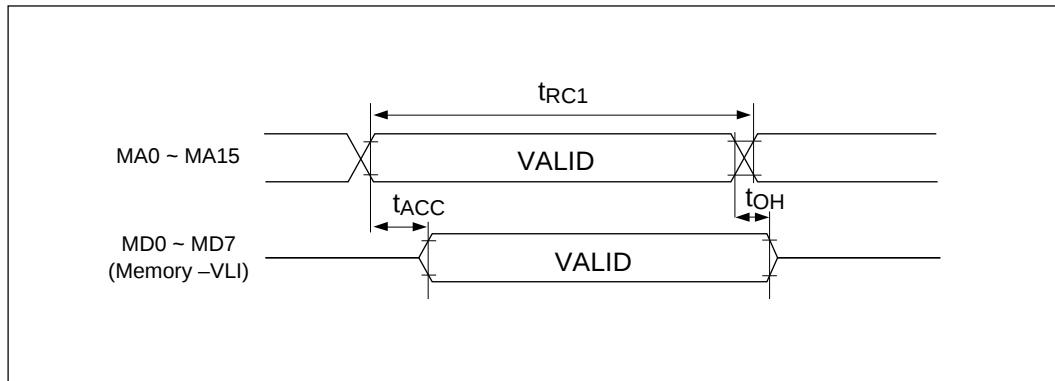
(When PL1 = "L", PL2 = "L", PL3 = "L")



(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

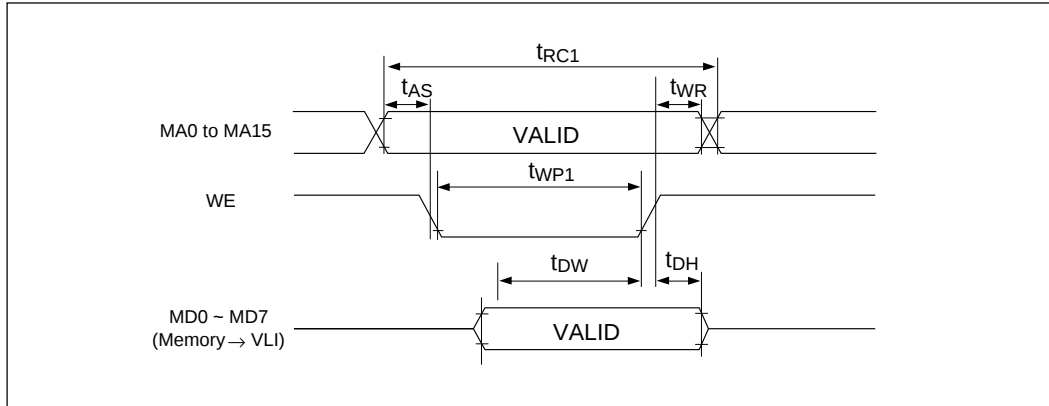
Parameter	Symbol	Condition	Min	Typ	Max	Unit
CK Cycle Timer	t _{CCK}		29.4	—	—	ns
CK "H" Pulse Width	t _{wCKw}		12	—	—	ns
CK "L" Pulse Width	t _{wCKL}		12	—	—	ns
Input Rise Time	t _{r2}		—	—	5	ns
Input Fall Time	t _{f2}		—	—	5	ns
VD Setup Time Before CK	t _{SUVD}		16	—	—	ns
VD Hold Time After CK	t _{HVD}		2	—	—	ns
CK Setup Time Before HSC	t _{SUCK}		20	—	—	ns
CK Hold Time After HSC	t _{HCK}		0	—	—	ns
HSC Setup Time Before VSC	t _{SUVW}		80	—	—	ns
HSC Hold Time After VSC	t _{HUM}		0	—	—	ns

- **Memory Interface**
 - **Read Cycle**

(V_{DD} = 5V±5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Read Cycle Time	t _{RC1}		4t _{CCK}	—	—	ns
Address Access Time	t _{ACC}		—	—	4t _{CCK} -17	ns
Output Hold Time	t _{OH}		10	—	—	ns

◦ Write Cycle



($V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0$ to 70°C)

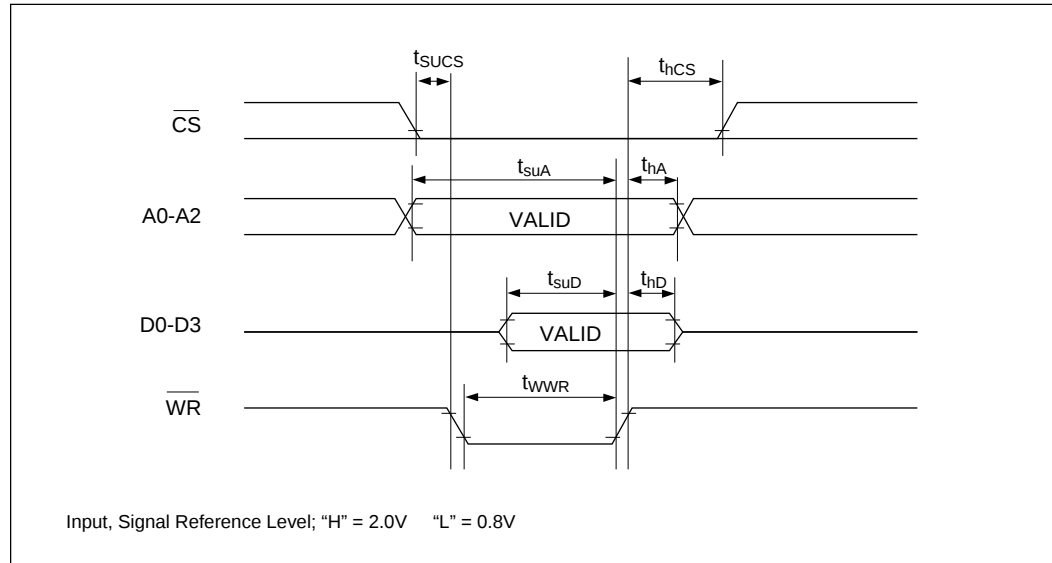
Parameter	Symbol	Condition	Min*	Typ	Max	Unit
Write Cycle Time	t_{WC1}		$4t_{CCK}$	—	—	ns
Write Pulse Width	t_{WD1}		$3t_{CCK} - 13$	—	—	ns
Address Setup Time	t_{AS}		$0.5t_{CCK} - 14$	—	—	ns
Address Hold Time	t_{WR}		$0.5t_{CCK} - 14$	—	—	ns
Data Setup Time	t_{DW}		$3t_{CCK} - 38$	—	—	ns
Data Hold Time	t_{DH}		5	—	—	ns

Input, Output Signal Reference Level; "H" = 2.0V "L" = 0.8V

* t_{CCK} is a cycle time of Dot Clock ($t_{CCK} = 1/f_{CK}$).

SED1341

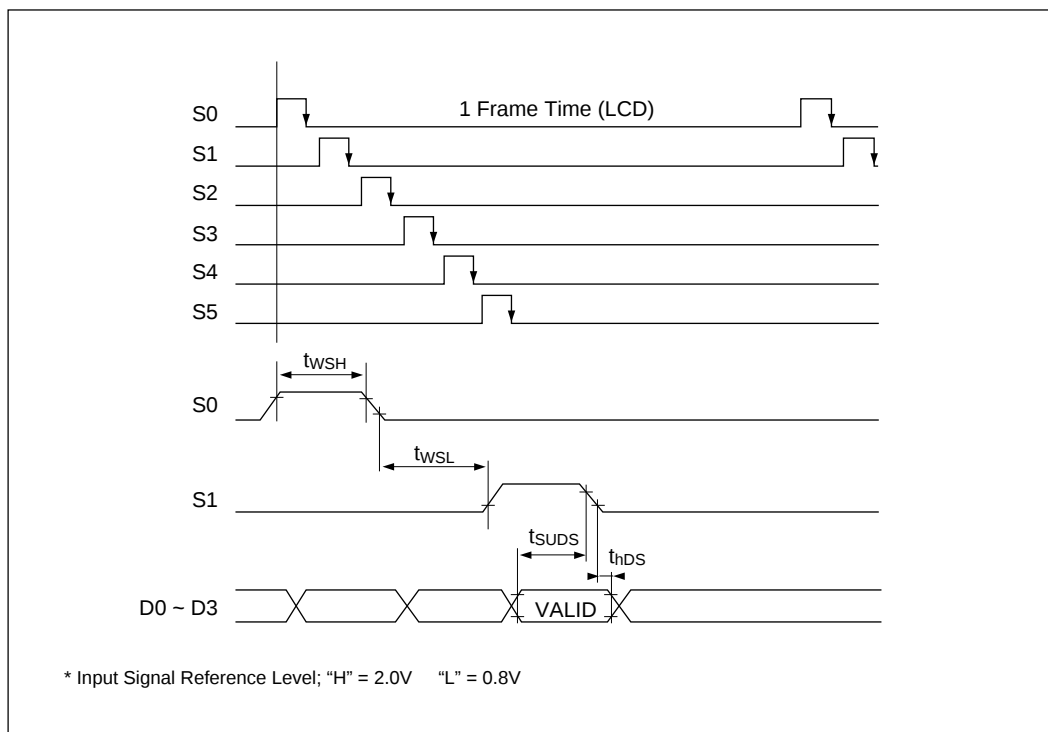
- Register Program
 - Write Method of MPU



($V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0$ to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CS Setup Time	t_{sUCS}		10	—	—	ns
CS Hold Time	t_{hCS}		10	—	—	ns
A0–A2 Setup Time	t_{sUA}		10	—	—	ns
A0–A2 Hold Time	t_{hA}		10	—	—	ns
D0–D3 Setup Time	t_{sUD}		50	—	—	ns
D0–D3 Hold Time	t_{hD}		10	—	—	ns
Pulse Width	t_{WWR}		50	—	—	ns

● Data Set Method By Digital Switch

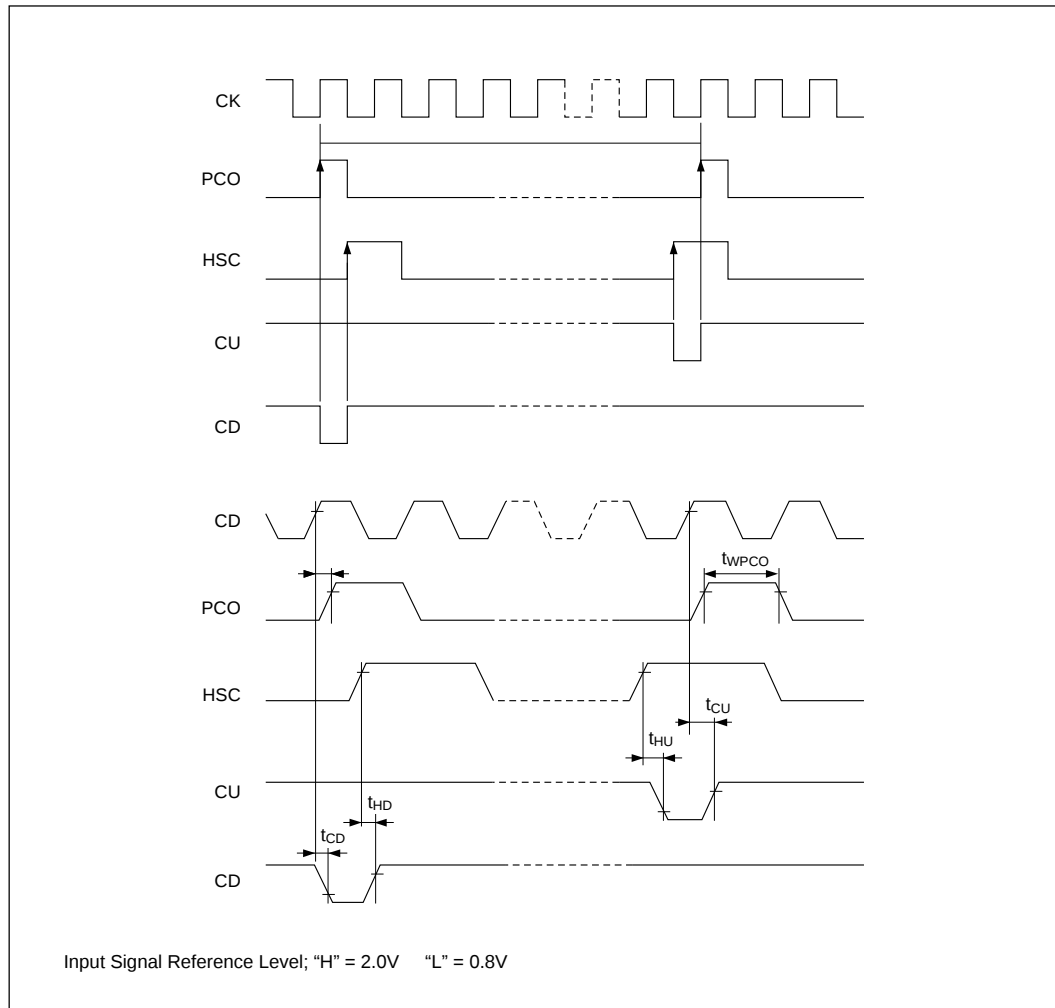


($V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0$ to 70°C)

Parameter	Symbol	Condition	Min*	Typ	Max	Unit
Scanning Signal "H" Pulse Width	t_{WSH}		$8t_1-150$	—	—	ns
Scanning Signal "OFF" Width	t_{WSL}		$8t_1-150$	—	—	ns
D0-D3 Setup Time	t_{sUDS}		100	—	—	ns
D0-D3 Hold Time	t_{hDS}		0	—	—	ns

* t_1 is an oscillation frequency of X'tal oscillation circuit ($t_1 = 1/f_{osc}$)

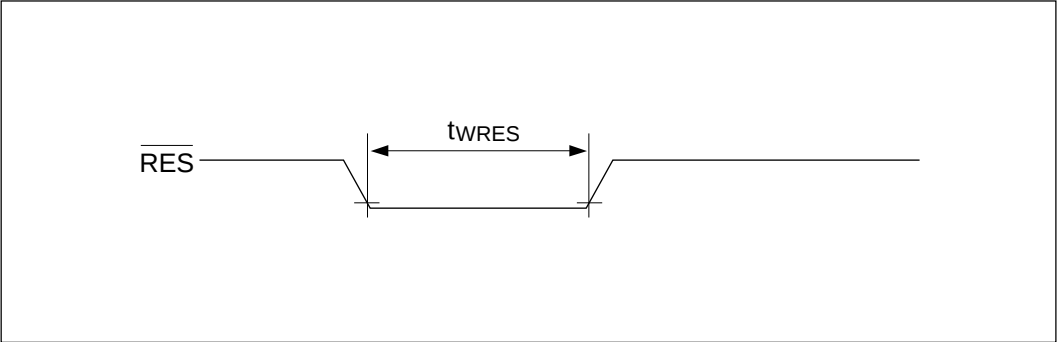
● PLL Interface



($V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0$ to 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{CU}}$ "ON" Delay Time After HSC	t_{HU}	$CL = 20\text{pF}$	—	22	40	ns
$\overline{\text{CU}}$ "OFF" Delay Time After CK	t_{CU}	$CL = 20\text{pF}$	—	22	40	ns
$\overline{\text{CU}}$ "ON" Delay Time After CK	t_{CD}	$CL = 20\text{pF}$	—	22	40	ns
CD "OFF" Delay Time After HSC	t_{HD}	$CL = 20\text{pF}$	—	22	40	ns
PCO Delay Time After CK	t_{CPCD}	$CL = 20\text{pF}$	—	—	35	ns
PCO Pulse Width	t_{WPCO}	$CL = 20\text{pF}$	$t_{CCK} - 25$	—	—	ns

● Reset Input

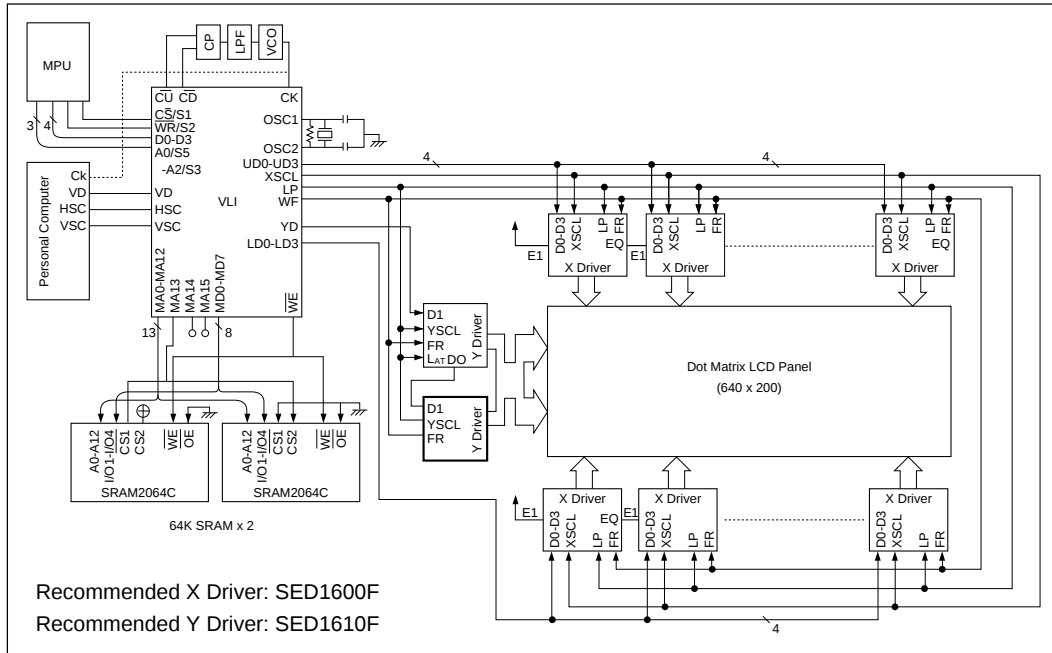


($V_{\text{DD}} = 5\text{V} \pm 5\%$, $V_{\text{SS}} = 0\text{V}$, $T_{\text{a}} = 0 \text{ to } 70^{\circ}\text{C}$)

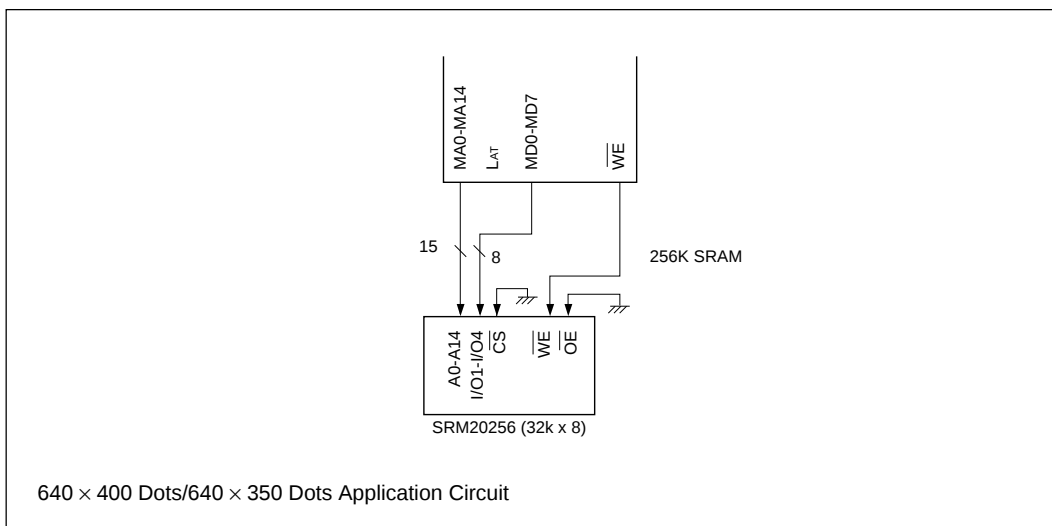
Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{RES}}$ Pulse Width	t_{WRES}		1.0	—	—	ns

Input Signal Reference Level; "H" = 2.0V "L" = 0.8V

■ EXAMPLE OF APPLICATION: 640 × 200 Dots, 4 bit 2-Bus, 2-Screen Operation



● 640 × 400 Dots/640 × 350 Dots Connecting to Memory



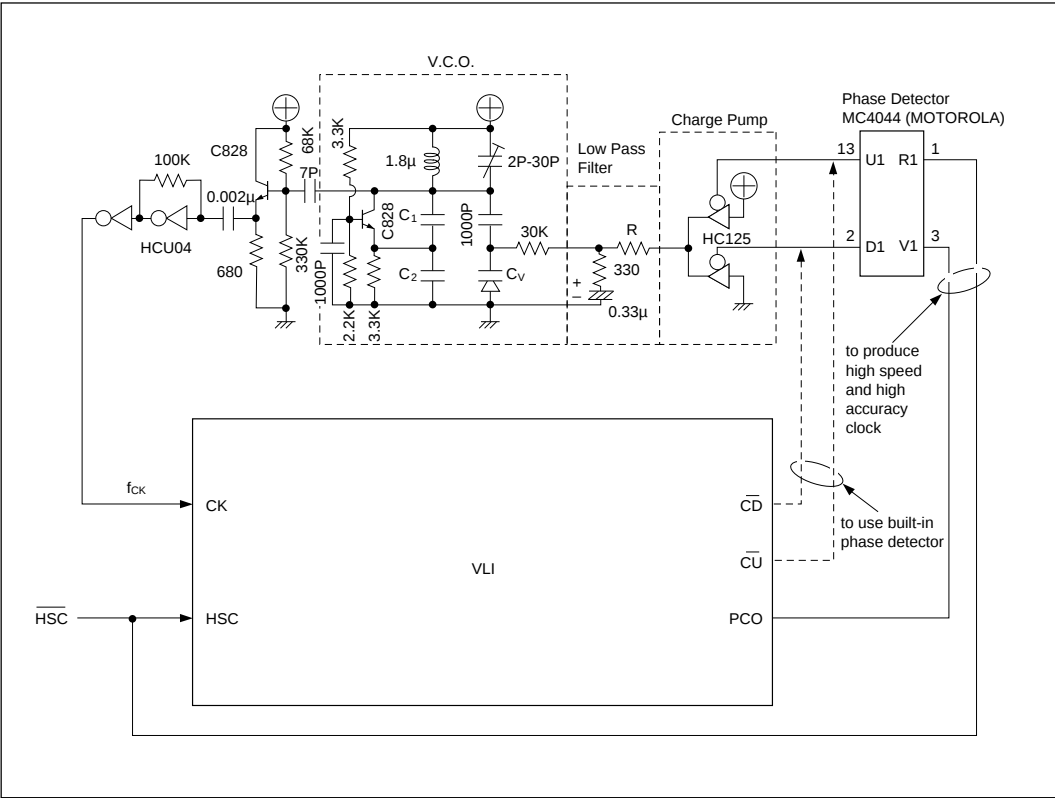
- **640 × 480 Dots Connecting to Memory**



- **Example of LCD Module**



● Example of PLL Circuit



f _{ck}	C _u	C ₁	C ₂	R
14.3 MHz	1SV73(JRC)	22pF	30pF	330 Ω
21 MHz	1S2267 (Toshiba)	10pF	15pF	510 Ω

■ DIFFERENCES BETWEEN SED1341F0C and SED1341F0E

No.	Name		No.	Name	
	D1341F0C	D1341F0E		D1341F0C	D1341F0E
1	OSC2	OSC2	41	MA1	MA1
2	UD3	UD3	42	MA0	MA0
3	UD2	UD2	43	NU/SEL9	SEL9
4	UD1	UD1	44	D3	D3
5	UD0	UD0	45	D2	D2
6	XECL	SEL13	46	D1	D1
7	XSCL	XSCL	47	D0	D0
8	LP1	LP	48	$\overline{\text{CS}}/\text{S1}$	$\overline{\text{CS}}/\text{S1}$
9	WF	WF	49	$\overline{\text{WR}}/\text{S2}$	$\overline{\text{WR}}/\text{S2}$
10	YD	YD	50	A2/S3	A2/S3
11	NU/LP2	YSCL	51	A1/S4	A1/S4
12	VSS	VSS	52	A0/S5	A0/S5
13	MD7	MD7	53	VDD	VDD
14	MD6	MD6	54	NU/S0	NU/S0
15	MD5	MD5	55	$\overline{\text{RES}}$	$\overline{\text{RES}}$
16	MD4	MD4	56	NU/ITS	SEL10
17	MD3	MD3	57	PCO	PCO
18	MD2	MD2	58	$\overline{\text{CU}}$	$\overline{\text{CU}}$
19	MD1	MD1	59	$\overline{\text{CD}}$	$\overline{\text{CD}}$
20	MD0	MD0	60	PL3	PL3
21	CAS	NU	61	VSC	VSC
22	WE	WE	62	HSC	HSC
23	NU	NU	63	CK	CK
24	SEL4	SEL4	64	VD	VD
25	RAS2	SEL11	65	PL0	PL0
26	RAS1	SEL12	66	SEL3	SEL3
27	MA14/MA15	MA15	67	PL1	PL1
28	MA14	MA14	68	PL2	PL2
29	MA13	MA13	69	SEL5	SEL5
30	MA12	MA12	70	NU/SEL6	SEL6
31	MA11	MA11	71	NU/SEL7	SEL7
32	MA10	MA10	72	NU/SEL8	SEL8
33	MA9	MA9	73	NU/LD3	NU/LD3
34	MA8	MA8	74	NU/LD2	NU/LD2
35	MA7	MA7	75	NU/LD1	NU/LD1
36	MA6	MA6	76	NU/LD0	NU/LD0
37	MD5	MD5	77	$\overline{\text{SEL}}$	NU
38	MA4	MA4	78	SEL1	SEL1
39	MA3	MA3	79	SEL2	SEL2
40	MA2	MA2	80	OSC1	OSC1

NU = Not Used. NU terminals must be open since they are wired to individual IC chips in the package.

SED1341

● Functional Comparison Table

Item	SED1341Foc	SED1341FoE
640 × 200	O	O
640 × 350	O	O
640 × 400	O	O
640 × 480	O	O
720 × 350	X	O
720 × 400	X	O
Automatic Centering Display	X	O
Automatic Horizontal Line Blanking	X	O
PLL Counter Dividing Ratio	1/706 to 1/961	1/514 to 1/1025
Frame Buffer Memory	SRAM/DRAM	SRAM
ITS (Half Tone) Display	O	X
XECL (X-Driver Enable Clock) (output)	O	X

O: Possible

X: Not Possible