S1D13504 COLOR GRAPHICS LCD/CRT CONTROLLER

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■ DESCRIPTION

The S1D13504 is a low cost, low power, color/monochrome LCD/CRT controller interfacing to a wide range of CPUs and LCDs. The S1D13504 architecture is designed to meet the requirements of embedded markets such as Office Automation equipment, Mobile Communications devices and Hand-Held PCs where Windows® CE may serve as a primary operating system.

The S1D13504 supports LCD interfaces with data widths up to 16-bits. Using Frame Rate Modulation (FRM), it can display 16 shades of gray on monochrome LCD panels, up to 4096 colors on passive color LCD, and 64K colors on active matrix TFT LCD panels. CRT support is handled through the use of an external RAMDAC interface allowing simultaneous display of both the CRT and LCD panel. A 16-bit memory interface supports up to 2M bytes of FPM-DRAM or EDO-DRAM. Supports flexible operating voltages from 2.7V to 5.5V.

■ FEATURES

Memory Interface

- 16-bit EDO-DRAM or FPM-DRAM interface.
- Memory size options:
  512K bytes using one 256K×16 device.
  2M bytes using one 1M×16 device.
- Addressable as a single linear address space.

CPU Interface

- Supports the following interfaces:
  Hitachi SH-3.
  Motorola M68K.
  ISA bus.
  MPU bus interface with programmable READY.
  i386/486 bus.
  Philips MIPS PR31500/31700.
  NEC MIPS VR4102.
- CPU write buffer.

Display Support

- 4/8-bit monochrome passive LCD interface.
- 4/8/16-bit color passive LCD interface.
- Single-panel, single-drive displays.
- Dual-panel, dual-drive displays.
- Direct support for 9/12-bit TFT; 18-bit TFT is supported up to 64K color depth (16-bit data).
- External RAMDAC support using the upper byte of the LCD data bus for the RAMDAC pixel data bus.
- Simultaneous display of CRT and 4/8-bit passive or 9-bit TFT panels, regardless of resolution.
- Maximum resolution of 800x600 pixels at a color depth of 16 bpp.

Display Modes

- 1/2/4/8/16 bit-per-pixel (bpp) support on LCD.
- 1/2/4/8 bit-per-pixel (bpp) on CRT.
- Up to 16 shades of gray using FRM on monochrome passive LCD panels.
- Up to 4096 colors on passive LCD panels.
- Up to 64K colors on active matrix TFT LCD in 16 bpp modes.
- Split Screen Display: allows two different images to be simultaneously displayed.
- Virtual Display Support: displays images larger than the panel size through the use of panning.
- Double Buffering/multi-pages: provides smooth animation and instantaneous screen update.
- Acceleration of screen updates by allocating full display buffer bandwidth to CPU.

Clock Source

- Single clock input for both pixel and memory clocks.
- Memory clock can be input clock or (input clock/2), providing flexibility to use CPU bus clock as input.
- Pixel clock can be memory clock or (memory clock/2), (memory clock/3) or (memory clock/4).

Power Down Modes

- Two power down modes: one software / one hardware.
- LCD Power Sequencing.

General Purpose IO pins

- Up to 12 General Purpose IO pins are available.

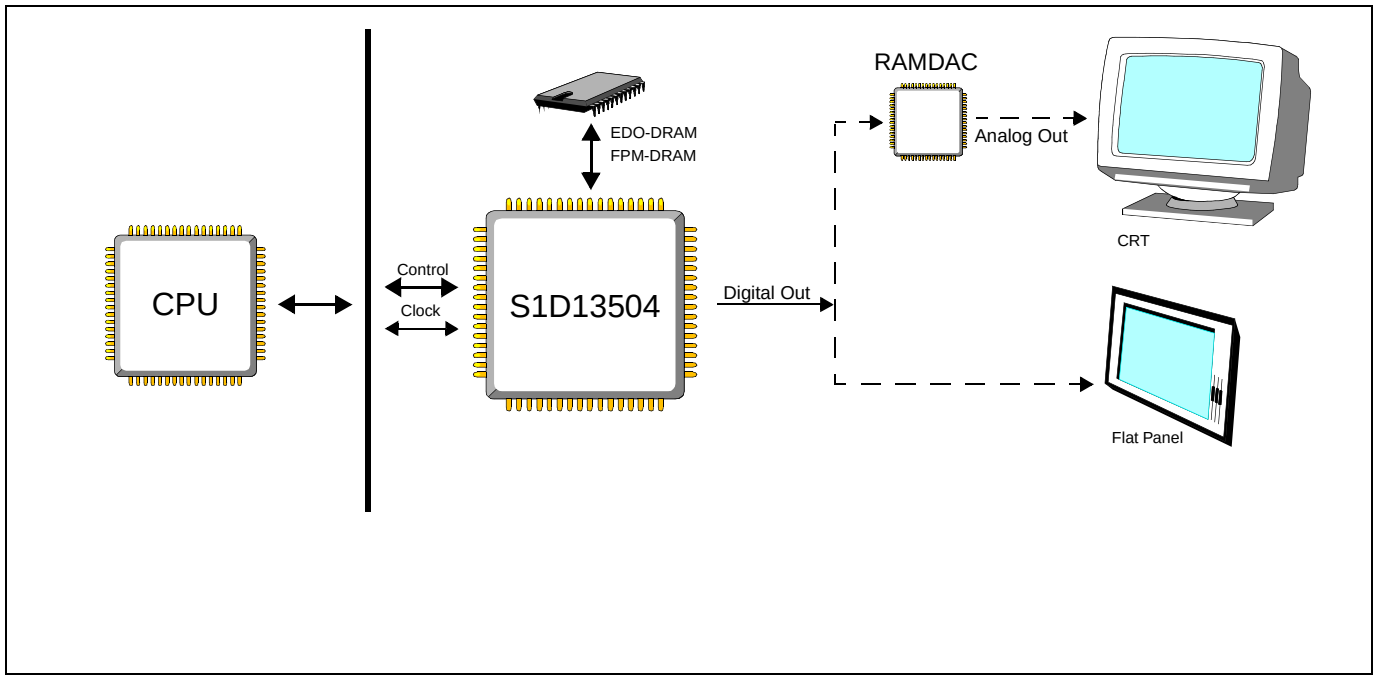
Operating Voltage

- 2.7 volts to 5.5 volts.

Package

- 128-pin QFP15 surface mount package
- 144-pin QFP20 surface mount package

SYSTEM BLOCK DIAGRAM



CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS:

- S1D13504 Technical Manual
- S5U13504 Evaluation Boards
- Windows® CE Display Driver
- CPU Independent Software Utilities

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