S1R72902

IEEE1394 AV/C-Compliant Integrated One-Chip Controller

■ DESCRIPTION

The S1R72902F00A is a digital AV system controller that contains an IEEE1394 interface and a stream interface conforming to the IEEE 1394-1995 and 1394a-2000 standards.
This single-chip IC integrates a 2-port cable PHY, a LINK/Transaction controller ideal for IEC61883 Isochronous packets, Seiko Epson's original 32-bit RISC processor, and a Flash memory for storing firmware.
For IEC61883 Isochronous packet transfer, this IC can add and remove CIP and source packet headers automatically. The stream interface can connect to separate 8-bit DMA interfaces for inputs and outputs.
Part of transactions is hardware-implemented. Setting PageTable addresses and sizes in the SBP-2 protocol automates subsequent PageTable fetch and data transfer.
The S1R72902F00A provides an optimal IEEE1394 interface to AV appliances from computer peripherals to digital home electronics.

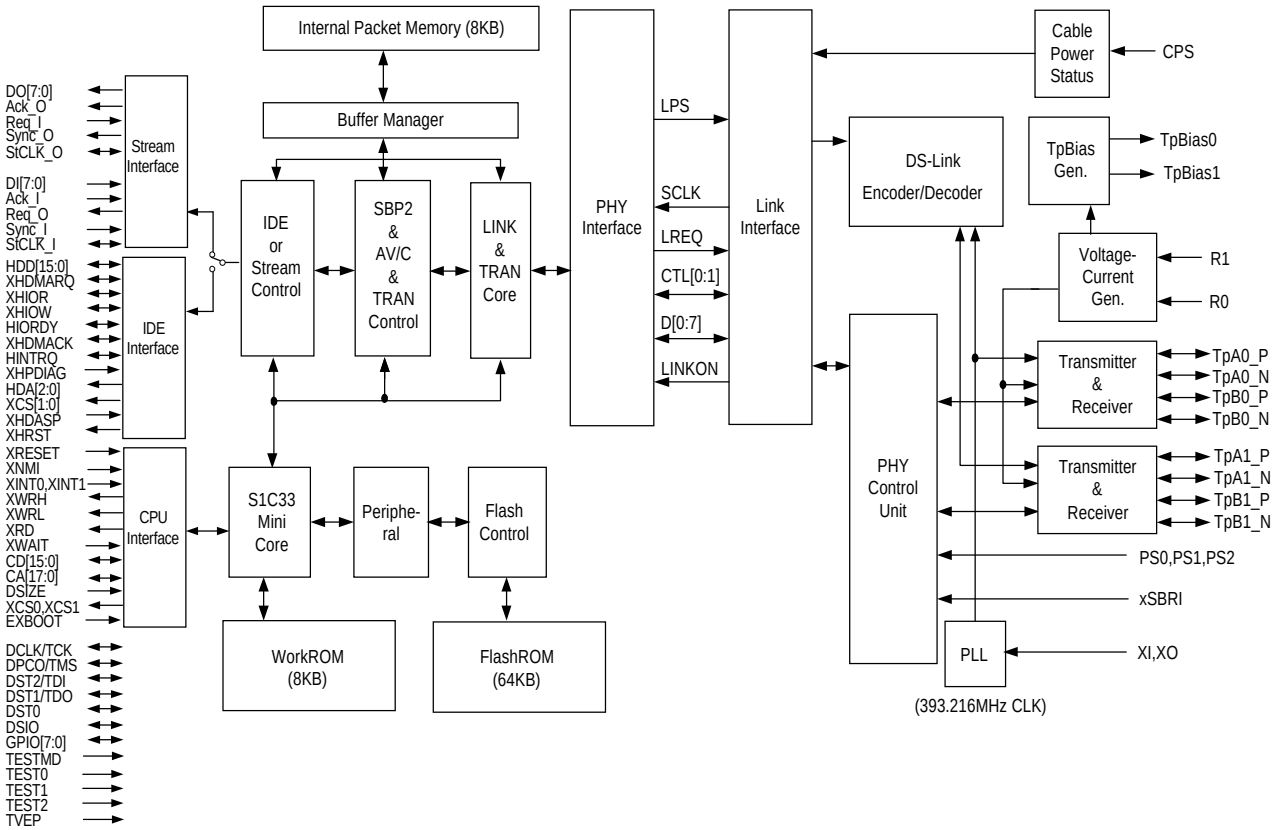
■ FEATURES

- Cable PHY Transceiver/Arbitor
  Contains a two-port small-amplitude differential transceiver that excels in precision and speed.
  The on-chip 400MHz PLL enables transmission and reception at S400, S200 and S100 speeds and 50MHz SCLK output.
  The Cable Power Status function detects a cable power drop.
- Link/Transaction Controller
  Supports bi-directional data transfer in both Asynchronous and Isochronous modes.
  The built-in SRAM implements stable bi-directional data transfer at a MaxPayload of up to 100/200/400Mbps.
  Simplifies communications with upper layers by separating header and data areas.
  The packet buffer area is divided into header, stream, and ORB areas.
  Each of the receive header area, receive data areas (receive stream and receive ORB areas), and transmit data area (transmit stream area) has a ring buffer. These areas can be configured to any size.
  Busy conditions during reception are automatically controlled by the hardware.
  The receive header area is divided into Isochronous and Asynchronous areas. This enables Asynchronous command packet transfer during Isochronous packet transmission.
  In Asynchronous data reception, the command packets and data packets can be identified according to the transaction label, and stored separately in the receive Stream area and the receive ORB area.
- IEC61883-compliant Isochronous packet transfer
  Automatically transmits up to eight packets with CIP and source packet headers.
  Automatically separates the received Isochronous packets into headers (Isochronous packet header, CIP header, and source packet header) and AV data, and stores them separately in the receive header and receive stream areas.
  Receives the packets in a specific format by identifying the FMT code in the CIP header.
- SBP-2 Support
  Once PageTable addresses and sizes in the SBP-2 protocol are set, subsequent PageTable fetch and data transfer are done automatically.
- Stream interface (supporting IDE interfaces)
  The stream interface can connect to separate 8-bit DMA interfaces for inputs and outputs, but they cannot be used simultaneously for bi-directional data transfer.
  Capable of outputting Sync (synchronous byte signals) for IEC61883-compliant Isochronous packets.
  The IDE interface can be switched to the stream interface supporting PIO 0-4, Multi-ward DMA 0-2, and Ultra DMA 0-4 modes.
  A 5V tolerant cell is used to operate the IC as a 3.3V single power supply.
- C33 RISC CPU
  Equipped with Seiko Epson's original RISC CPU, this IC does not require an extra CPU.

- External CPU interface
  This IC has 18 address lines, 16 data lines, a read strobe, and a write H/L strobe for an external C33 RISC CPU.
- Flash ROM
  This IC contains a 64kbyte Flash ROM. There's no need for additional Flash ROMs.
- ICD33 Interface
  This IC reserves six pins as an interface with ICD33 that facilitates the development of firmware for the internal CPU.
  These pins can also function as JTAG pins, allowing the user to rewrite the built-in Flash ROM easily.
- Supply voltage
  3.3V±0.15V
- 176-pin flat package (24 × 24 × 1.4mm, 0.5mm pin pitch)
  Pb-free package

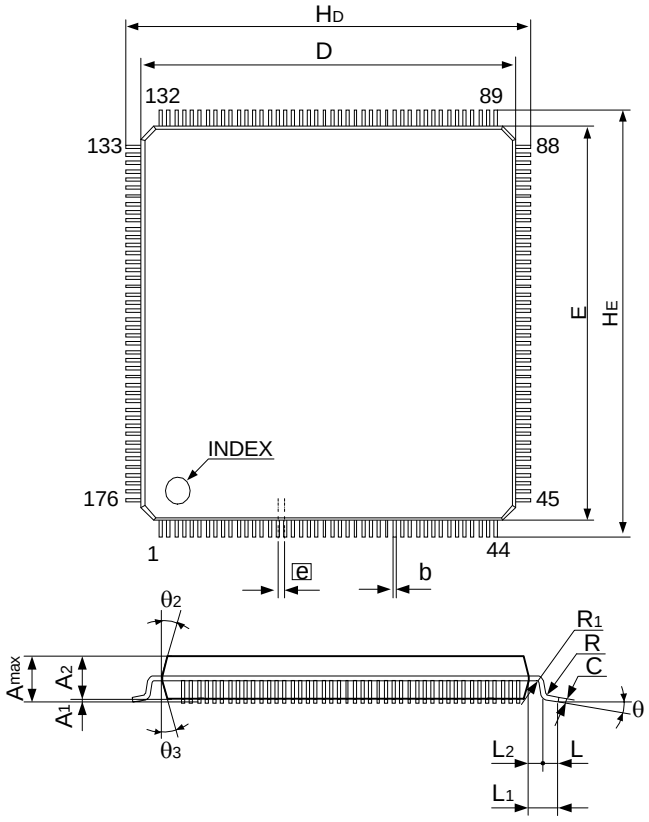
※ Radiation shield is not included.

■ BLOCK DIAGRAM



■ PACKAGE DIMENSIONS

Plastic QFP 176pin Body size 24 × 24 × 1.4mm (QFP21)



Lead type STD (QFP21-176pin STD)						
Symbol	Dimension in Millimeters			Dimension in inches*		
	Min.	Nom.	Max.	Min.	Nom.	Max.
E	23.9	24	24.1	(0.941)	(0.945)	(0.948)
D	23.9	24	24.1	(0.941)	(0.945)	(0.948)
A			1.7			(0.066)
A_1		0.1			(0.004)	
A_2	1.3	1.4	1.5	(0.052)	(0.055)	(0.059)
e		0.5			(0.020)	
b	0.15	0.2	0.3	(0.006)	(0.008)	(0.011)
C	0.1	0.125	0.175	(0.004)	(0.005)	(0.006)
θ	0°		10°	(0°)		(10°)
L	0.3	0.5	0.7	(0.012)	(0.020)	(0.027)
L_1		1			(0.039)	
L_2		0.5			(0.020)	
H_E	25.6	26	26.4	(1.008)	(1.024)	(1.039)
H_D	25.6	26	26.4	(1.008)	(1.024)	(1.039)
θ_2		15°			(15°)	
θ_3		15°			(15°)	
R		0.2			(0.008)	
R_1		0.2			(0.008)	

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