EPSON

S1R72901

Single chip LSI for high-speed interface IEEE1394a-2000

■ DESCRIPTIONS

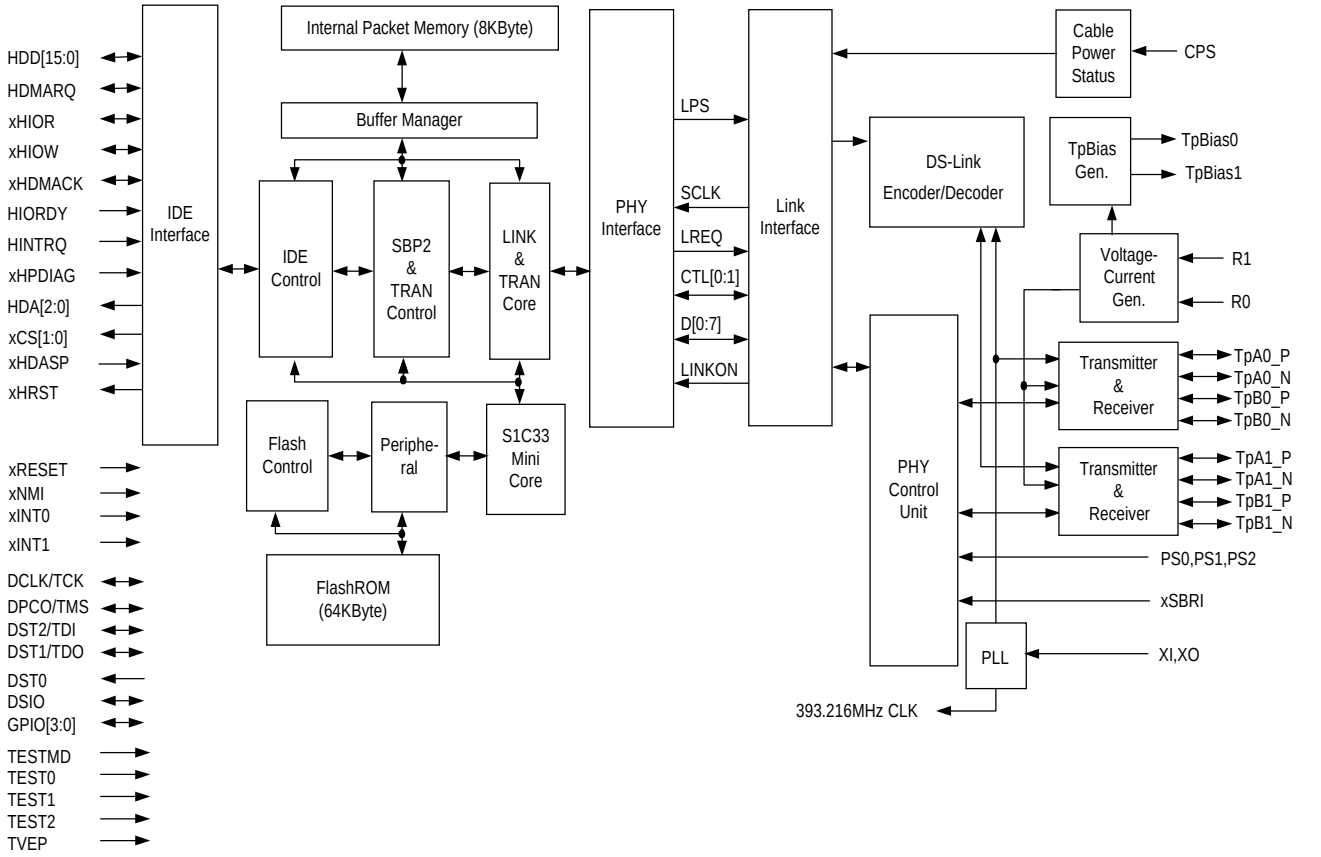
The S1R72901 is the single chip controller that bridges the IEEE1394 interface conforming to 1394-1995 and 1394a-2000 of the IEEE standard, with the IDE interface conforming to the ATA5.
The following components are integrated into single chip; two-port cable PHY, the LINK/Transaction controller most suitable to the SBP-2 protocol, Seiko Epson original 32-bit RISC processor and the Flash memory for Firmware storage.
Hardware includes a part of transaction functions that allows automatic PageTable fetch and the data transfer once the PageTable address and size for the SBP-2 protocol are set.
The S1R72901 provides the IEEE1394 interface to the computer peripheral devices, especially to the storage devices that are most suitable.

■ FEATURES

- Cable PHY Transceiver/Arbitor
  - Built-in 2 port high-precision small amplitude differential high-speed transceiver.
  - Built-in on-chip 400MHz PLL that realizes the S400/S200/S100 transmission and reception, and the 50MHz SCLK output.
  - Cable Power Status function that detects the cable power drop.
- Link/Transaction Controller
  - Realizes duplex data transfer including Asynchronous and Isochronous transfer.
  - Realizes stable duplex data transfer up to the Maxpayload at 100Mbps, 200Mbps and 400Mbps with the built-in SRAM.
- SBP-2 Support
  - A part of transactions is realized by hardware (a dedicated area is secured) to prevent actual transfer rate drop due to the overhead.
  - The header area and the data area are separated to simplify the communication with the upper layers. The data area is divided into the stream area and the ORB area.
  - The ring buffer is applied to the receiving header area, the receiving data area (receiving stream area, receiving ORB area) and sending data area (sending stream area).
  - Sizes of the respective areas can be set as desired, independently.
  - The busy status is automatically controlled by hardware when receiving a signal.
  - Once the PageTable address and size in the SBP-2 are set, the PageTable fetch and the data transfer can be done automatically.
- IDE interface
  - Compatible with PIO mode 0/1/2/3/4, multiword DMA mode 0/1/2 and Ultra-DMA mode 0/1/2/3/4/5
  - 3.3V single power source is applicable with the 5V tolerant cell.
- C33 RISC CPU
  - 32-bit RISC CPU EIAC332×501 operating at 25MHz (CPU cycle minimum 2τ operation)
  - Built-in SRAM: 8KB, no wait operation
  - Built-in Flash ROM: 64KB, no wait operation
  - Programmable timer: built-in 3-channel timers
- Flash ROM
  - Built-in 64KB Flash ROM, no need of external Flash ROM
- ICD33 interface
  - Incorporates the ICD33 interface that facilitates development of Firmware to operate the CPU. The ICD33 can be connected with as few as six pins.
  - This terminal can be used as a JTAG terminal to rewrite the data in the built-in Flash ROM easily.
- Power voltage
  - 3.3V±0.3V
- 100-pin flat package (pin pitch is 0.5 mm).

✧ Radiation-proof design is not done.

■ BLOCK DIAGRAM



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