EPSON

S1C63455

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Original Architecture Core CPU
- Low Current Consumption
- Wide-range Operating Voltage (1.8V to 6.4V)
- High Speed Operation in Low Voltage

■ DESCRIPTION

The S1C63455 is a microcomputer which has a high-performance 4-bit CPU S1C63000 as the core CPU, ROM (4,096 words × 13 bits), RAM (1,024 words × 4 bits), serial interface, watchdog timer, programmable timer, time base counters (2 systems), a dot-matrix LCD driver that can drive a maximum 60 segments × 8 commons and sound generator built-in. The S1C63455 features high speed operation and low current consumption in a wide operating voltage range (1.8 V to 6.4 V), this makes it suitable for applications working with batteries. It is also suitable for portable products.

■ FEATURES

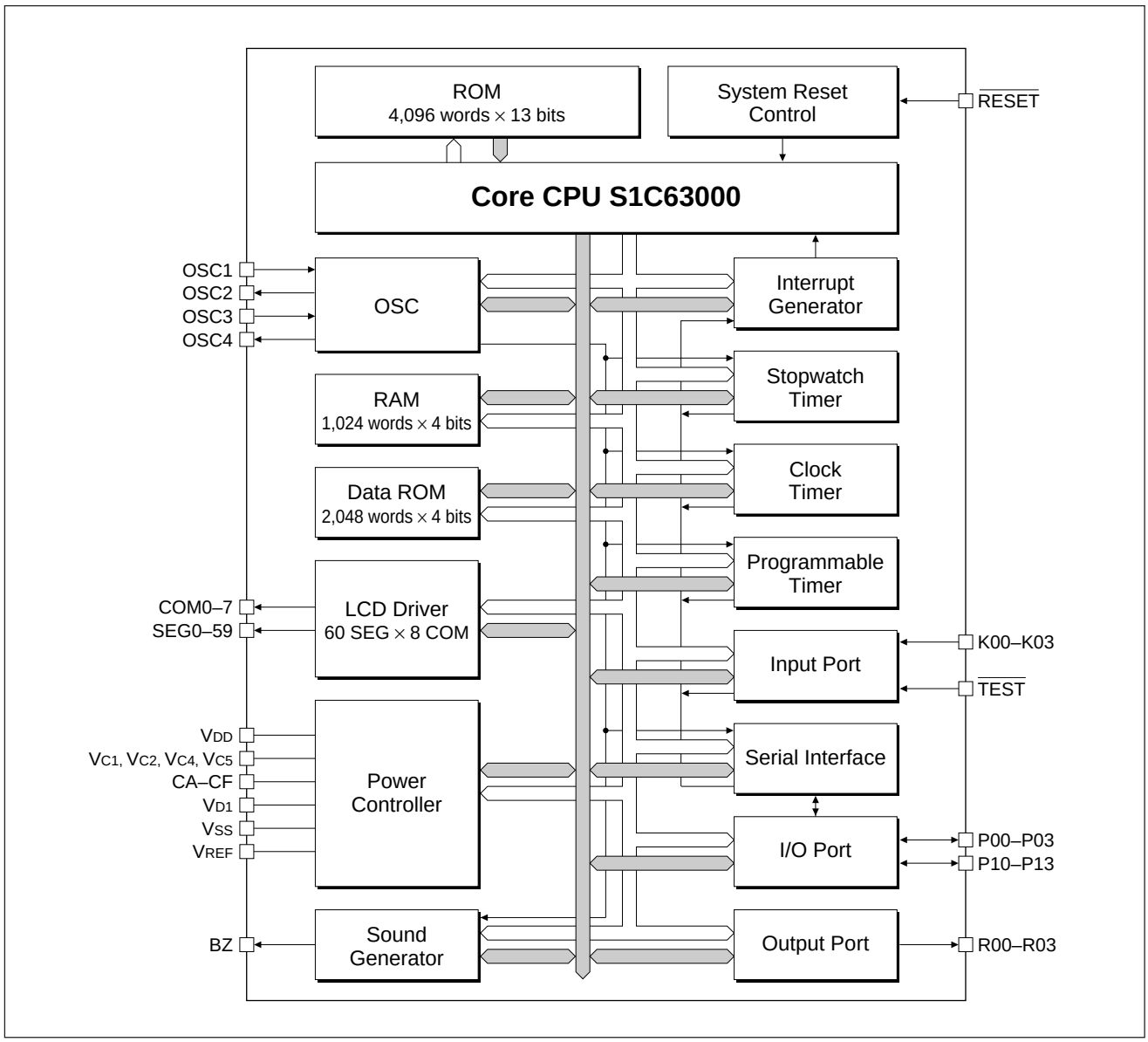
- OSC1 oscillation circuit ..... 32.768 kHz (Typ.) crystal or 60 kHz (Typ.) CR oscillation circuit (∗1)
- OSC3 oscillation circuit ..... 1.8 MHz (Typ.) CR or 4 MHz (Max.) ceramic oscillation circuit (∗1)
- Instruction set ..... Basic instruction: 46 types (411 instructions with all)
  Addressing mode: 8 types
- Instruction execution time ..... During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec
  During operation at 60 kHz: 33 µsec 67 µsec 100 µsec
  During operation at 4 MHz: 0.5 µsec 1 µsec 1.5 µsec
- ROM capacity ..... Code ROM: 4,096 words × 13 bits
  Data ROM: 2,048 words × 4 bits (= 8K bits)
- RAM capacity ..... Data memory: 1,024 words × 4 bits
  Display memory: 480 bits (120 words × 4 bits)
- Input port ..... 4 bits (Pull-up resistors may be supplemented ∗1)
- Output port ..... 4 bits (It is possible to switch the 2 bits to special output ∗2)
- I/O port ..... 8 bits (It is possible to switch the 4 bits to serial I/F input/output ∗2)
- Serial interface ..... 1 port (8-bit clock synchronous system)
- LCD driver ..... 60 segments × 8 commons
- Time base counter ..... 2 systems (Clock timer, stopwatch timer)
- Programmable timer ..... Built-in, 2 inputs × 8 bits
- Watchdog timer ..... Built-in
- Sound generator ..... With envelope and 1-shot output functions
- External interrupt ..... Input port interrupt: 1 system
- Internal interrupt ..... Clock timer interrupt: 4 systems
  Stopwatch timer interrupt: 2 systems
  Programmable timer interrupt: 2 systems
  Serial interface interrupt: 1 system
- Power supply voltage ..... 1.8 V–6.4 V: OSC1 Crystal oscillator, OSC3 Not use
  2.2 V–6.4 V: OSC1 Crystal oscillator, OSC3 CR or ceramic oscillator
  OSC1 CR oscillator, OSC3 ceramic oscillator
  2.0 V–6.4 V: OSC1 CR oscillator, OSC3 CR oscillator
  OSC1 CR oscillator, OSC3 Not use
- Operating temperature range ..... -20°C to 70°C

● Current consumption (Typ.) ..... Single clock (OSC1: Crystal oscillation):
During HALT (32 kHz)
3.0 V (LCD power OFF) 1 µA
3.0 V (LCD power ON, V_{C1} standard) 6 µA
3.0 V (LCD power ON, V_{C2} standard) 4 µA
During operation (32 kHz)
3.0 V (LCD power ON, V_{C1} standard) 10 µA
Twin clock:
During operation (4 MHz)
3.0 V (LCD power ON, V_{C1} standard) 1,000 µA

● Package ..... QFP5-128pin (plastic), QFP8-128pin (plastic) or chip

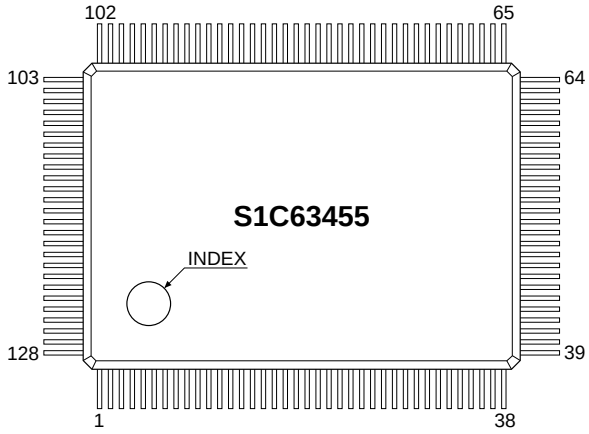
∗1: Can be selected with mask option ∗2: Can be selected with software

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

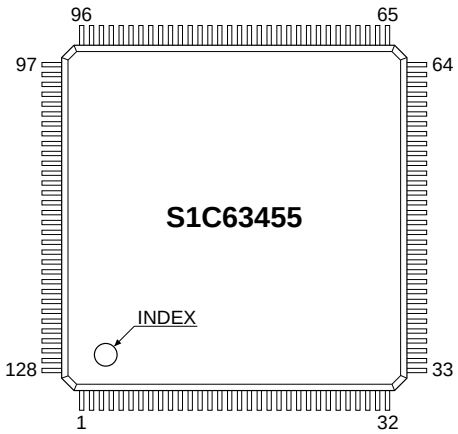
QFP5-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG12	33	N.C.	65	N.C.	97	SEG41
2	SEG11	34	N.C.	66	N.C.	98	N.C.
3	N.C.	35	N.C.	67	N.C.	99	N.C.
4	N.C.	36	N.C.	68	N.C.	100	N.C.
5	N.C.	37	N.C.	69	V_{C1}	101	SEG40
6	N.C.	38	N.C.	70	V_{C2}	102	SEG39
7	N.C.	39	N.C.	71	V_{C4}	103	SEG38
8	SEG10	40	N.C.	72	V_{C5}	104	SEG37
9	SEG9	41	OSC3	73	CF	105	SEG36
10	SEG8	42	OSC4	74	CE	106	SEG35
11	SEG7	43	V_{DD}	75	CD	107	SEG34
12	SEG6	44	$\overline{RESET}$	76	CC	108	SEG33
13	SEG5	45	$\overline{TEST}$	77	CB	109	SEG32
14	SEG4	46	V_{REF}	78	CA	110	SEG31
15	SEG3	47	R03	79	SEG59	111	SEG30
16	SEG2	48	R02	80	SEG58	112	SEG29
17	SEG1	49	R01	81	SEG57	113	SEG28
18	SEG0	50	R00	82	SEG56	114	SEG27
19	COM7	51	P13	83	SEG55	115	SEG26
20	COM6	52	P12	84	SEG54	116	SEG25
21	COM5	53	P11	85	SEG53	117	SEG24
22	COM4	54	P10	86	SEG52	118	SEG23
23	COM3	55	P03	87	SEG51	119	SEG22
24	COM2	56	P02	88	SEG50	120	SEG21
25	COM1	57	P01	89	SEG49	121	SEG20
26	COM0	58	P00	90	SEG48	122	SEG19
27	BZ	59	K03	91	SEG47	123	SEG18
28	V_{SS}	60	K02	92	SEG46	124	SEG17
29	OSC1	61	K01	93	SEG45	125	SEG16
30	OSC2	62	K00	94	SEG44	126	SEG15
31	V_{D1}	63	N.C.	95	SEG43	127	SEG14
32	N.C.	64	N.C.	96	SEG42	128	SEG13

N.C. : No Connection

QFP8-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	33	N.C.	65	N.C.	97	N.C.
2	N.C.	34	N.C.	66	V_{C1}	98	SEG40
3	N.C.	35	N.C.	67	V_{C2}	99	SEG39
4	N.C.	36	N.C.	68	V_{C4}	100	SEG38
5	SEG10	37	N.C.	69	V_{C5}	101	SEG37
6	SEG9	38	OSC3	70	CF	102	SEG36
7	SEG8	39	OSC4	71	CE	103	SEG35
8	SEG7	40	V_{DD}	72	CD	104	SEG34
9	SEG6	41	$\overline{RESET}$	73	CC	105	SEG33
10	SEG5	42	$\overline{TEST}$	74	CB	106	SEG32
11	SEG4	43	V_{REF}	75	CA	107	SEG31
12	SEG3	44	R03	76	SEG59	108	SEG30
13	SEG2	45	R02	77	SEG58	109	SEG29
14	SEG1	46	R01	78	SEG57	110	SEG28
15	SEG0	47	R00	79	SEG56	111	SEG27
16	COM7	48	P13	80	SEG55	112	SEG26
17	COM6	49	P12	81	SEG54	113	SEG25
18	COM5	50	P11	82	SEG53	114	SEG24
19	COM4	51	P10	83	SEG52	115	SEG23
20	COM3	52	P03	84	SEG51	116	SEG22
21	COM2	53	P02	85	SEG50	117	SEG21
22	COM1	54	P01	86	SEG49	118	SEG20
23	COM0	55	P00	87	SEG48	119	SEG19
24	BZ	56	K03	88	SEG47	120	SEG18
25	V_{SS}	57	K02	89	SEG46	121	SEG17
26	OSC1	58	K01	90	SEG45	122	SEG16
27	OSC2	59	K00	91	SEG44	123	SEG15
28	V_{D1}	60	N.C.	92	SEG43	124	SEG14
29	N.C.	61	N.C.	93	SEG42	125	SEG13
30	N.C.	62	N.C.	94	SEG41	126	SEG12
31	N.C.	63	N.C.	95	N.C.	127	SEG11
32	N.C.	64	N.C.	96	N.C.	128	N.C.

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP5-128pin	QFP8-128pin		
V_{DD}	43	40	–	Power (+) supply pin
V_{SS}	28	25	–	Power (–) supply pin
V_{D1}	31	28	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}, V_{C2}, V_{C4}, V_{C5}	69, 70, 71, 72	66, 67, 68, 69	–	LCD system power supply pin 1/4 bias generated internally
V_{REF}	46	43	O	LCD system power supply testing pin
CA–CF	78–73	75–70	–	LCD system boosting/reducing capacitor connecting pin
OSC1	29	26	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	30	27	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	41	38	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	42	39	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	62–59	59–56	I	Input port
P00–P03	58–55	55–52	I/O	I/O port
P10–P13	54–51	51–48	I/O	I/O port (switching to serial I/F input/output is possible by software)
R00	50	47	O	Output port
R01	49	46	O	Output port
R02	48	45	O	Output port (switching to TOUT signal output is possible by software)
R03	47	44	O	Output port (switching to FOUT signal output is possible by software)
COM0–COM7	26–19	23–16	O	LCD common output pin
SEG0–SEG59	18–8, 2–1, 128–101, 97–79	15–5, 127–98, 94–76	O	LCD segment output pin
$\overline{BZ}$	27	24	O	Sound output pin
$\overline{RESET}$	44	41	I	Initial reset input pin
$\overline{TEST}$	45	42	I	Testing input pin

■ OPTION LIST

1 OSC1 SYSTEM CLOCK
- ☐ 1. Crystal (32.768 kHz)
- ☐ 2. CR (60 kHz)

2 OSC3 SYSTEM CLOCK
- ☐ 1. Use <Ceramic (4 MHz)>
- ☐ 2. Use <CR (1.8 MHz)>

3 MULTIPLE KEY ENTRY RESET COMBINATION
- ☐ 1. Not Use
- ☐ 2. Use <K00, K01, K02, K03>
- ☐ 3. Use <K00, K01, K02>
- ☐ 4. Use <K00, K01>

4 MULTIPLE KEY ENTRY RESET TIME AUTHORIZE
- ☐ 1. Not Use
- ☐ 2. Use

5 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct

6 OUTPUT PORT OUTPUT SPECIFICATION

• R00	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R01	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R02	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• R03	☐ 1. Complementary	☐ 2. Nch-OpenDrain

7 I/O PORT OUTPUT SPECIFICATION

• P0x	☐ 1. Complementary	☐ 2. Nch-OpenDrain
• P1x	☐ 1. Complementary	☐ 2. Nch-OpenDrain

8 I/O PORT PULL UP RESISTOR

• P0x	☐ 1. With Resistor	☐ 2. Gate Direct
• P1x	☐ 1. With Resistor	☐ 2. Gate Direct

9 I/O PORT INPUT SPECIFICATION

☐ 1. Normal CMOS Input
☐ 2. Schmitt Trigger Input

10 SERIAL PORT INTERFACE POLARITY

☐ 1. Positive
☐ 2. Negative

11 SOUND GENERATOR POLARITY FOR OUTPUT

☐ 1. Positive
☐ 2. Negative

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).
∗2: In case of plastic package.

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V, OSC3 oscillation OFF	OSC1 Crystal oscillation	1.8	3.0	6.4	V
			OSC1 CR oscillation	2.0	3.0	6.4	V
		V_{SS}=0V, OSC3 oscillation ON	OSC3 Ceramic oscillation	2.2	3.0	6.4	V
			OSC3 CR oscillation	2.0	3.0	6.4	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		–	32.768	–	kHz
		CR oscillation		40	60	80	kHz
	f_{OSC3}	CR oscillation			1,800		kHz
		Ceramic oscillation				4,100	kHz

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03,P00–03, P10–13	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$, P10–13	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03,P00–03, P10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$, P10–13	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	-12	-7	-5	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, P00–03, P10–13			-2	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-2	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, P00–03, P10–13	3			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	3			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–7			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03,P00–03, P10–13	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$, P10–13	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03,P00–03, P10–13	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$, P10–13	0		0.1·V_{DD}	V
High level input current	I_{IH}	V_{IH}=5.0V	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, P00–03, P10–13 $\overline{RESET}$, $\overline{TEST}$	-20	-12	-9	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, P00–03, P10–13			-5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, P00–03, P10–13	7.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	7.5			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–7			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, R_{CR1}=600kΩ, R_{CR2}=47kΩ, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load)	LC0–3="0"	Typ. ×0.88	0.975	Typ. ×1.12	V
			LC0–3="1"		0.990		
			LC0–3="2"		1.005		
			LC0–3="3"		1.020		
			LC0–3="4"		1.035		
			LC0–3="5"		1.050		
			LC0–3="6"		1.065		
			LC0–3="7"		1.080		
			LC0–3="8"		1.095		
			LC0–3="9"		1.110		
			LC0–3="10"		1.125		
			LC0–3="11"		1.140		
			LC0–3="12"		1.155		
			LC0–3="13"		1.170		
			LC0–3="14"		1.185		
			LC0–3="15"		1.200		
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load)		$2 \cdot V_{C1}$ ×0.9		$2 \cdot V_{C1}$	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (without panel load)		$3 \cdot V_{C1}$ ×0.9		$3 \cdot V_{C1}$	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (without panel load)		$4 \cdot V_{C1}$ ×0.9		$4 \cdot V_{C1}$	V
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (without panel load)		$1/2 \cdot V_{C2}$ ×0.95		$1/2 \cdot V_{C2}$ +0.1	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load)	LC0–3="0"	Typ. ×0.88	1.95	Typ. ×1.12	V
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"		2.16		
			LC0–3="8"		2.19		
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (without panel load)		$3/2 \cdot V_{C2}$ ×0.95		$3/2 \cdot V_{C2}$	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (without panel load)		$2 \cdot V_{C2}$ ×0.95		$2 \cdot V_{C2}$	V
Current consumption	I_{OP}	During HALT (32kHz crystal), LCD power OFF	*1,*2		1	2	µA
		During HALT (32kHz crystal), LCD power ON (V_{C1} standard)	*1,*2		6	12	µA
		During HALT (32kHz crystal), LCD power ON (V_{C2} standard)	*1,*2		4	8	µA
		During HALT (60kHz CR), LCD power OFF	*2		23	45	µA
		During HALT (60kHz CR), LCD power ON (V_{C1} standard)	*2		30	60	µA
		During HALT (60kHz CR), LCD power ON (V_{C2} standard)	*2		26	50	µA
		During execution (32kHz crystal), LCD power ON (V_{C1} standard)	*1,*2		10	19	µA
		During execution (60kHz CR), LCD power ON (V_{C1} standard)	*2		45	80	µA
		During execution (2MHz ceramic), LCD power ON (V_{C1} standard)			500	700	µA
		During execution (4MHz ceramic), LCD power ON (V_{C1} standard)			1,000	1,200	µA
		During execution (1,800kHz CR), LCD power ON (V_{C1} standard)			700	1,000	µA

*1: VDC = "0"
*2: OSCC = "0"

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=-20 to 70°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})		1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=2.2 to 6.4V	without VDC switching			5	ppm
			with VDC switching			10	ppm
Frequency/IC deviation	∂f/∂IC			-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF		10	20		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})		6.4			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}		200			MΩ

OSC1 CR Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR1}=578kΩ, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	60kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.0			V
Oscillation start time	tsta	V_{DD}=2.0 to 6.4V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.0			V

OSC3 Ceramic Oscillation Circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Ceramic oscillator: 4MHz, C_{GC}=C_{DC}=30pF, Ta=-20 to 70°C)

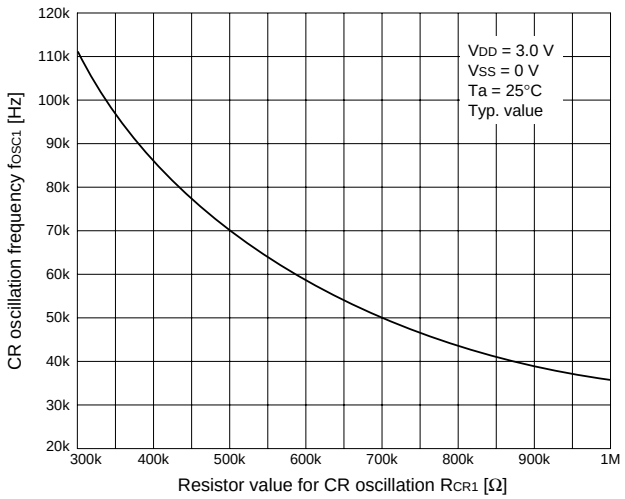
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 6.4V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 CR Oscillation Circuit

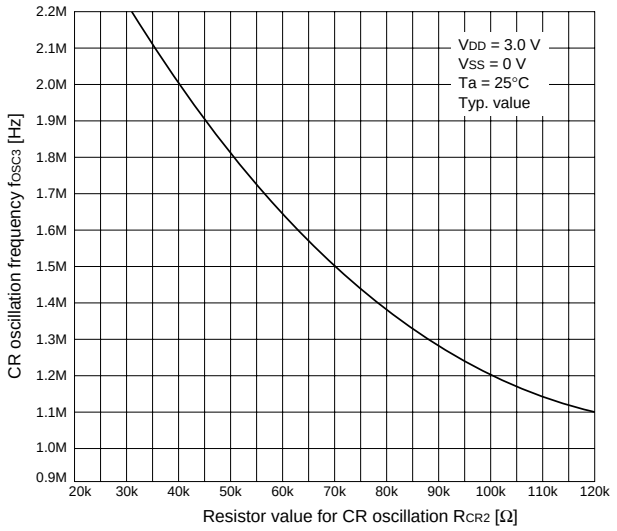
(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR2}=50kΩ, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	1,800kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	1.8			V
Oscillation start time	tsta	V_{DD}=2.0 to 6.4V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	1.8			V

- **OSC1 CR oscillation frequency-resistance characteristic**



- **OSC3 CR oscillation frequency-resistance characteristic**



● Serial Interface AC Characteristics

Clock Synchronous Master Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µS
Receiving data input set-up time	tsms	10			µS
Receiving data input hold time	tsmh	5			µS

• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	nS
Receiving data input set-up time	tsms	400			nS
Receiving data input hold time	tsmh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

Clock Synchronous Slave Mode

• During 32 kHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µS
Receiving data input set-up time	tsss	10			µS
Receiving data input hold time	tssh	5			µS

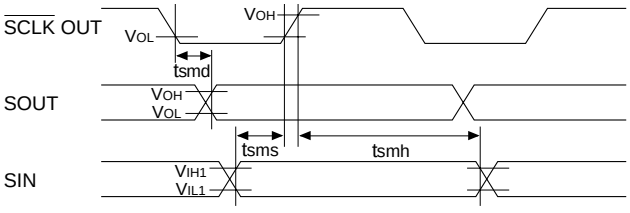
• During 1 MHz operation

(Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=25°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD})

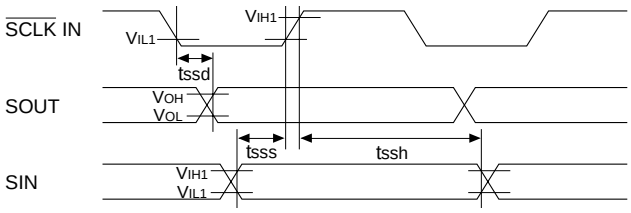
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	nS
Receiving data input set-up time	tsss	400			nS
Receiving data input hold time	tssh	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>

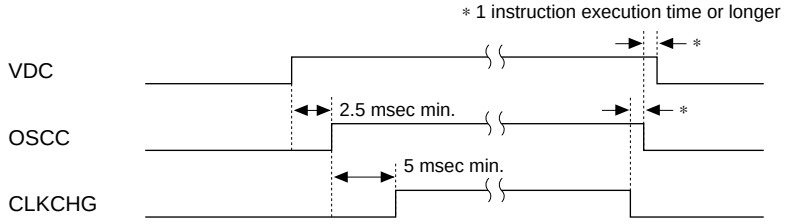


<Slave mode>



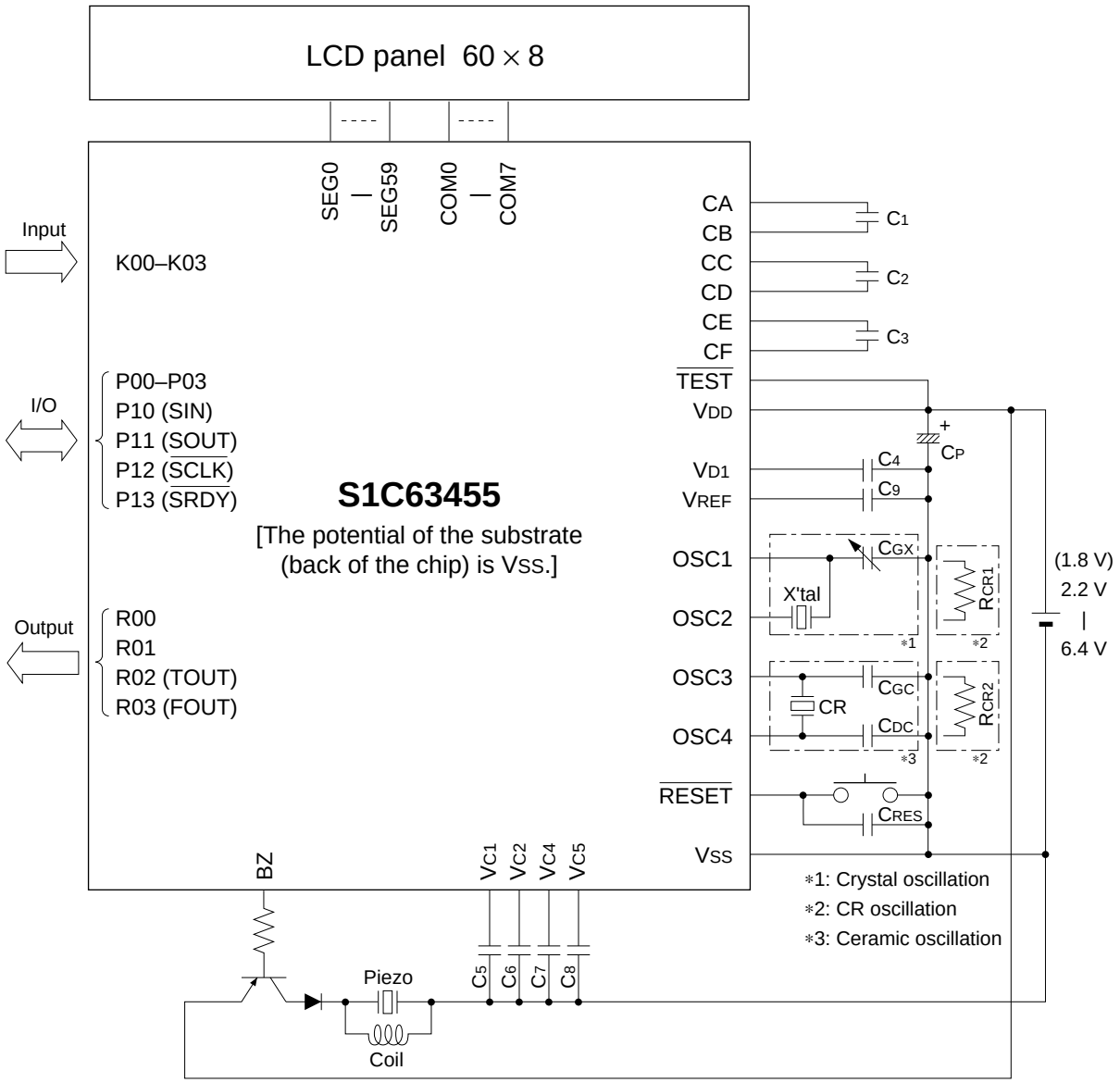
● Timing Chart

System clock switching



(Note) When the OSC1 oscillation circuit has been selected as the CR oscillation circuit, it is not necessary to set the VDC register.
Whether the VDC register value is "1" or "0" does not matter.

■ BASIC EXTERNAL CONNECTION DIAGRAM

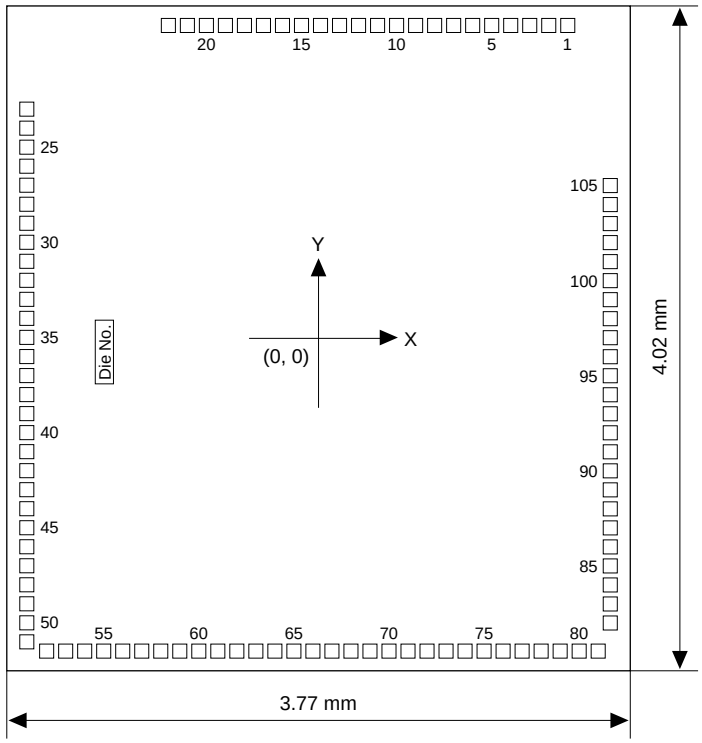


X'tal	Crystal oscillator	32.768 kHz, C_I (Max.) = 34 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
R_{CR1}	Resistor for OSC1 CR oscillation	578 kΩ (60 kHz)
CR	Ceramic oscillator	4 MHz (3.0 V)
C_{GC}	Gate capacitor	30 pF
C_{DC}	Drain capacitor	30 pF
R_{CR2}	Resistor for OSC3 CR oscillation	50 kΩ (1.8 MHz)
C_1–C_8	Capacitor	0.2 µF
C_9	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF
C_{RES}	$\overline{\text{RESET}}$ terminal capacitor	0.1 µF

Note: The above table is simply an example, and is not guaranteed to work.

■ PAD LAYOUT

● Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 85 µm

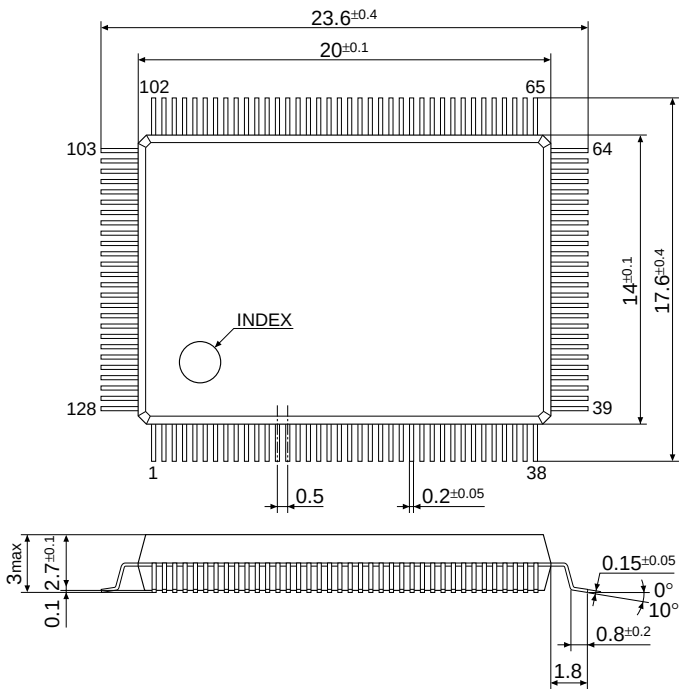
● Pad Coordinates

Unit: µm

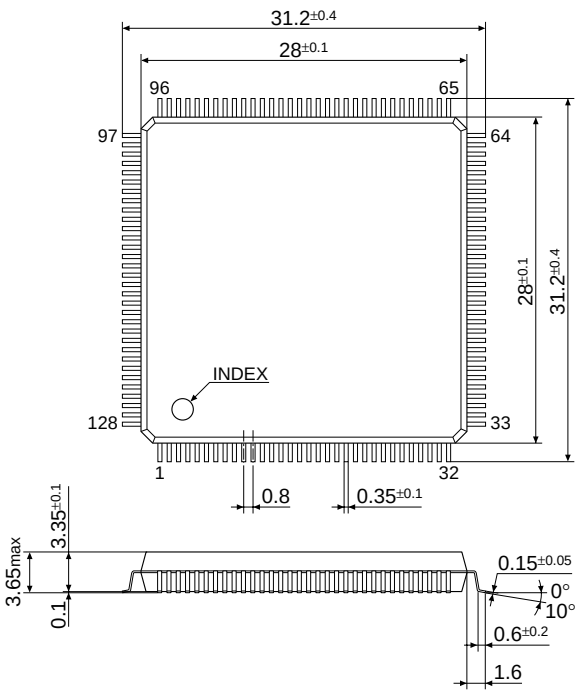
No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	OSC3	1,507	1,892	28	CE	-1,764	811	55	SEG37	-1,299	-1,891	82	SEG10	1,764	-1,721
2	OSC4	1,392	1,892	29	CD	-1,764	696	56	SEG36	-1,184	-1,891	83	SEG9	1,764	-1,606
3	V_{DD}	1,277	1,892	30	CC	-1,764	581	57	SEG35	-1,069	-1,891	84	SEG8	1,764	-1,491
4	$\overline{RESET}$	1,162	1,892	31	CB	-1,764	466	58	SEG34	-954	-1,891	85	SEG7	1,764	-1,376
5	$\overline{TEST}$	1,047	1,892	32	CA	-1,764	351	59	SEG33	-839	-1,891	86	SEG6	1,764	-1,261
6	V_{REF}	932	1,892	33	SEG59	-1,764	236	60	SEG32	-724	-1,891	87	SEG5	1,764	-1,146
7	R03	817	1,892	34	SEG58	-1,764	121	61	SEG31	-609	-1,891	88	SEG4	1,764	-1,031
8	R02	702	1,892	35	SEG57	-1,764	6	62	SEG30	-494	-1,891	89	SEG3	1,764	-916
9	R01	587	1,892	36	SEG56	-1,764	-110	63	SEG29	-379	-1,891	90	SEG2	1,764	-801
10	R00	472	1,892	37	SEG55	-1,764	-225	64	SEG28	-264	-1,891	91	SEG1	1,764	-686
11	P13	357	1,892	38	SEG54	-1,764	-340	65	SEG27	-149	-1,891	92	SEG0	1,764	-571
12	P12	242	1,892	39	SEG53	-1,764	-455	66	SEG26	-34	-1,891	93	COM7	1,764	-456
13	P11	127	1,892	40	SEG52	-1,764	-570	67	SEG25	81	-1,891	94	COM6	1,764	-341
14	P10	12	1,892	41	SEG51	-1,764	-685	68	SEG24	196	-1,891	95	COM5	1,764	-226
15	P03	-103	1,892	42	SEG50	-1,764	-800	69	SEG23	311	-1,891	96	COM4	1,764	-111
16	P02	-218	1,892	43	SEG49	-1,764	-915	70	SEG22	426	-1,891	97	COM3	1,764	4
17	P01	-333	1,892	44	SEG48	-1,764	-1,030	71	SEG21	541	-1,891	98	COM2	1,764	119
18	P00	-448	1,892	45	SEG47	-1,764	-1,145	72	SEG20	656	-1,891	99	COM1	1,764	234
19	K03	-563	1,892	46	SEG46	-1,764	-1,260	73	SEG19	771	-1,891	100	COM0	1,764	349
20	K02	-678	1,892	47	SEG45	-1,764	-1,375	74	SEG18	886	-1,891	101	BZ	1,764	464
21	K01	-793	1,892	48	SEG44	-1,764	-1,490	75	SEG17	1,001	-1,891	102	V_{SS}	1,764	579
22	K00	-908	1,892	49	SEG43	-1,764	-1,605	76	SEG16	1,116	-1,891	103	OSC1	1,764	694
23	V_{C1}	-1,764	1,386	50	SEG42	-1,764	-1,720	77	SEG15	1,231	-1,891	104	OSC2	1,764	809
24	V_{C2}	-1,764	1,271	51	SEG41	-1,764	-1,835	78	SEG14	1,346	-1,891	105	V_{D1}	1,764	924
25	V_{C4}	-1,764	1,156	52	SEG40	-1,644	-1,891	79	SEG13	1,461	-1,891				
26	V_{C5}	-1,764	1,041	53	SEG39	-1,529	-1,891	80	SEG12	1,576	-1,891				
27	CF	-1,764	926	54	SEG38	-1,414	-1,891	81	SEG11	1,691	-1,891				

■ PACKAGE DIMENSIONS

Plastic QFP5-128pin



Plastic QFP8-128pin



Unit: mm

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