Multi-Output, Low-Noise Power Supply Controller for Notebook Computers

SC1402

December 15, 2000

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1402 is pin compatible with the MAX1632 with improved load regulation performance. The SC1402 is a multiple-output power supply controller designed to power logic supply components in battery operated systems. The SC1402 utilizes synchronous rectified buck topologies to generate two voltages, (3.3V and 5V) with up to 95% efficiency. It also provides two linear regulators for system housekeeping functions. The 12V linear regulator output is generated from a coupled inductor of the 5V switching regulator.

Control functions include: power up sequencing, soft start, power-good signaling, automatic bootstrapping for high side MOSFETs, and frequency synchronization. An internal precision 2.5V reference ensures ±2% output voltage. The internal oscillator can be adjusted to 200kHz, 300kHz or synchronized to an external clock. The MOSFET drivers provide 1A peak drive current for fast MOSFET switching.

The SC1402 includes a PSAVE enable input to select a pulse skipping mode for high efficiency or a fixed frequency mode for low noise operation.

FEATURES

- 6V to 30V Input range
- 3.3V and 5V dual synchronous rectified outputs
- Fixed frequency or PSAVE for maximum efficiency over wide load current range
- 5V/50mA linear regulator
- 12V/120mA linear regulator
- Precision 2.5V reference output
- Programmable power-up sequence
- Power good output (RESET)
- Output over current protection
- Output over voltage protection
- Output under voltage shut down
- 4µA typical shut down current
- 7mW typical quiescent power

APPLICATIONS

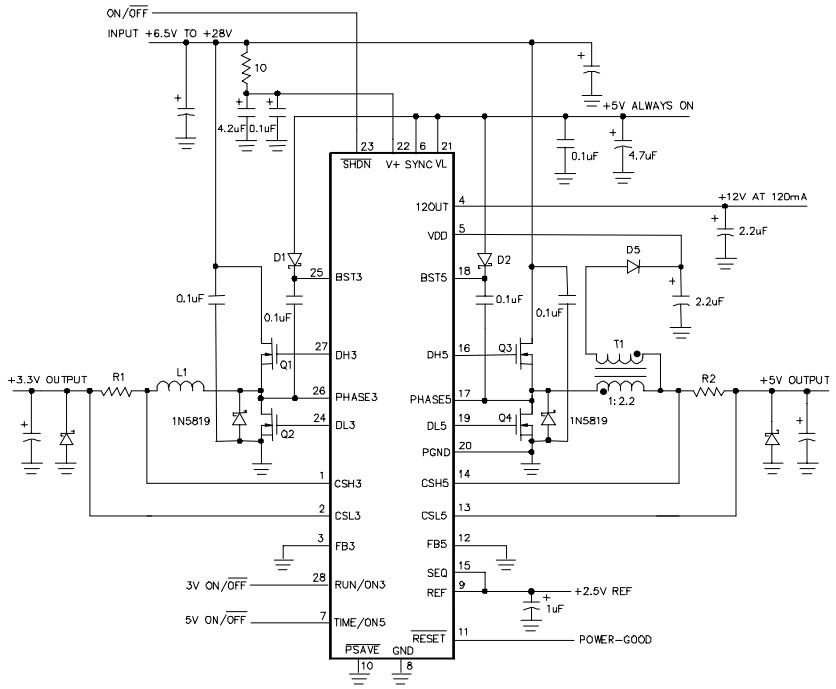
- Notebook and subnotebook computers
- PDAs and Mobile communicators
- Desktop DC-DC converters

ORDERING INFORMATION:

DEVICE	PACKAGE(1)	TEMP. (T_A)
SC1402ISS	SSOP-28	-40 - +85°C

Note:
(1) Only available in tape and reel packaging. (Suffix '.TR').

TYPICAL APPLICATION CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MAXIMUM	UNITS
V+, BST3, BST5 to GND	-0.3, +36	V
PGND to GND	± 0.3	V
PHASE3 to BST3, and PHASE5 to BST5	-6 to +0.3	V
VL to GND	-0.3 to 6	V
REF,SYNC,SEQ,PSAVE,TIME_ON5,RESET to GND	-0.3 to (VL+.3V)	V
RUN/ON3, SHDN to GND	-0.3 to (V+ + 0.3V)	V
VDD to GND	-0.3 to +30V	V
12 Out to GND	-0.3 to (VDD + 0.3V)	V
VL, REF Short to GND	Continuous	sec.
12 Out Short to GND	Continuous	sec.
REF Current	+5	mA
VL Current	+50	mA
12 Out Current	+200	mA
VDD Shunt Current	+15	mA
T_S Storage Temperature	-65 to +150	°C
T_L Lead soldering temperature	+300, 10 seconds	°C

ELECTRICAL CHARACTERISTICS(1)

(Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = VL, VL load = 0mA, REF load = 0mA, PSAVE = 0V, T_A =-40 to +85°C. Typical values are at T_A = +25°C).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SMPS CONTROLLERS					
Input Voltage Range		6.0		30.0	V
3V Output Voltage in Adjustable Mode	V+ = 6V to 30V, CSH3-CSL3 = 0V, CSL3 tied to FB3	2.45	2.5	2.55	V
3V Output Voltage in Fixed Mode	V+ = 6V to 30V, 0mV < CSH3-CSL3 < 80mV, FB3 = 0V	3.17	3.3	3.43	V
5V Output Voltage in Adjustable Mode	V+ = 6V to 30V, CSH5-CSL5 = 0V, CSL5 tied to FB5	2.45	2.5	2.55	V
5V Output Voltage in Fixed Mode	V+ = 6V to 30V, 0mV < CSH5-CSL5 < 80mV, FB5 = 0V	4.82	5.0	5.18	V
Output Voltage Adjust Range	Either SMPS	REF		5.5	V
Adjustable-Mode Threshold Voltage	Dual Mode comparator	0.5		1.3	V
Load Regulation	Either SMPS, 0V < CSH_-CSL_ < 80mV		-0.8		%
Line Regulation	Either SMPS, 6V < V+ < 30V		0.03		%/V
Current-Limit Threshold	CSH3-CSL3 or CSH5-CSL5 PSAVE = VL or V12OUT < 11.9V	80 -50	100 -100	120 -150	mV
PSAVE Mode Threshold	PSAVE = 0V, not tested	10	25	40	mV
Soft-Start Ramp Time	From enable to 95% full current limit with respect to f_{OSC} Note 2.		512		clks
Oscillator Frequency	SYNC = VL SYNC = 0V	270 170	300 200	330 235	kHz
Maximum Duty Factor	SYNC = VL SYNC = 0V		94 96		%

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ELECTRICAL CHARACTERISTICS (continued)

(Unless otherwise noted: (V+ = 15V, both PWMs on, SYNC = VL, VL load = 0mA, REF load = 0mA, PSAVE = 0V, T_A = -40 to +85°C Typical values are at T_A = +25°C).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Input High Pulse[2]		300			ns
SYNC Input Low Pulse Width[2]		300			
SYNC Rise/Fall Time[2]				200	
SYNC Input Frequency Range		240		350	kHz
Current-Sense Input Leakage Current	V+ = VL = 0V, CSL3 = CSH3 = CSL5 = CSH5 = 5.5V		0.01	10	µA
FLYBACK CONTROLLER					
VDD Shunt Threshold	Rising edge, hysteresis = 1%	18		20	V
VDD Shunt Sink Current	VDD = 20V	5	10	30	mA
VDD Leakage Current	VDD = 5V , Standby mode			30	µA
12V LINEAR REGULATOR					
12OUT Output Voltage	0mA < Load < 120mA	11.55	12.1	12.50	V
12OUT Current Limit	12OUT forced to 11V, VDD = 13V		150		mA
12OUT Regulation Threshold	Falling edge		11.9		V
Quiescent VDD Current	VDD = 18V, run mode, no 12OUT load		50	100	µA
INTERNAL REGULATOR AND REFERENCE					
VL Output Voltage	SHDN = V+, 6V < V+ < 30V, 0mA < ILOAD < 50mA, RUN/ON3 = TIME/ON5 = 0V	4.6		5.2	V
Undervoltage Fault Lockout Threshold	Falling edge, hysteresis = 0.9V	3.5	3.7	4.0	
Switchover Threshold	Switch over at startup		4.5		
REF Output Voltage	No external load, Standby Mode	2.45	2.5	2.55	
REF Load Regulation	0µA < LOAD < 50µA			12.5	mV
	0mA < LOAD < 5mA			50	
REF Sink Current			10		µA
REF Fault Lockout Voltage	Falling edge	1.8		2.2	V
V+ Operating Supply Current	VL switched over to CSL5, 5V SMPS on		10	50	µA
V+ Standby Supply Current	V+ = 6V to 30V, SMPS off, includes current into SHDN		180		
V+ Shutdown Supply Current	V+ = 6V to 30V, SHDN = 0V		4	20	
Quiescent Power Consumption	SMPS enabled, FB3 = FB5 = 0V, CSL3 = CSH 3 = 3.5V, CSL5 = CSH5 = 5.5V		7.5		mW

Table 2

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ELECTRICAL CHARACTERISTICS (continued)

(Unless otherwise noted: (V+ = 15V, both PWMs on, SYNC = VL, VL load = 0mA, REF load = 0mA, PSAVE = 0V, T_A = -40 to +85°C Typical values are at T_A = +25°C).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT DETECTION					
Overvoltage Trip Threshold	With respect to unloaded output voltage	3.5	7	10	%
Overvoltage-Fault Propagation Delay	CSL_ driven 2% above overvoltage trip threshold		1.5		µs
Output Undervoltage Threshold	With respect to unloaded output voltage	60	70	80	%
Output Undervoltage Lockout Time	From each SMPS enabled, with respect to f_{OSC}	5000	6144	7000	clks
Thermal Shutdown Threshold	Typical hysteresis = +10°C		150		°C
RESET					
RESET Trip Threshold	With respect to unloaded output voltage, falling edge; typical hysteresis = 1%	-10	-7	-4	%
RESET Propagation Delay	Falling edge, CSL_ driven 2% below RESET trip threshold		1.5		µs
RESET Delay Time	With respect to fOSC	27,000	32,000	37,000	clks
INPUTS AND OUTPUTS					
Logic Input Low Voltage	RUN/ON3, PSAVE, TIME/ON5 (SEQ = REF), SHDN, SYNC			0.6	V
Logic Input High Voltage	RUN/ON3, PSAVE, TIME/ON5 (SEQ = REF), SHDN, SYNC	2.4			V
Input Leakage Current	RUN/ON3, PSAVE, TIME/ON5 (SEQ = REF), SHDN, SYNC, SEQ = 0V or 3.3V			±1	µA
Logic Output Low Voltage	RESET, ISINK = 4mA			0.4	V
Logic Output High Current	RESET = 3.5V	1			mA
TIME/ON5 Input Trip Level	SEQ = 0 or VL	2.4		2.6	V
TIME/ON5 Source Current	TIME/ON5 = 0V, SEQ = 0 or VL	2	3	4	µA
TIME/ON5 On-Resistance	TIME/ON5, RUN/ON3 = 0V, SEQ = 0 or VL		100		Ω
Gate Driver Sink/Source Current	DL3, DH3, DL5, DH5, forced to 2V		1		A
Gate Driver On-Resistance	High or low		1.5	7	Ω

Note 1: This device is ESD sensitive. Use of standard ESD handling precautions is required.
Note 2: Guaranteed by design.

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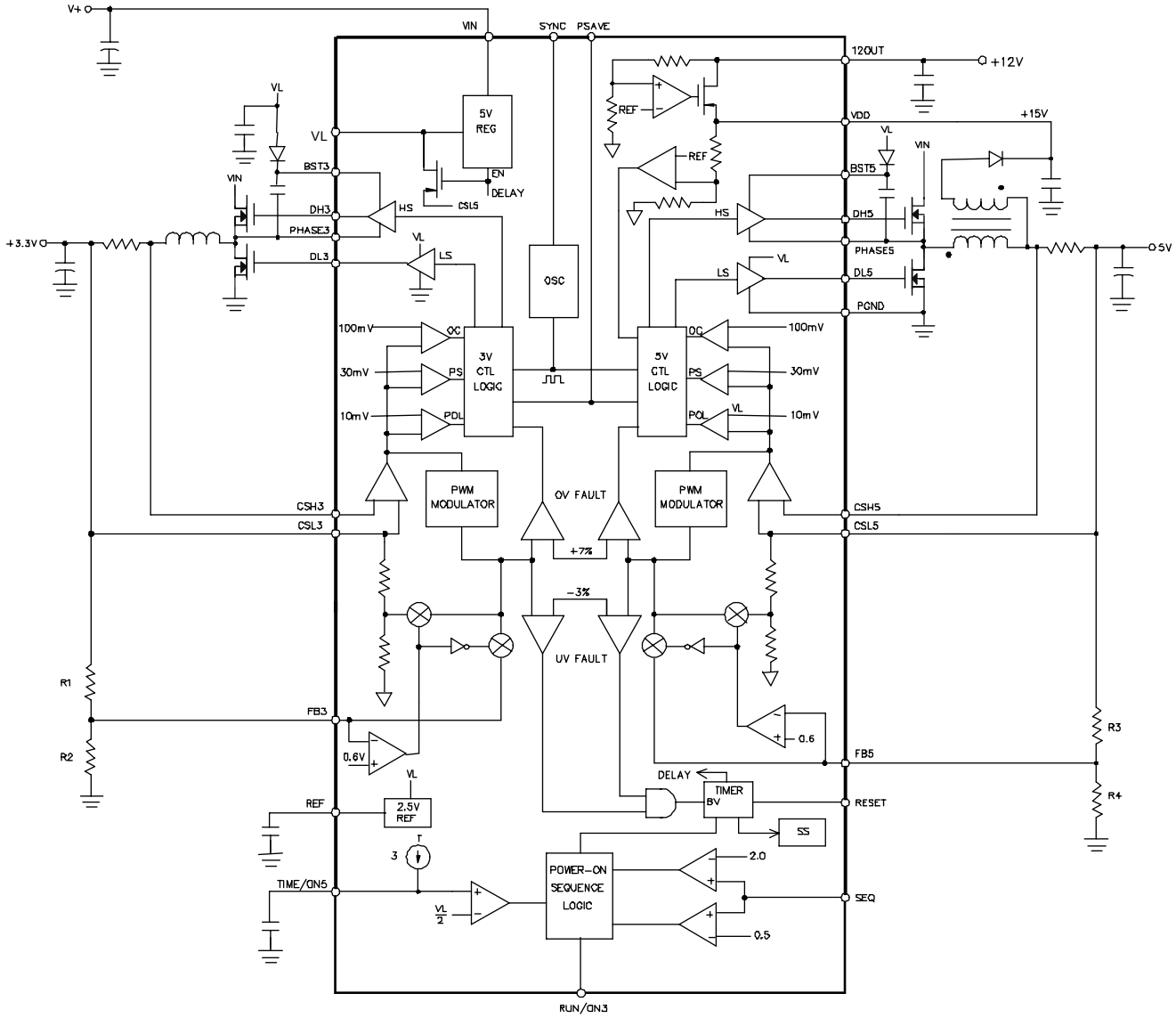
BLOCK DIAGRAM



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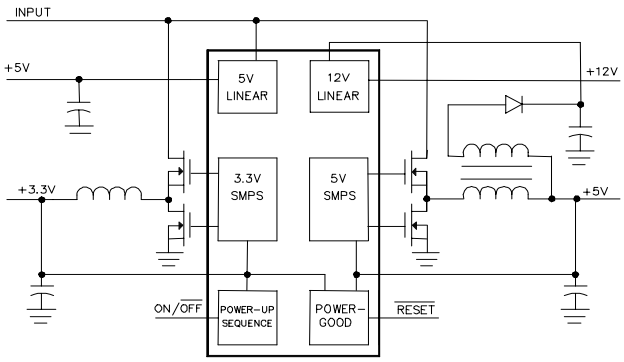
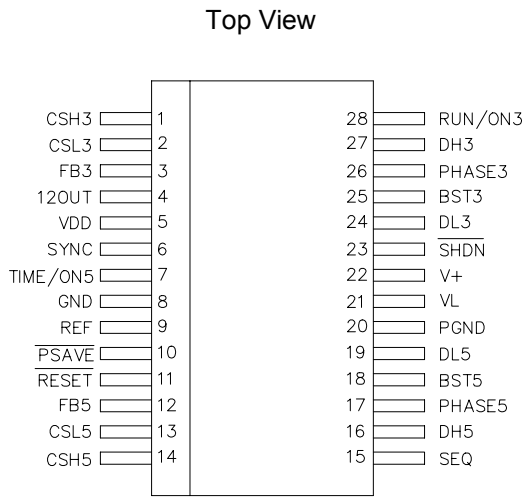
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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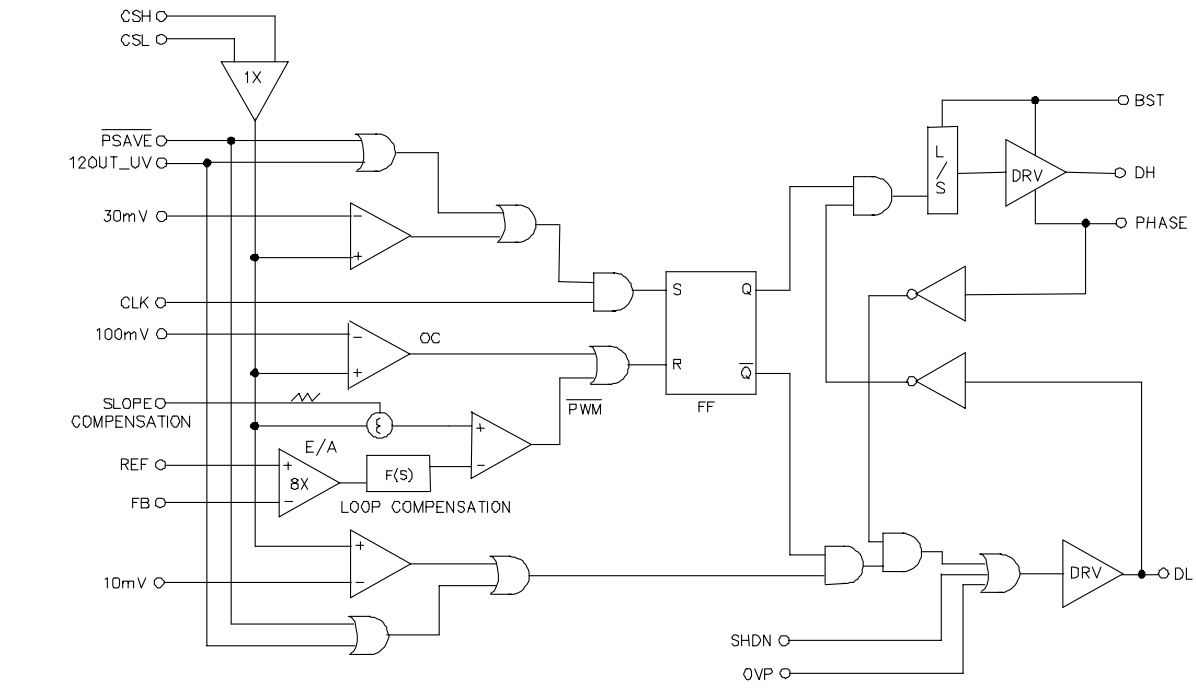
PWM CONTROLLER DIAGRAM (Fig. 1)



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PIN DESCRIPTION

Pin #	Pin Name	Pin Function
1	CSH3	Current Sense Input for the 3.3V SMPS. Current limit level is 100mV referred to CSL3.
2	CSL3	Current Sense Input. Also serves as the feedback input in fixed output mode.
3	FB3	Feedback Input for the 3.3V SMPS; Connect FB3 to a resistor divider for adjustable output mode and FB3 is regulated to REF (approx. 2.5V). FB3 selects the 3.3V fixed output voltage setting when tied to GND.
4	12 OUT	12V, 120mA Linear Regulator Output. Input supply comes from V_{DD}. Bypass 12 OUT to GND with 1µF minimum capacitor.
5	VDD	Supply Voltage Input for the 12 OUT Linear Regulator. Also connects to a 18V overvoltage shunt regulator clamp.
6	SYNC	Oscillator Synchronization and Frequency Select. Tie to VL for 300kHz operation; tie to GND for 200kHz. Driven externally to SYNC between 240kHz and 350kHz.
7	TIME/ON5	Dual Purpose Timing Capacitor Pin and 5V SMPS ON/OFF Control Input. Input resistor of 1K is required when using ON/OFF control input.
8	GND	Low noise Analog Ground and Feedback reference point.
9	REF	2.5V Reference Voltage Output. Bypass to GND with 1µF minimum capacitor.
10	$\overline{\text{PSAVE}}$	Logic Control Input that disables PSAVE Mode when high. Connect to GND for power save mode.
11	$\overline{\text{RESET}}$	Active Low Timed Output. RESET swings from GND to VL. Goes high after 32,000 clock cycle delay following power up as a power good signal.
12	FB5	Feedback Input for 5V SMPS; Connect FB5 to a resistor divider for adjustable output mode and FB5 regulates to REF (approx. 2.5V). FB5 selects the 5V fixed output voltage setting when tied to GND.
13	CSL5	Current Sense Input for 5V SMPS.
14	CSH5	Current Sense Input for 5V SMPS.
15	SEQ	Input that selects SMPS power up sequence.
16	DH5	Gate Drive Output for the 5V, high side N-Channel MOSFET.
17	PHASE5	Switching Node inductor connection.
18	BST5	Boost capacitor connection for 5V, SMPS high-side gate drive. Connect a 0.1µF capacitor.
19	DL5	Gate Drive Output for the 5V, SMPS low-side N-Channel MOSFET.
20	PGND	Power Ground.
21	VL	5V, Internal Linear Regulator Output.
22	V+	Battery Voltage Input.
23	$\overline{\text{SHDN}}$	Shutdown Control Input, active low.
24	DL3	Gate Drive Output for the 3.3V, SMPS low-side N-Channel MOSFET.
25	BST3	Boost Capacitor Connection for high side gate drive. Connect a 0.1µF capacitor.
26	PHASE3	Switching Node inductor Connection.
27	DH3	Gate Drive Output for the 3.3V, high-side N-Channel MOSFET.
28	RUN/ON3	ON/OFF Control Input of 3.3V SMPS.

Note: All logic level inputs and outputs are open collector TTL compatible.

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Detailed Description

The SC1402 is a multiple-output, high efficiency, versatile power supply controller designed to power battery operated systems. Four high current gate drive outputs are supplied to control all MOSFETs in two synchronous rectified buck converters. These buck converters can be programmed to operate at either fixed or adjustable output voltages. The power save feature of the SC1402 achieves high efficiency over a wide range of load current. The control and fault monitoring circuitry associated with each PWM controller includes digital softstart, turn-on sequencing, voltage error amplifier with slope compensation, pulse width modulator, power save, over-current and over-voltage and under voltage fault protection. Two linear regulators and a precision reference voltage are also provided by the SC1402.

PWM Control Block

The two PWM control blocks for the 3V and 5V power supply outputs are identical. The SC1402 employs peak current mode control with slope compensation to provide fast output response to load and line transients. The PWM control block consists of an analog PWM modulator followed by PWM logic control. The analog modulator combines the output current, slope compensation signal and error voltage to generate a PWM pulse train. The PWM logic uses the pulse train from the modulator and other control signals to generate the output states for the high and low side gate driver outputs. A block diagram of the PWM control block is shown in Fig. 1.

An error amplifier generates the difference signal between the reference voltage and the feedback voltage to generate the error voltage for the peak current mode comparator. A nominal gain of 8 is used in the error amplifier to increase the system loop gain and to reduce the load regulation error typically seen in low loop-gain, current-mode controllers. The increased gain in the voltage loop is compensated by pole-zero-pole response of the voltage error amplifier. The current feedback signal is summed with the slope compensation signal and compared to the error voltage at the PWM comparator.

When the power supply is operating in continuous conduction mode, the high-side MOSFET is turned on at the beginning of each switching cycle. The high-side MOSFET is turned off when the desired duty cycle is reached. Active shoot-thruough protection delays the turn-on of the low-side MOSFET until the phase node drops below 2.5V. The low-side MOSFET remains on until the beginning of the next switching cycle. Again, active shoot-through protection ensures that the gate to the low-side MOSFET has dropped low before the high side MOSFET is turned on.

When PSAVE is enabled (low) and the output current drops below 25% of its peak level, the PWM logic will automatically enter PSAVE mode to improve efficiency. When the controller enters power save, it increases the regulation point by 0.8%, typically issuing one more high side pulse as the converter enters PSAVE. The PWM control then disables switching cycles until the FB falls below the reference. At light loads the effective switching frequency will drop dramatically and efficiency will increase because of the reduced gate charge current required to switch the power stage. Boosting the regulation point when entering PSAVE gives the output improved dynamic regulation because the output voltage is not allowed to droop below the nominal regulation point. Load current steps, that cause the converter to come out of PSAVE, will not cause as large a negative dip in the output voltage.

Gate Drive/Control

The gate driver on the SC1402 are designed to switch large MOSFETs up to 350kHz. The high side gate driver is required to drive the gates of the high side MOSFET above the V+ input. The supply for the gate driver is generated by charging a bootstrap capacitor from the VL supply when the low-side driver is on. Monitoring circuit ensures that the bootstrap capacitor is charged when coming out of shutdown or fault conditions where the bootstrap capacitor may be depleted.

In continuos conduction mode, the low-side driver output that controls the synchronous rectifier in the power stage is on when the high-side driver is off. Under light load conditions the inductor ripple current will approach the point where it reverses polarity. This is detected by the low side driver control and the synchronous rectifier is turned off before the current reverses, preventing energy drain from the output. The low-side driver operation is also affected by various fault conditions as described in the Fault Protection section.

Internal Bias Supply

The VL linear regulator provides a 5V output that is used to power the gate drivers, 2.5V reference, and internal control sections of the SC1402. The regulator is capable of supplying up to 50mA (including MOS-

FET gate charge current). The VL pin should be bypassed to GND with 4.7uF to supply the peak current requirements of the gate driver outputs.

This regulator receives its input power from the V+ battery input. Efficiency is improved by providing a bootstrapping mode for the VL bias. When the 5V SMPS output voltage reaches 5V, internal circuitry detects this condition and turns on a PMOS pass device between CSL5 and VL. The internal VL regulator is then disabled and the VL bias is provided by the high efficiency switch mode power supply.

The REF output is accurate to +/- 2% over temperature. It is capable of delivering 5mA max and should be bypassed with 1uF minimum capacitor. Loading the REF output will reduce the REF voltage slightly.

Current Sense (CSH,CSL)

The output current of the power supply is sensed as the voltage drop across an external resistor between the CSH and CSL pins. Over-current is detected when the current sense voltage exceeds +/-100mV. The negative current limit (i.e. -100mV) is required for operation with PSAVE mode disabled, and also to limit the output current when charging the bulk supply capacitor of the 12V regulator. A positive over-current will turn off the high-side driver, a negative over-current will turn off the low-side driver, each on a cycle by cycle basis. The current sense is also used for peak current feed back in the main PWM loop and for determining the current level for entering power save mode and the turn off time for the synchronous rectifier.

Oscillator

The SC1402 oscillator frequency is trimmed to +/- 10%. When the SYNC pin is set high the oscillator runs at 300kHz; when SYNC is set low the frequency is 200kHz. The oscillator can also be synchronized to the falling edge of a clock on the SYNC pin with a frequency between 240kHz and 350kHz. In general, 200kHz operation is used for highest efficiency, and the 300kHz for minimum output ripple and/or smaller inductor and output capacitor sizes.

Fault Protection

In addition to cycle-by-cycle current limit, the SC1402 monitors over-temperature, and output over-voltage and under-voltage conditions. The over-temperature detect will shut the part down if the die temperature exceeds 150°C with 10°C of hysteresis.

If either SMPS output is greater than 7% above its nominal value, both SMPS are latched off and synchronous rectifiers are latched on. To prevent the output from ringing below, ground a 1A Schottky diode should be placed across each output, anode at GND.

Two different levels of undervoltage are detected. If the output falls 5% below its nominal output, the RESET output is pulled low. If the output falls 30% below its nominal output following a startup delay, both SMPS are latched off.

Both of the latched fault modes will remain in effect until SHDN or RUN/ON3 is toggled or the V+ input is brought below 1V.

Shutdown and Operating Modes

Holding the SHDN pin low disables the SC1402, reducing the V+ input current to <10uA. When SHDN goes high, the part enters a standby mode where the VL regulator and VREF are enabled. Turning on either SMPS will put the SC1402 in run mode.

$\overline{\text{SHDN}}$	RUN/ ON3	TIME/ ON5	MODE	DESCRIPTION
Low	X	X	Shut-down	Minimum bias current
High	Low	Low	Standby	VREF and VL regulator enabled
High	High	High	Run Mode	Both SMPS Running

Output Voltage Selection

If FB is connected to ground, internal resistors setup 3.3V and 5V output voltages. If external resistors are used, the internal feedback is disabled and the output is regulated based on 2.5V at the FB pin.

12OUT Supply

The 12OUT linear regulator is capable of supplying 120mA. The input voltage to the 12OUT regulator is generated by a secondary winding on the 5V SMPS

inductor.

A heavy load on the 12OUT regulator when the 5V SMPS is in PSAVE will cause the VDD input to drop, browning out the regulator. If the output drops 0.8% from its nominal value, the 5V SMPS is forced out of PSAVE mode and into continuous conduction mode for 8 cycles. This recharges the bulk input capacitor on VDD. The 12OUT linear regulator has a current limit to prevent damage under short circuit conditions.

Over-voltage protection is provided on the VDD input. If the VDD input is above 19V, an over-voltage is detected and a 10mA current shunt load is applied to VDD. The over-voltage threshold has 0.5V of hysteresis.

Power up Controls and Soft Start

The user has control of the SC1402 startup sequence by setting the SEQ, RUN/ON3 and TIME/ON5 pins as described in the following table.

Each SMPS contains its own counter and DAC to gradually increase the current limit at startup to prevent input surge currents. The current limit is increased from 0, 20%, 40%, 60%, 80%, to 100% linearly over the course of 512 switching cycles.

A RESET output is also generated at startup. The RESET pin is held low for 32K switching cycles. Another timer is used to enable the undervoltage protection. The undervoltage protection circuitry is enabled after 6144 switching cycles at which time the SMPS should be in regulation.

When SEQ is set to REF, the RESET only monitors the 3.3V SMPS in regulation. The 5V SMPS is ignored.

SEQ	RUN/ON3	TIME/ON5	RESET	DESCRIPTION
REF	LOW	LOW	Follows 3.3V SMPS.	Independent start control mode. Both SMPSs off.
REF	LOW	HIGH	Low.	5V SMPS ON, 3.3V SMPS OFF.
REF	HIGH	LOW	Follows 3.3V SMPS.	3.3V SMPS ON, 5V SMPS OFF.
REF	HIGH	HIGH	Follows 3.3V SMPS.	Both SMPSs on.
GND	LOW	TIMING CAP	Low.	Both SMPS off.
GND	HIGH	TIMING CAP	High after both outputs are in regulation.	5V starts on rising edge of RUN/ON3, 3V starts when TIME/ON5 > REF.
VL	LOW	TIMING CAP	Low.	Both SMPS off.
VL	HIGH	TIMING CAP	High after both outputs are in regulation.	3.3V starts on rising edge of RUN/ON3, 5V starts when TIME/ON5 > REF.

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APPLICATION INFORMATION

Introduction

The SC1402 is a versatile dual switching regulator adjustable from 2.5V to 5.5V with fixed 5V and 3.3V modes. In addition, there are two on-chip 12V & 5V linear regulators capable of supplying 120mA & 50mA of output current, respectively. The SC1402 is designed for notebook applications but has applications anywhere high efficiency, small size and low cost are required.

The Semtech SC1402 EVAL board consists of a 3.3V, 3A switcher, a 5.0V, 3A switcher, an onboard 12V linear regulator. A 15V flyback supply developed off the 5V SMPS inductor delivers the input voltage to the onboard 12V linear regulator.

Design Guidelines

The schematic for the EVAL board is shown on page 18. The EVAL board is configured as follows:

Switching Regulator 1	Vout1 = 3.3V, 3A
Switching Regulator 2	Vout2 = 5.0V, 3A
Linear Regulator 1	Vout3 = 12V, 120mA
Linear Regulator 2	Vout4 = 5V, 50mA

Designing the Output Filter

Before calculating the output filter inductance and output capacitor, an acceptable amount of output ripple current is to be determined. The ESR of the output capacitor multiplied by the ripple current sets the maximum allowable ripple voltage. So once the ripple voltage specification is selected, the capacitor ESR is chosen usually based on capacitor cost and size constraints. This then sets the maximum output ripple current through the capacitor and inductor.

For the EVAL board 3.3V switcher, we selected a maximum ripple voltage of 50mV. Choosing two 330uF, 6.3V tantalum capacitors C21 & C22, each having an ESR of 100mΩ, their combined ESR equaling 50mΩ, sets the maximum ripple current as follows:

$$\Delta I_O = \frac{\Delta V_O}{ESR} \qquad \Delta I_O = \frac{0.05}{0.05} = 1Amp$$

Be sure that the two output capacitors can handle this ripple current. Ripple current specifications are found in the capacitor data sheet for high quality capacitors intended for use in switching power supplies.

The inductance can now be found:

$$L1 = \frac{(V_{INMAX} - V_O) \bullet D \bullet t}{\Delta I_O}$$

These inductance and duty cycle equations exclude any resistive drops due to winding resistance and MOSFET on resistance.

Where:

For f = 300KHz, t = 1/f

$$D = \frac{V_O}{V_{IN}}; L1 = \frac{(28 - 3.3) \bullet \frac{3.3}{28} \bullet 3.33 \bullet 10^{-6}}{1}$$

From this calculation we choose L1 to be 10uH.

For a 200kHz operating frequency, L1 calculates to be 14.5uH.

Choosing Inductor & FET Current Rating

The current carrying capability of the inductor and MOSFETs should be sized to handle the maximum current of the supply set by the current sense resistor, Rsense = R9. Here we use the minimum current threshold value:

$$R9 = \frac{80mV}{I_{PEAK}}$$

Where Ipeak equals:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_O}{2}$$

Ipeak = 3.5 Amps

$$R9 = \frac{0.080}{3.5} = 0.023\ \Omega$$

Here we chose a sense resistor of 20mΩ. Now we can determine FET and inductor current carrying capability

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by using the maximum current limit threshold:

$$I_{PEAK} = \frac{0.120}{R9} = \frac{0.120}{0.020} = 6$$

From this value choose an inductor with Isat > 6 Amps, and for the FET choose a continuous conduction current rating greater than 6 Amps.

The same calculation process can be made for the 5V supply for its Inductor L2 and Rsense resistor, R8.

The results are:

L2 = 13.4 uH at 300KHz, 20uH at 200KHz, For our EVAL board we choose the transformer with a 11uH primary at the expense of slightly higher ripple current.
R8 = 0.02 Ω
Co = C18 = 330uF/10V

Calculating output capacitance and ESR for Stability.

Now that the basic output filter has been designed, it is time to check if the output filter will allow stable operation. Since the control loop is internal to the SC1402, the output filter capacitor and its associated equivilant series resistance (ESR), will effect stability. It is important to choose a capacitor with its ESR for stable SMPS operation. A seven step procedure for choosing the output capacitor and ESR ensuring a stable control loop is shown below for the 3.3V supply. The same procedure should also be implemented for the 5V supply.

System Paramaters:
Fs = 300000Hz Vout = 3.3V Vinmin = 6V
Vref = 2.5V Rs = 0.020 Ω

Where Fs is the switching frequency.
Vout is the output voltage.
Vinmin is the minimum input voltage.
Vref is the SC1402 reference voltage.
Rs is the sense resistor, (R9 on the EVAL board).

Step 1: Determine the Crossover Frequency

$$Fc = \frac{Fs}{3 \bullet \left(1 + \frac{Vout}{Vinmin}\right)}$$

$$Fc = 64.516KHz$$

Step 2: Determine the Maximum & Minimum ESR Capacitance

$$ESRmax = \frac{Vout}{Vref} \bullet Rs$$

$$ESRmax = 0.026\Omega$$

$$ESRmin = \frac{ESRmax}{(1.2)^2}$$

$$ESRmin = 0.018\Omega$$

Step 3: Determine the Minimum Output Capacitance

$$Comin = \frac{Vref}{2 \bullet \pi \bullet Fc \bullet Vout \bullet Rs \bullet \tan(30^0)}$$

$$Comin = 162uF$$

Step 4: Determine the Actual Output Capacitance

$$Co = \frac{ESRmax}{ESRmin} \bullet Comin$$

$$Co = 233uF$$

Step 5: Determine the Actual ESR Value

$$ESR = \frac{ESRmax + ESRmin}{2}$$

$$ESR = 0.022\ \Omega$$

Step 6: From Above Calculations Choose:

$$Co \geq 233uF$$

$$ESR = 0.022\ \Omega$$

Step 7: Check the Ripple Current

If Co can handle the ripple current you're done. Otherwise increase the output capacitance to handle the ripple current at maximum Vin and recheck the ESR using the equation for determining the actual output capacitance.

If you are using tantalum or electrolytic capacitors you should increase the capacitance to the level of approaching the calculated ESR.

If you are using poly capacitors a small resistor in series with the capacitor to bring the ESR to the desired level may be necessary for stability due to their low ESR values.

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If your ESR value varies significantly from the calculated value and you don't want to add more capacitance or add a series resistor in the capacitor path as described above. We recommend that you bench test the supply over temperature to verify transient response and operation of the SMPS.

Input Capacitor Selection

Input capacitor is selected based upon the input ripple current demand of the converter. First determine the input ripple current expected and then choose a capacitor to meet that demand.

The input RMS ripple current can be calculated as follows:

$$I_{RMS} = \sqrt{V_{OUT} \bullet (V_{IN} - V_{OUT})} \bullet \frac{I_{OUT}}{V_{IN}}$$

The worse case input RMS ripple current occurs at 50% duty cycle (D = 0.5 or Vin = 2 Vout) and therefore under this condition the I_{RMS} ripple current can be approximated by:

$$I_{RMS} = \frac{I_{LOAD}}{2}$$

Therefore, for a maximum load current of 3.0A , the input capacitors should be able to safely handle 1.5A of ripple current. For the EVAL board there are two such regulators that operate simultaneously. Each capable of 1.5A of ripple current, although it is impossible for both regulators to be at 50% duty cycle at the same time since they have different output voltages. For the EVAL board, we chose four 10uF, 30V OS-CON capacitors, two for each supply. Each capacitor has a ripple current capability of 1.38A at 100KHz, 45°C. Following the capacitor-derating chart for temperature and frequency operation at 300KHz, two of these capacitors in parallel will suffice, as calculated below:

The RMS ripple current is under a worst-case condition at full load, 3A each when both SMPSs are on.

When the 5V output is at maximum ripple of 1.5A (D = 50%), the 3.3V output adds 1.41A of ripple current.

The maximum ripple current is then calculated by:

$$I_{RMS(MAX)} = \sqrt{1.5^2 + 1.41^2} = 2.06A$$

Conversely:
When the 3V output is at maximum ripple 1.5A (D = 50%), the 5V output adds 1.29A of ripple current.

The worse case ripple current is then calculated by:

$$I_{RMS(MAX)} = \sqrt{1.5^2 + 1.29^2} = 1.98A$$

Clearly, the combined input capacitor bank must be chosen to handle 2A of ripple current under worst-case conditions.

MOSFET Switches

After selecting the voltage and current requirements of each MOSFET device for the upper and lower switches, the next step is to determine their power handling capability. For the EVAL board the IRF7413 met the voltage and current requirements. These are 30V, 9A FET's. Based on 85^{0}C ambient temperature, 150^{0}C junction temperature and thermal resistance, their power handling is calculated as follows:

Power Limit for Upper & Lower FET:

T_J = 150^{0}C; T_A = 85^{0}C; θ_{ja} = 50°C/W

$$P_T = \frac{T_J - T_A}{\theta_{JA}} = \frac{150 - 85}{50} = 1.3W$$

Each FET must not exceed 1.3W of power dissipation. The conduction losses for the upper & lower FET can be determined. For the calculations below, a nominal input voltage of 12V, for Vout = 3.3V, Iout = 3A and f = 300KHz. The Rdson value for the upper & lower FET is 11mΩ. We will calculate the conduction losses and switching losses for each FET. From the calculations below we are well within the 1.3W dissipation limit as calculated above.

Conduction Losses Upper FET:

$$P_{CU} = R_{DS} \bullet D \bullet I^2$$

$$P_{CU} = 0.011 \bullet \frac{3.3}{12} \bullet 3^2 = 0.027W$$

Conduction Losses Lower FET:

$$P_{CL} = R_{DS} \bullet (1 - D) \bullet I^2$$

$$P_{CL} = 0.011 \bullet \left(1 - \frac{3.3}{12}\right) \bullet 3^2 = 0.072W$$

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Switching Losses Upper FET:

$$P_{SU} = \frac{C_{RSS} \bullet V_{IN}^{2} \bullet F \bullet I_{OUT}}{I_G} = \frac{240 \bullet 10^{-12} \bullet 12^{2} \bullet 300000 \bullet 3}{1} = 0.031W$$

Note: switching losses exist on the upper FET only because the clamp diode across the lower FET will turn on prior to the lower FET turning on.
Where Ig is the gate driver current. This is equal to 1A for the SC1402.

Crss is the reverse transfer capacitance of the FET; in this case it equals 240pF for the IRF7413.

So the total FET losses equate to:

P_{FETS} = 0.027+0.072+0.031 = 0.130W

Note that as Vin increases the power dissipation from switching losses will also increase. This is especially important if the input to the supply is from an AC adapter. Therefore, it is necessary to check the calculations with your maximum input voltage specification. In addition, the distribution of power in the upper and lower FET will change as input voltage increases.

Other losses to consider are gate charge losses, inductor switching and copper losses, and losses in the input and output capacitors. All these items will decrease efficiency and need to be carefully analyzed to obtain the highest efficiency possible, especially if running off battery power.

Basic Application Circuit

The basic dual-output 3.3V / 5V synchronous buck converter is shown in Figure 2. This circuit shows the minimum requirements for successful operation. For varying current levels, Table 3 provides a useful selection of components for varying supply requirements and is based on the calculations described previously. Input voltage ranges for all designs in the table are 6.5V to 28V. Frequency used in calculations is 300KHz.

	2A	3A	4A
High & Low Side FET's	IR IRF7901D1 Siliconix Si4412	IR IRF7413 Siliconix Si4412	IR IRF7805 Siliconix Si4410
Input Capacitor	10uF, 30V Sanyo OS-CON	2 X 10uF, 30V Sanyo OS-CON	3 X 10uF, 30V Sanyo OS-CON
Output Capacitor	330uF, 6.3V/10V* AVX TPS	2X 330uF, 6.3V/10V* AVX TPS	4X 330uF, 6.3V/10V* AVX TPS
Resistor	0.033Ω, Dale WSL2010-R033-F	0.02Ω, Dale WSL2010-R020-F	0.012Ω, Dale WSL2512-R012-F
Inductor	15uF, Coilcraft DO-3316P-153	10uF, Coilcraft DO3316P-103	4.7uF, Coilcraft DO3316P-472
*10V for 5V SMPS, 6.3V for 3V SMPS			

Table 3

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PCB Layout

As with any high frequency switching regulator it is advisable to practice a careful layout strategy. This includes keeping loop area as small as possible. Properly decoupling lines that pull large amounts of current in short periods of time. To keep loop area small always use a ground plane and if possible split the plane in two areas, signal GND and power GND then tie the two together at one point. Be sure that high current paths have low inductance by making track widths wide where possible. We recommend the following layout for the SC1042 shown below. This layout has been optimized for having tight loop areas and bypassing the SC1402 properly.

652 MITCHELL ROAD NEWBURY PARK CA 91320

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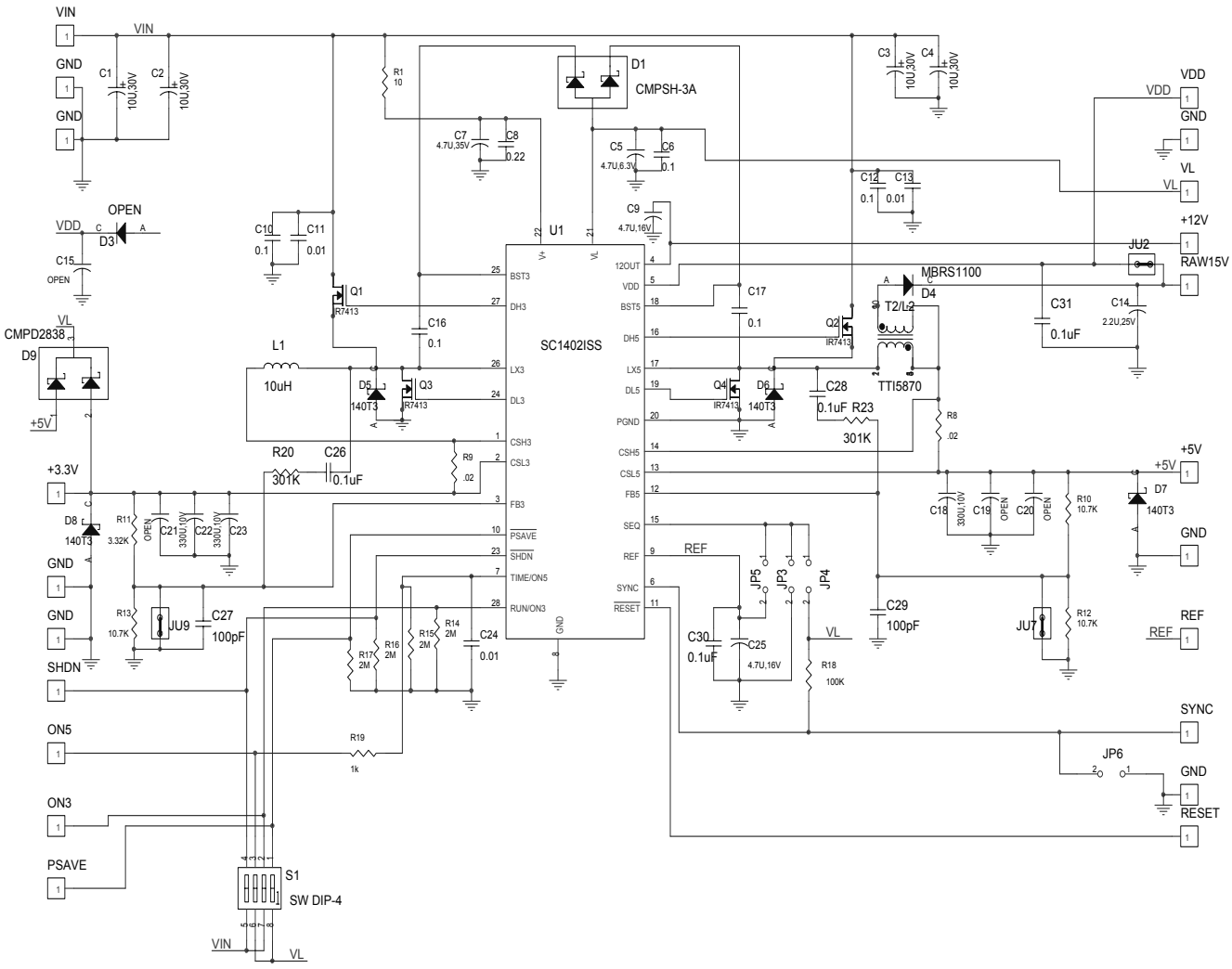
EVALUATION BOARD SCHEMATIC



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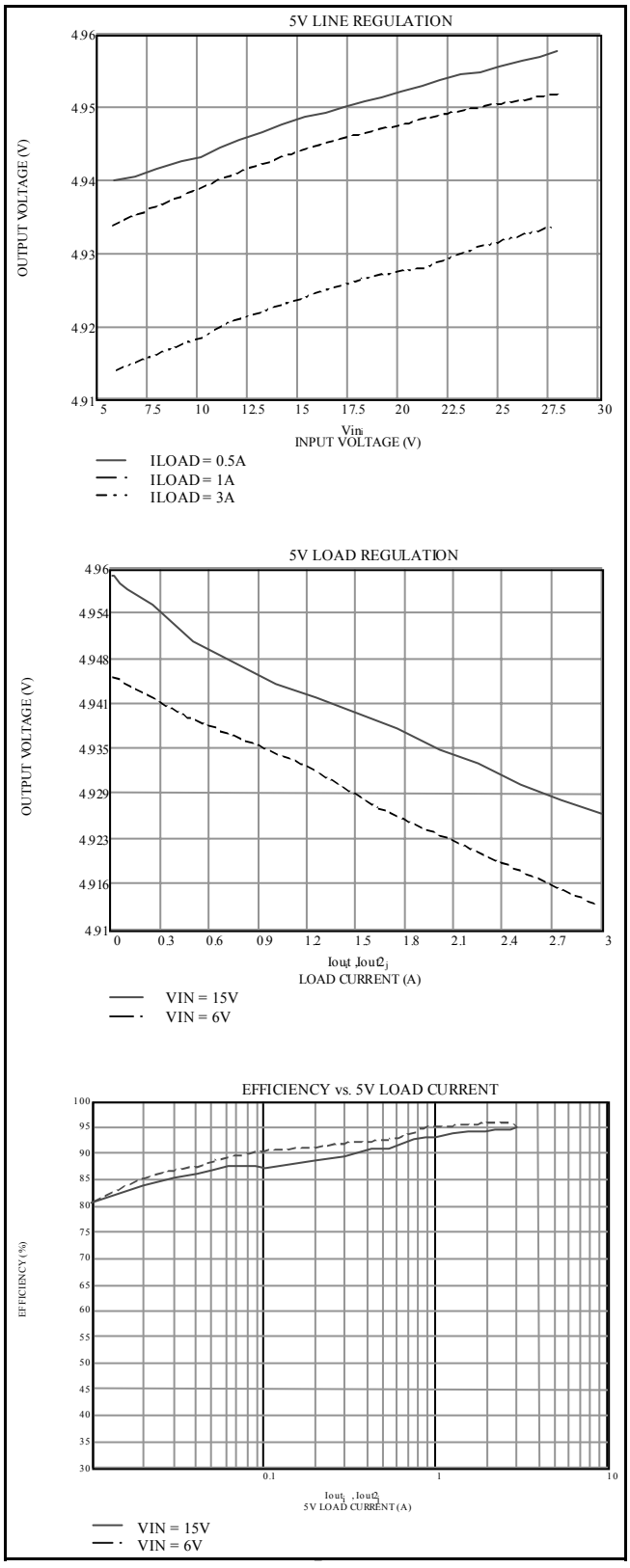

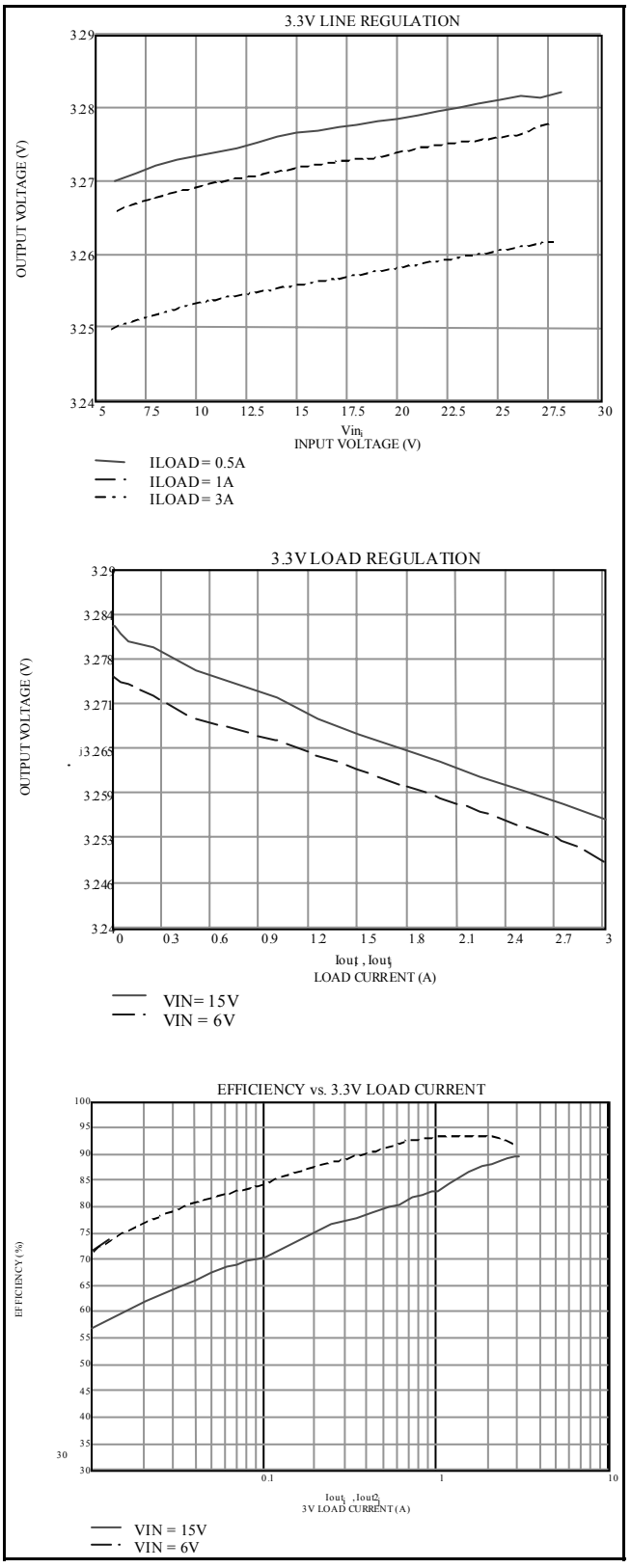

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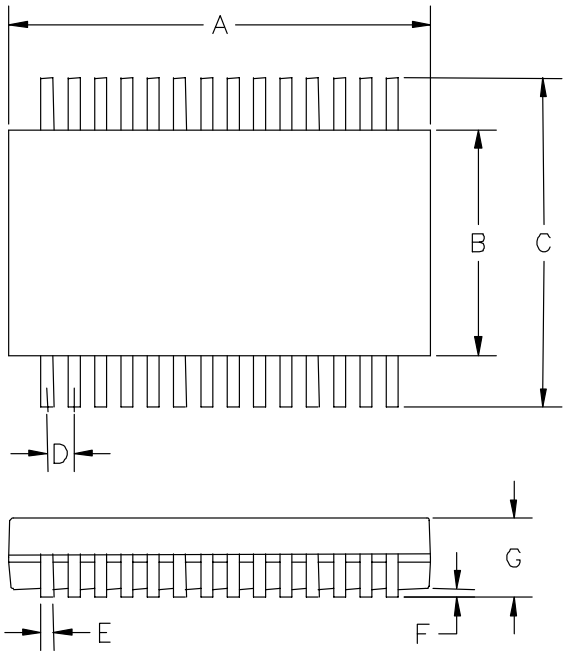
OUTLINE DRAWING - SSOP-28



DIMENSIONS					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.390	.413	9.90	10.50	
B	.197	.221	5.00	5.60	
C	.291	.323	7.40	8.20	—
D	.026 BSC		.65 BSC		—
E	.009	.015	.22	.38	—
F	.002	.008	.05	.20	—
G	.068	.078	1.73	2.00	—
J	.004	.010	.09	.25	—
K	0°	8°	0°	8°	—
L	.022	.037	.55	.95	—

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Ref. MO-150AH

ECN00-1004