



1-W High-Voltage Switchmode Regulator

FEATURES

- CCITT Compatible
- Current-Mode Control
- Low Power Consumption (less than 5 mW)
- 10- to 120-V Input Range
- 200-V, 250-mA MOSFET
- Internal Start-Up Circuit
- SHUTDOWN and RESET
- Maximum Duty Cycle of 99.9%

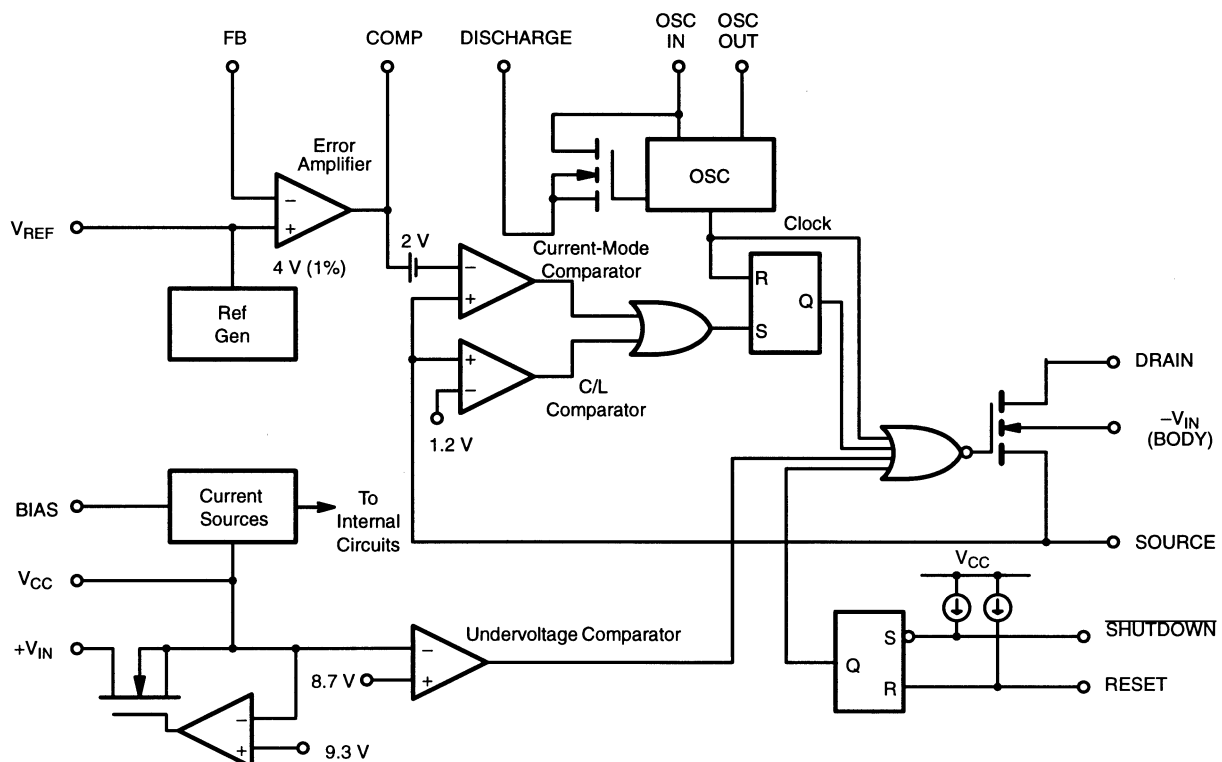
DESCRIPTION

The Si9108 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc/dc converter in ISDN terminals up to 3 watts. A 0.5-mA max supply current makes possible the design of a dc/dc converter with 60% efficiency at 25 mW, therefore meeting the recommended performance under the CCITT I.430 specifications.

This device may be used with an appropriate transformer to implement isolated flyback power converter topologies to provide single or multiple regulated dc outputs (i.e., ± 5 V).

The Si9108 is available in 16-pin wide-body SOIC, 14-pin plastic DIP, and 20-pin PLCC packages, and is specified over the industrial, D suffix (-40 to 85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)

V_{CC}	15 V
$+V_{IN}$	120 V
V_{DS}	200 V
I_D (Peak) (300 μ s pulse, 2% duty cycle)	2 A
I_D (rms)	250 mA
Logic Inputs (RESET, SHUTDOWN, OSC IN) ..	-0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SOURCE)	-0.3 V to 7 V
HV Pre-Regulator Input Current (continuous)	5 mA
Storage Temperature	-65 to 125°C
Operating Temperature	-40 to 85°C
Junction Temperature (T_J)	150°C

Power Dissipation (Package)^a

14-Pin Plastic DIP (J Suffix) ^b	750 mW
16-Pin Plastic Wide-Body SOIC (W Suffix) ^c	900 mW
20-Pin PLCC (N Suffix) ^d	1400 mW
Thermal Impedance (Θ_{JA})	
14-Pin Plastic DIP	167°C/W
16-Pin Plastic Wide-Body SOIC	140°C/W
20-Pin PLCC	90°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 6 mW/°C above 25°C

c. Derate 7.2 mW/°C above 25°C

d. Derate 11.2 mW/°C above 25°C

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$

V_{CC}	10 V to 13.5 V	R_{OSC}	25 k Ω to 1 M Ω
$+V_{IN}$	10 V to 120 V	Linear Inputs	0 to $V_{CC} - 3$ V
f_{OSC}	40 kHz to 1 MHz	Digital Inputs	0 to V_{CC}

SPECIFICATIONS^a

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = -V _{IN} = 0 V V _{CC} = 10 V, +V _{IN} = 48 V R _{BIAS} = 820 kΩ, R _{OSC} = 910 kΩ	Limits D-Suffix, -40°C to 85°C				Unit
			Temp ^b	Min ^c	Typ ^d	Max ^c	
Reference							
Output Voltage	V _R	OSC IN = V _{IN} (OSC Disabled) R _L = 10 MΩ	Room	3.92	4.00	4.08	V
Output Impedance ^e	Z _{OUT}	OSC IN = -V _{IN}	Room	15	300	45	kΩ
Short Circuit Current	I _{SREF}	OSC IN = - V _{IN} , V _{REF} = -V _{IN}	Room	70	100	130	μA
Temperature Stability ^e	T _{REF}	OSC IN = -V _{IN}	Full		0.25	1.0	mV/°C
Long Term Stability ^e		t = 1000 hrs, T _A = 125°C	Room		5.00	25.00	mV
Oscillator							
Maximum Frequency ^e	f _{MAX}	R _{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f _{OSC}	See Note e	Room	32	40	48	kHz
Voltage Stability	Δf/f	Δf/f = f (13.5 V) - f (9.5 V)/f (9.5 V)	Room		10	15	%
Temperature Coefficient ^e	T _{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V _{FB}	FB Tied to COMP OSC IN = -V _{IN} (OSC Disabled)	Room	3.96	4	4.04	V
Input BIAS Current	I _{FB}	OSC IN = -V _{IN} , V _{FB} = 4 V	Room		25	500	nA
Open Loop Voltage Gain ^e	A _{VOL}	OSC IN = -V _{IN} (OSC Disabled)	Room	60	80		dB
Input Offset Voltage	V _{OS}	OSC IN = -V _{IN}	Room		±15	±40	mV
Unity Gain Bandwidth ^e	BW		Room	0.5	0.8		MHz
Dynamic Output Impedance	Z _{OUT}		Room		1		kΩ
Output Current	I _{OUT}	Source (V _{FB} = 3.4 V)	Room		-1.2	-0.32	mA
		Sink (V _{FB} = 4.5 V)	Room	0.05	0.08		
Power Supply Rejection	PSRR	10 V ≤ V _{CC} ≤ 13.5 V	Room		70		dB



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			Temp ^b	Min ^c	Typ ^d	Max ^c	
PWM							
Maximum Duty Cycle	D _{MAX}		Room	99.0	99.6	99.9	%
Dead Time			Room		100		ns
Minimum Duty Cycle	D _{MIN}		Room			0	%
Minimum Pulse Width Before Pulse Drops Out			Room		110	175	ns
Current Limit							
Threshold Voltage	V _{SOURCE}	R _L = 100 Ω from DRAIN to V _{CC} V _{FB} = 0 V	Room	0.8	1.0	1.2	V
Delay to Output ^e	t _d	R _L = 100 Ω from DRAIN to V _{CC} V _{SOURCE} = 1.5 V, See Figure 1	Room		200	300	ns
Input Voltage	+V _{IN}	I _{IN} = 10 μA	Room	120			V
Input Leakage Current	+I _{IN}	V _{CC} ≥ 10 V	Room			10	μA
Pre-Regulator Start-Up Current	I _{START}	Pulse Width ≤ 300 μs, V _{CC} = 7 V	Room	8	15		mA
V _{CC} Pre-Regulator Turn-Off Threshold Voltage	V _{REG}	I _{PRE-REGULATOR} = 10 μA	Room	7.5	9.3	9.7	V
Undervoltage Lockout	V _{UVLO}	R _L = 100 Ω from DRAIN to V _{CC} See Detailed Description	Room	7.0	8.7	9.2	
V _{REG} - V _{UVLO}	V _{DELTA}		Room	0.25	0.5		
Supply							
Supply Current	I _{CC}		Room		0.35	0.5	mA
Bias Current	I _{BIAS}		Room		7.5		μA
SHUTDOWN Delay	t _{SD}	V _{SOURCE} = -V _{IN} , See Figure 2	Room		50	100	ns
SHUTDOWN Pulse Width	t _{SW}	See Figure 3	Room	50			
RESET Pulse Width	t _{RW}		Room	50			
Latching Pulse Width SHUTDOWN and RESET Low	t _{LW}		Room	25			
Input Low Voltage	V _{IL}		Room			2.0	V
Input High Voltage	V _{IH}		Room	8.0			
Input Current Input Voltage High	I _{IH}	V _{IN} = 10 V	Room		1	5	μA
Input Current Input Voltage Low	I _{IL}	V _{IN} = 0 V	Room	-35	-25		



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			Temp ^b	Min ^c	Typ ^d	Max ^c	
MOSFET Switch							
Breakdown Voltage	V _{(BR)DSS}	I _{DRAIN} = 100 μA	Full	200	220		V
Drain-Source On Resistance ^g	r _{DS(on)}	I _{DRAIN} = 100 mA	Room		5	7	W
Drain Off Leakage Current	I _{DSS}	V _{DRAIN} = 100 V	Room			10	μA
Drain Capacitance	C _{DS}		Room		35		pF

Notes

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Guaranteed by design, not subject to production test.
- f. C_{STRAY} Pin 8 = ≤ 5 pF
- g. Temperature coefficient of r_{DS(on)} is 0.75% per °C, typical.

TIMING WAVEFORMS

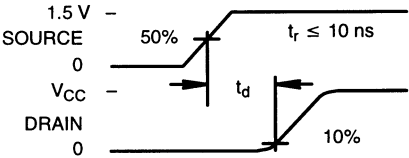


FIGURE 1.

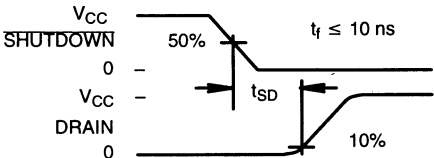


FIGURE 2.

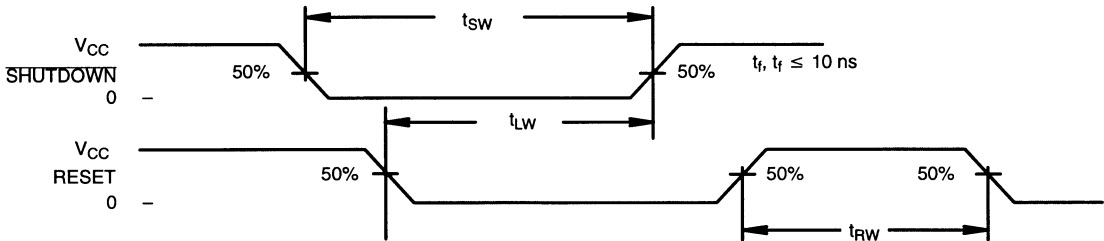


FIGURE 3.



TYPICAL CHARACTERISTICS

Output Switching Frequency vs. Oscillator Resistance

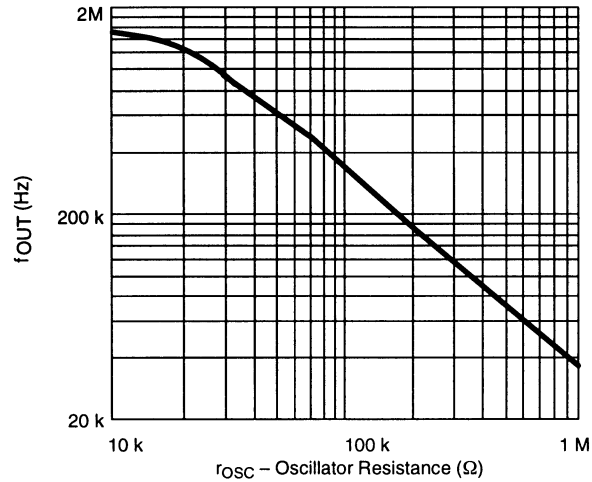
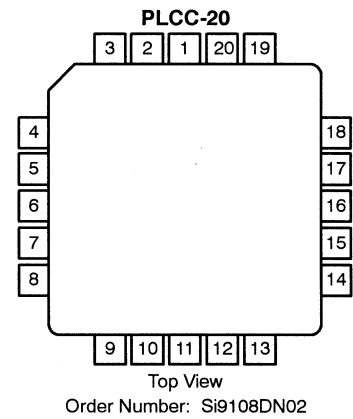
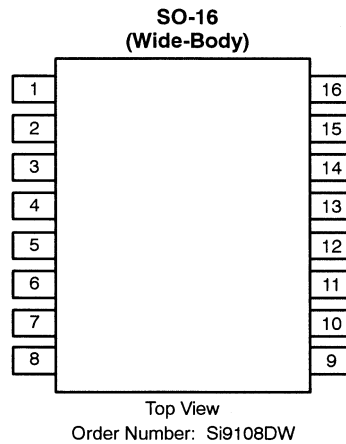
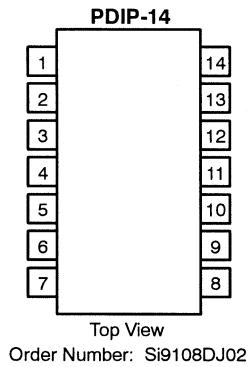


FIGURE 4.

PIN CONFIGURATIONS



PIN DESCRIPTION			
Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
-V _{IN}	5	2	8
V _{CC}	6	4	9
OSC _{OUT}	7	5	10
OSC _{IN}	8	6	11
DISCHARGE	9	7	12
V _{REF}	10	8	14
SHUTDOWN	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
+V _{IN}	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19