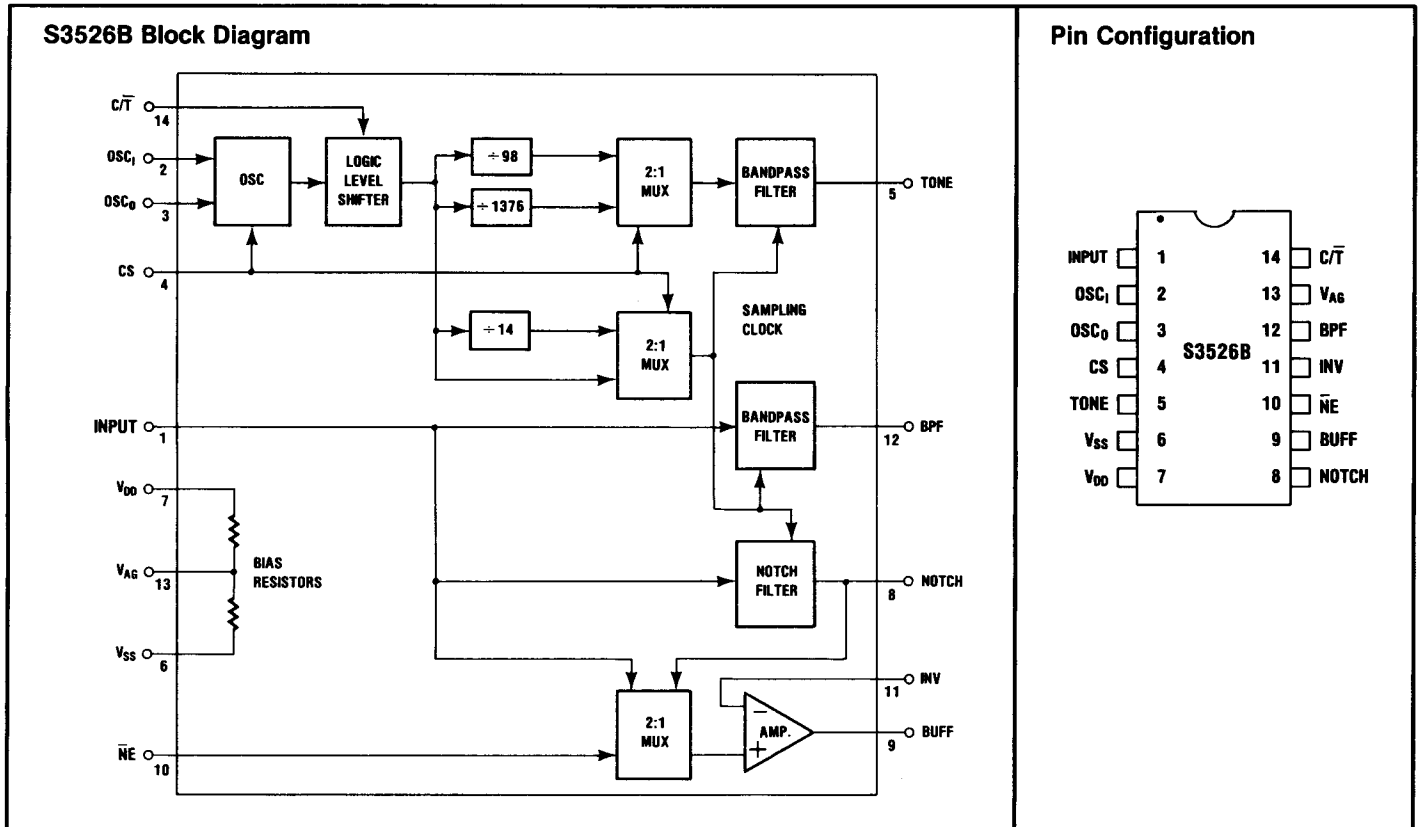February 1993   **Single Frequency Tuneable Bandpass/Notch Filter/Tone Generator**

Features

- Center Frequency of Filters Match and Track Frequency of Generated Tone
- Tone Frequency Adjustable Over a 100Hz to 5kHz Range
- Unfiltered Input, Input with Notched Tone, Input Tone and Tone Generator Outputs
- Operation from a Crystal or External CMOS/TTL Clock
- Operation at 2600Hz from a Low Cost 3.58MHz TV Color Burst Crystal or 256kHz Ext. Clock
- Buffered Output Drives 600Ω Loads
- Single or Split Supply Operation
- Low Power CMOS Technology

General Description

The S3526B is a low power CMOS Circuit which may be used in a variety of single frequency (SF) communication applications such as SF-Tone Receivers, Tone Remote Control in Mobile systems, Loopback Diagnostics in Modems, control of Echo Cancellers, dialing and privacy functions in Common Carrier Radio Telephone, etc. The main functional blocks of the S3526B include a low distortion tone (sinewave) generator whose frequency may be programmed using a crystal (i.e. 2600Hz using a low cost TV color burst crystal) or external clock time base; a bandpass filter used to extract tone information from the input signal; a band reject filter which is used to "Notch" out tone information from the input signal; and a buffer amplifier with selectable input (unfiltered input signal, or input signal with tone notched) capable of driving a 600Ω load.

S3526B Block Diagram

Pin Configuration

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Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$) .... $+ 15.0V$

Operating Temperature .... $0°C$ to $+ 70°C$

Storage Temperature .... $-65°C$ to $+150°C$

Input Voltage, All Pins .... $V_{SS} - 0.3V < V_{IN} < V_{DD} + 0.3V$

D.C. Electrical Operating Characterisitcs: $T_A = 0°C$ to $+ 70°C$, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation (Maximum @13.5V)		100	275	mW
R_{IN}	Input Resistances (Except Input)	8			MΩ
C_{IN}	Input Capacitances			15.0	pF

General Analog Signal Parameters: $T_A = 0°C$ to $+ 70°C$, $(V_{DD} - V_{SS}) = 10V$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Straight Through Gain (Measured at $-10dBm0$)	-0.1	0	0.1	dB
Z_{IN}	Input Impedance (Input, Pin 1)		2.5		MΩ
TLP	Transmission Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level ($+ 3dBm0$)		2.1		VRMS
R_L	Load Resistance (BPF, NOTCH)	10			kΩ
R_L	Load Resistance (BUFF)	600			ohms
V_{OSB}	Buffer Output Offset Voltage		± 50	± 150	mV
ICN_P	Idle Channel Noise in Pass Condition		2		dBrnC0
V_{OUT}	Output Signal Level into R_L for NOTCH, BPF, BUFF	2.0	2.1		VRMS
V_{OT}	Sine Wave (Tone) Output (Load = 10KΩ)		$0.6(V_{DD} - V_{SS}) \pm 0.5dB$		Vpk-pk
V_{TD}	Sine Wave Distortion ($f_{OSC} = 3.58MHz$) (See Figure 4)		-35		dB

Filter Performance Specifications

Band Pass Filter Characteristics $T_A = 0°C$ to $+ 70°C$, $(V_{DD} - V_{SS}) = 10V$, $f_{OSC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{FS}	Maximum Input Voltage ($+ 3dBm0$)		2.1		VRMS
A_{BP}	Passband Gain @ $-10dBm0$	-0.8	0	$+ 0.8$	dB
I_{CN}	Idle Channel Noise		24		dBrnC0
V_{OS}	Output Offset		± 50	± 150	mV
	* 2600Hz Bandpass Filter Response (referenced from 2600Hz, $+ 3dBm0$) (See Figures 1 and 2)				
	DC to 1600Hz		-80		dB
	2100Hz		-63	-50	dB
	2400Hz		-37	-30	dB
	2540Hz		-7.0	-3	dB
	2560Hz	-3	-1.8		dB
	2640Hz	-3	-1.0		dB
	2660Hz		-5.4	-3	dB
	2800Hz		-35	-30	dB
	3100Hz		-58	-50	dB
	3600Hz		-74		dB
DR	Dynamic Range (V_{FS} to ICN)		70		dB

*Delay from input to output is approximately 8mseconds.   38

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Notch Filter Characteristics: $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$ (Symmetrical Supplies), $f_{OSC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{FS}	Maximum Input Voltage ($+3dBm0$)		2.1		VRMS
A_{BR}	Passband Gain @ $-10dBm0$)	-0.5	0	$+0.5$	dB
ICN	Idle Channel Noise		18		dBrnC0
V_{OS}	Output Offset		±100	±225	mV
DR	Dynamic Range (V_{FS} to ICN)		75		dB
	2600Hz Notch Filter Response (referenced from 1000Hz, ($+3dBm0$) (See Figures 1 and 3)				
	250Hz to 2200Hz	-0.5	±0.1	0.5	dB
	2200Hz to 2400Hz	-5.0		0.5	dB
	2585Hz to 2615Hz		-70	-53	dB
	2800Hz to 3000Hz	-5.0		0.5	dB
	3000Hz to 3400Hz	-0.5	±0.1	0.5	dB

Digital Electrical Parameters $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$

Symbol	Mode Control Logic Levels	Min.	Typ.	Max.	Units
V_{IH}	C/T CMOS Operation (Pin 14)	$V_{DD} - 0.5$		V_{DD}	V
V_{IL}	C/T TTL Operation (Pin 14)	V_{SS}		$V_{DD} - 4$	V
V_{IH}	CS for Low Speed Clock Input	$V_{DD} - 0.5$		V_{DD}	V
V_{IL}	CS for Crystal or High Speed Clock	V_{SS}		V_{AG}	V

	CMOS Logic Levels				
V_{IH}	Input Voltage "1" Level	$V_{AG} + 2$		V_{DD}	V
V_{IL}	Input Voltage "0" Level	V_{SS}		$V_{AG} - 2$	V

Control Pin Definitions

Pin#	Name	Connection	Operation	Note
14	C/T	V_{DD} to $(V_{DD} - 0.5V)$	CMOS Logic Levels	1
		$(V_{DD} - 4V)$ to V_{SS}	TTL Logic Levels	
4	CS	V_{DD}	Ext. Low Speed Sq. Wave Clock @ Pin 3	2
		V_{SS} or V_{AG}	Crystal Connected Between Pins 2 and 3 or High Speed Clock to Pin 2	
10	NE	V_{DD} to .7 $(V_{DD} - V_{SS})$ 70%	Buffer Out = Input Signal	
		V_{SS} to .3 $(V_{DD} - V_{SS})$ 30%	Buffer Out = Notch Filter Out	

NOTES:
1) CMOS logic levels are same as V_{DD} and V_{SS} supply voltage levels. For TTL interface ground of TTL logic must be connected to V_{SS} supply pin.
2) For ext. low speed clock operation pin 2 is open. For ext. high speed clock, drive pin 2, leave pin 3 open.
3) The performance specifications are guaranteed with $\pm5\%$ power supplies for normal operation.

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Pin Function Description

Pin	No.	Function
Input	1	This pin is the analog input to the filters and the buffer. It is a high impedance input ($Z \cong 2.5M\Omega$).
OSC_I OSC_O	2 3	These pins are the timing control for the entire chip. A crystal may be connected across these two pins in parallel with a $10M\Omega$ resistor. Another option is to provide an ext clock at pin 3 and leave pin 2 to open. TTL or CMOS may be used. As a third choice, a CMOS level external clock may be applied to pin 2 directly leaving pin 3 open.
CS	4	Clock Select-This pin when tied to V_{DD} configures the chip to operate from a low speed clock. When tied to V_{AG} or V_{SS} the chip operates from external crystal or high speed clock.
TONE	5	This is an output pin providing a sine wave with a frequency of fosc $\div$ 1376 if CS is low or fosc $\div$ 98 if CS is high.
V_{SS}	6	Negative supply voltage pin. Typically $-5V \pm 5\%$
V_{DD}	7	Positive supply voltage pin. Typically $+5V \pm 5\%$.
NOTCH	8	Band Reject (Notch) Filter-This is the output of the filter that notches the tone information from the input signal. It is capable of driving a load $\geqslant 10k\Omega$.
BUFF	9	Buffer Output-The buffer is capable of driving a 600Ω load and provides from its output either the signal input without filtering, or the signal input with the tone frequency notched out.
NE	10	Notch Enable-This pin controls which signal is presented to the buffer input. A logic high (V_{DD}) connects the input signal. A logic low (V_{SS}) connects the output of the band reject (notch) filter.
INV	11	Inverting-This is the inverting input of the buffer.
BPF	12	Band Pass Filter-This is the output of the band pass filter which will pass any energy at the tone frequency present in the input signal. It is capable of driving a load $\geqslant 10k\Omega$.
V_{AG}	13	Analog Ground-This is the analog ground pin. When used with a single supply, this pin is $\frac{1}{2}$ ($V_{DD} - V_{SS}$) $\pm 100mV$. When used with $\pm 5V$ supplies, this point is at ground. The S3526 has internal voltage divider resistors to V_{DD} and V_{SS} of $\cong 20k\Omega$.
C/T	14	CMOS/TTL-This pin determines whether CMOS or TTL levels will be accepted at pin 3 for a clock input. When tied to V_{DD}, the chip accepts CMOS logic levels. When tied to a point $\leqslant (V_{DD} - 4V)$, the chip accepts TTL levels referenced to V_{SS}. For crystal operation pin 14 should be at V_{DD}.

Application Information

The S3526B device is a very versatile filter chip. Although it was designed for the telephone market SF signaling application when used with the commonly available TV colorburst crystal, it will work over a wide range of frequencies. Typically, it will cover from 100Hz to 5kHz providing coverage of the entire voice band for in-band signaling.

Because it is a very high Q filter the transient response time must be considered when determining the maximum data rate for a particular frequency. This response is illustrated in Figure 5 and shows that it is quite adequate for 10 pulse-per-second (50% duty cycle) data rate at 2600Hz. But the same data rate could not be used at 500Hz, for example, as a detector could not differentiate between tone on and tone off conditions.

Figure 1. Typical Filter Performance Curves at 2600Hz

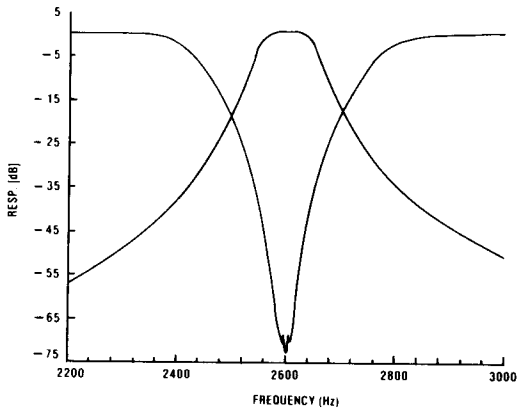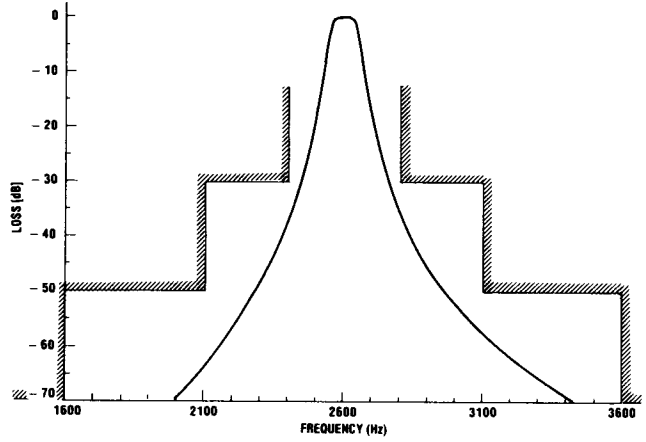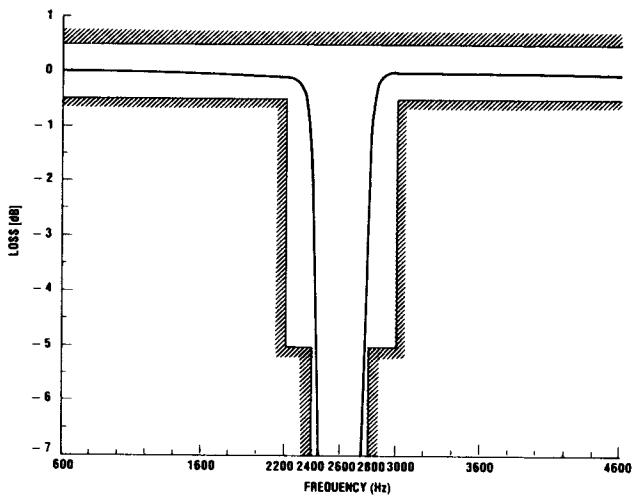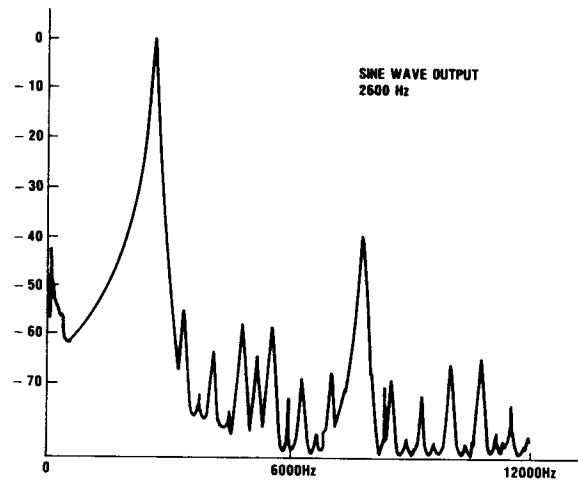**Figure 2. Typical Bandpass Response**

Figure 3. Typical Notch Response

Figure 4. Typical Sine Wave Output Spectrum from Pin 5

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Figure 5. Typical Delay Characteristics at + 3dBmO with 2600Hz Pulsed at 10pps with 50% Duty Cycle

Figure 6. Typical Filter Performance Curves at 1000Hz
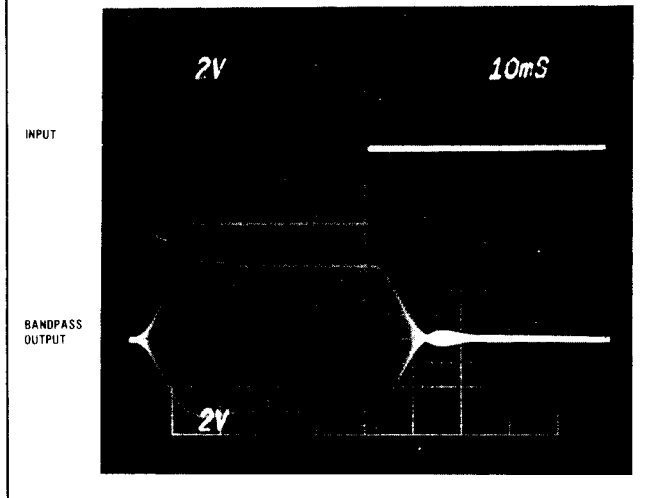
The combination of tone generator, notch filter, and bandpass filter allows one to generate a signaling tone at the sending end and notch it out at the receiving end, as well as detect it through the bandpass filter. For reliable detection the output of the bandpass filter can be compared with the output of the bandreject filter. If the output of the BR filter is within a fixed ratio of the BP filter (such as 10dB) then the signal present may be considered voice rather than signaling and ignored.
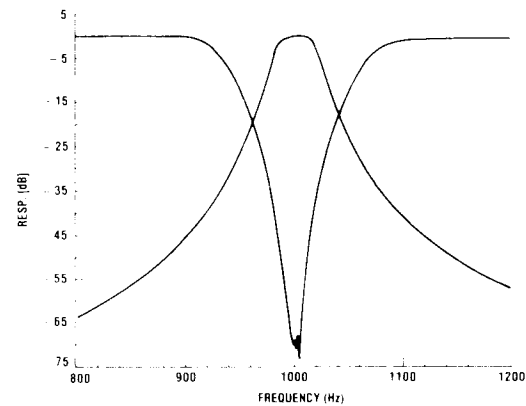
In situations where the entire voice band is desired except during signaling the buffer output can be switched straight through to the input. When the output of the filters indicates that a signaling tone is present, the NE pin can be switched low, switching the notch filter into the signal path to prevent the tone from reaching the listener or from being passed further down the system to another signaling receiver.

By using the notch filter with telephone accessories it can be guaranteed that the accessory will not violate the telephone company specifications about transmitting 2600Hz into the lines, causing disconnected calls.

Power Supplies

The S3526B will work with either single or dual power supplies. When used with dual power supplies ($\pm$ 5V) the analog inputs and outputs will be referenced to ground. If an external clock signal is provided, rather

than using a crystal, it must be swinging from V_{SS} to V_{AG} for TTL swings or from V_{SS} to V_{DD} for CMOS swings. If this is not convenient the signal can be capacitively coupled into pin 3 as illustrated in Figure 7. In the dual supply mode, the power supplies should track or maintain close tolerances for maximum accuracy. If the supplies should skew, the filter characteristics will change very slightly and in most applications, will have no effect at all but can be seen if the curves are plotted on high accuracy equipment.

When using the S3526B on a single power supply the analog inputs and outputs will be referenced to V_{AG} which is $\frac{1}{2}$ ($V_{DD} - V_{SS}$). This means that the analog signals may need to be capacitively coupled in and out if they are normally ground referenced. For example, the input may appear as in Figure 8. But when an external clock is used in the single supply situation it can be direct coupled TTL levels referenced to ground.

Selecting Clocking Sources

The switched capacitor filter design allows the S3526B to be easily tuned by varying the clock frequency. This makes it useful for many applications in telephone signaling, data communications, medical telemetry, test equipment, automatic slide projectors, etc. The necessary clock frequency can be determined by multiplying the desired center frequency by 1376. This frequency

can then be provided from a crystal, an external clock, or a rate multiplier chip. With Clock Select (CS), pin 4 tied low the TONE, pin 5, will provide the desired frequency and the filters will be centered around that frequency. There are many common, low cost microprocessor frequency crystals available that might be very close to a desired frequency. Table 1 illustrates some possible application frequencies. For example, by using a standard 3.00MHz crystal the 2175Hz tone would be 2180Hz or .23% high.

If it is desired to use a lower frequency clock and precision tone generation is not required the external clock can be determined by multiplying the center frequency by 98.4, and tying Clock Select (CS) pin 4 high. Note that the TONE, pin, 5, is not accurate in this situation, being .41% higher than the filter center frequency, although it will fall well within the passband of both filters and be perfectly usable.
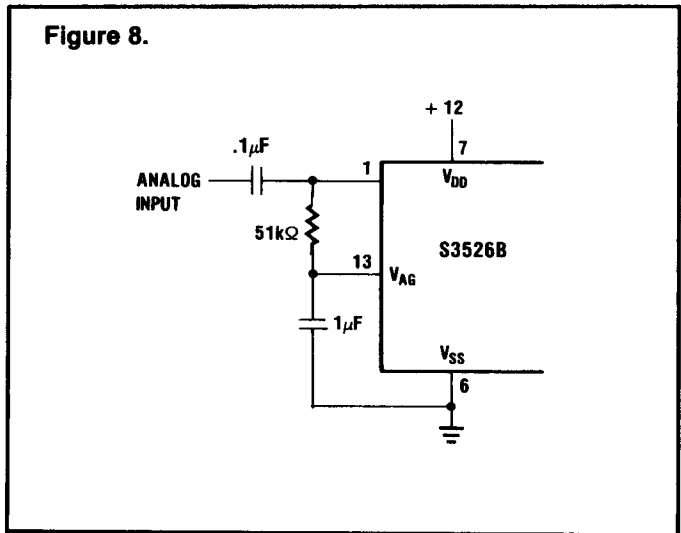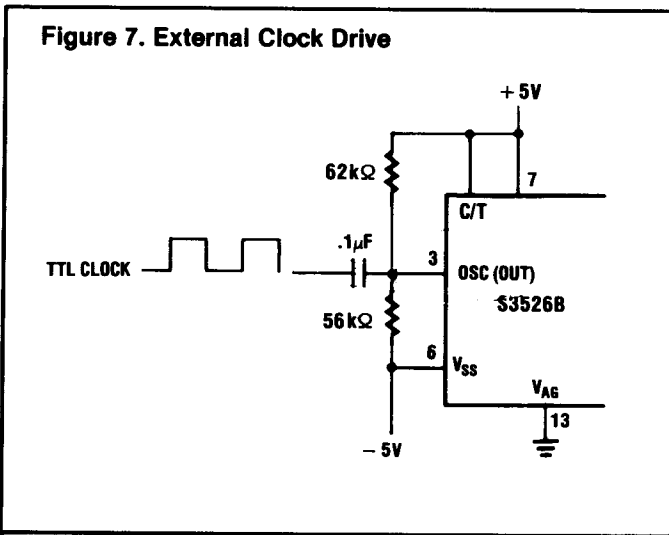

Figure 7. External Clock Drive

Figure 8.

Table 1. Tone and Clock Frequencies for Various Applications

Tone In Hertz	Application	CS = 0 XTAL or HIGH Freq. Clock (MHz)	CS = 1 Ext. Clock Input (Low Freq.) (Hz)
550	Guard Tone-Data Comm	.756800	54,120
1000	Test Tone	1.376000	98,400
1020	Test Tone	1.403520	100,368
1400	Medical Telemetry	1.926400	137,760
1600	SF Signaling—Military	2.201600	157,440
1800	Guard Tone-Data Comm	2.476800	177,120
1850	Pilot Tone-Radio	2.545600	182,040
1950	Pilot Tone-Radio	2.683200	191,880
2125	Echo Suppressor Disable	2.924000	209,100
2150	Echo Suppressor Disable	2.958400	211,560
2175	Guard Tone-Radio	2.992800	214,020
2280	SF Signaling-Telephone	3.137280	224,352
2400	SF Signaling-Telephone	3.302400	236,160
2600	SF Signaling-Telephone	3.579545	256,000
2713	Loopback Tone-Datacom	3.733088	266,959
2800	SF Signaling-Telephone	3.852800	275,520
2805	Signaling Tone-Radio	3.859680	276,012
3825	SF Signaling-European	5.263200	376,380