- **Fully Integrated SONET/SDH Transceiver Supporting Clock/Data Recovery and MUX/DEMUX Functions**
- **Compliant With OIF-VSR4-03.0 (Former OIF2000.074.4 and OIF2001.284) Supporting SONET/SDH OC-192 Data Over Four Fibers**
- **Compliant With OIF-SFI4-01.0 Electrical Interface (Former OIF99.102) Supporting 4x4 Bit or 1x16 Bit LVDS Electrical Interface**
- **Supports OC-48/STM16 and Forward Error Correction (FEC) Data Rates Up To 2.7 Gbps**
- **Selectable Transmit Only, Receiver Only, Transceiver and Repeater Functions**
- **Supports SONET/SDH Frame Detection**
- **On-Chip PRBS Generation and Verification (2^{31}–1 and 2^7–1)**
- **Dual Power Supply 1.8/3.3 V**
- **Interfaces to Back Plane, Copper Cables or Optical Modules**
- **Hot Plug Protection**
- **Supports Redundancy**
- **VML Serial Interface With Programmable Pre-Emphasis and Internal Termination + Biasing**
- **On-Chip Termination for LVDS and PECL Compatible Interfaces**
- **Receiver Differential Input Thresholds 150 mV PP Min**
- **Supports SONET Loop Timing**
- **Low Power (1.5 W) at OC-48 rate**
- **ESD Protection >2 kV**
- **155-MHz or 622-MHz Reference Clock**
- **Maintains Clock Output in Absence of Data**
- **Local and Remote Loopback**
- **Advanced 0.18-μm CMOS Technology**
- **Small Footprint (19x19 mm) 289-Ball PBGA Package**

PRODUCT PREVIEW

description

The SLK2504 is a single chip quad transceiver IC used to derive high-speed timing signals for SONET/SDH based equipment. The chip performs clock and data recovery, serial-to-parallel, parallel-to serial conversion and frame detection function conforming to the SONET/SDH standards on 4 separate channels.

A user selectable external reference clock operating at 622.08MHz or 155.52MHz is required for the recovery loop. The reference clock also provides a stable clock source in the absence of serial data transitions.

The SLK2504 accepts4 sets of 4-bit LVDS parallel data/clock and generates 4 NRZ SONET/SDH compliant signals at OC-48 rates. It also recovers the data and clock from serial SONET streams and de-multiplexes it into 4 sets of 4 bit LVDS parallel data for full duplex operation. The 4 serial channels have a low jitter Voltage Mode Logic (VML) differential interface. It is recommended to AC-couple the input of the receiver (see Figure 24).

The SLK2504 provides a comprehensive suite of built-in tests for self-test purposes including local and remote loopback and PRBS (2^7–1 and 2^{31}–1) generation and verification.

The device comes in a 289-pin PBGA package, requires a 1.8-V supply for the device core and a 3.3-V supply for the TTL control inputs. The SLK2504 is very power efficient dissipating less than 0.4-W per channel at 2.488 Gbps, the OC-48 data rate, and it is characterized for operation from –40°C to 85°C.

The four channel of the SLK2504 can be used as 4 independent OC-48 data lanes or can be configured as one OC-192 data lane fully compliant with OIF-VSR4-03.0.

In OC-192 mode, the transmitter receives a 16-bit 622Mbps LVDS electrical signal from the OC-192 framer chip, serializes the data and sends it to the high-speed serial side. The 4x2.488Gbps receiver input RXxP/N buffers data out of the optical receive stage. Each channel clock becomes recovered and the byte aligned before the data word is stored into the according FIFO. The SLK2504 meets or exceeds the Sonet jitter specification.

description (continued)

The SLK2504 offers 4 data channels (running independently or synchronized as OC-192) or can be configured as a two-port device with built in redundancy.

The SLK2504 meets the 3 SONET jitter specifications (jitter generation, jitter transfer, and jitter tolerance). However, the OIF-VSR4-03.0 as well as many backplane applications require a improved receiver jitter tolerance and are less critical to jitter transfer characteristics. The SLK2504 can be switched into a second mode with improved receiver jitter tolerance at the cost of Jitter transfer. This can be done by setting the VSR pin high.

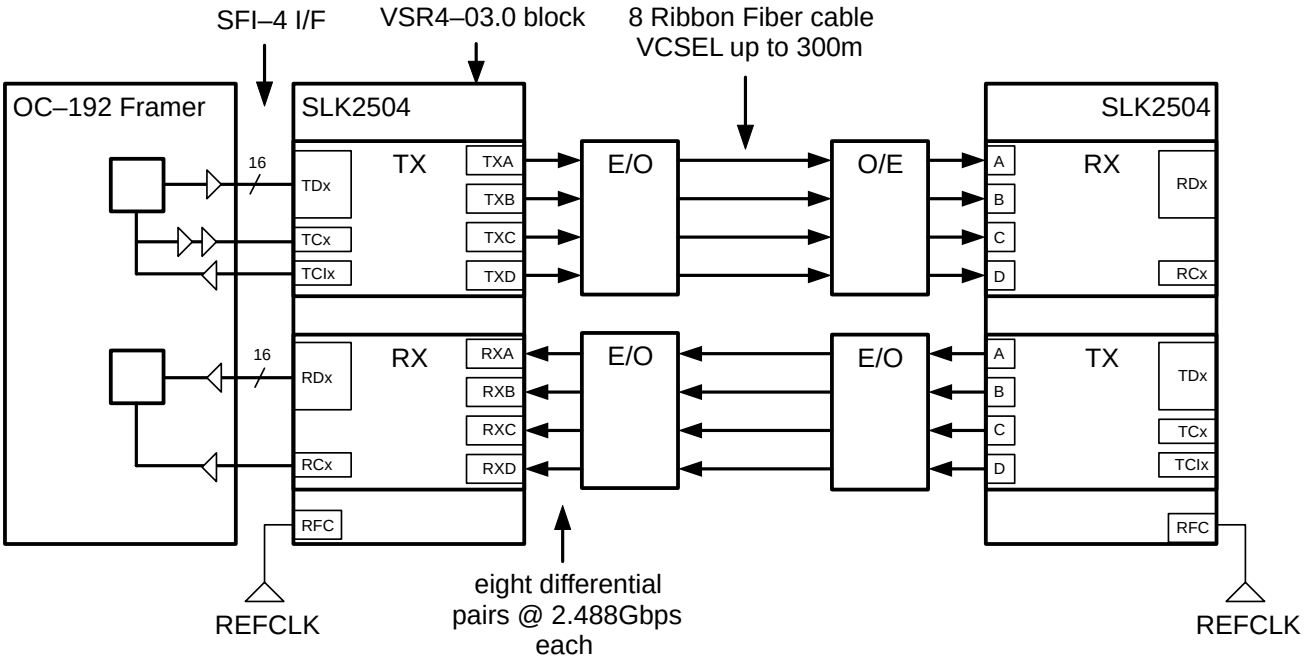

Figure 1. Typical VSR4-03.0 Set-Up Supporting OC-192/STM-64 Data Split Over Four 2.5-Gbps Links

The following block diagram provides a high-level description of the SLK2504. For a detailed diagram of the individual channels, please see Figure 3.

PRODUCT PREVIEW

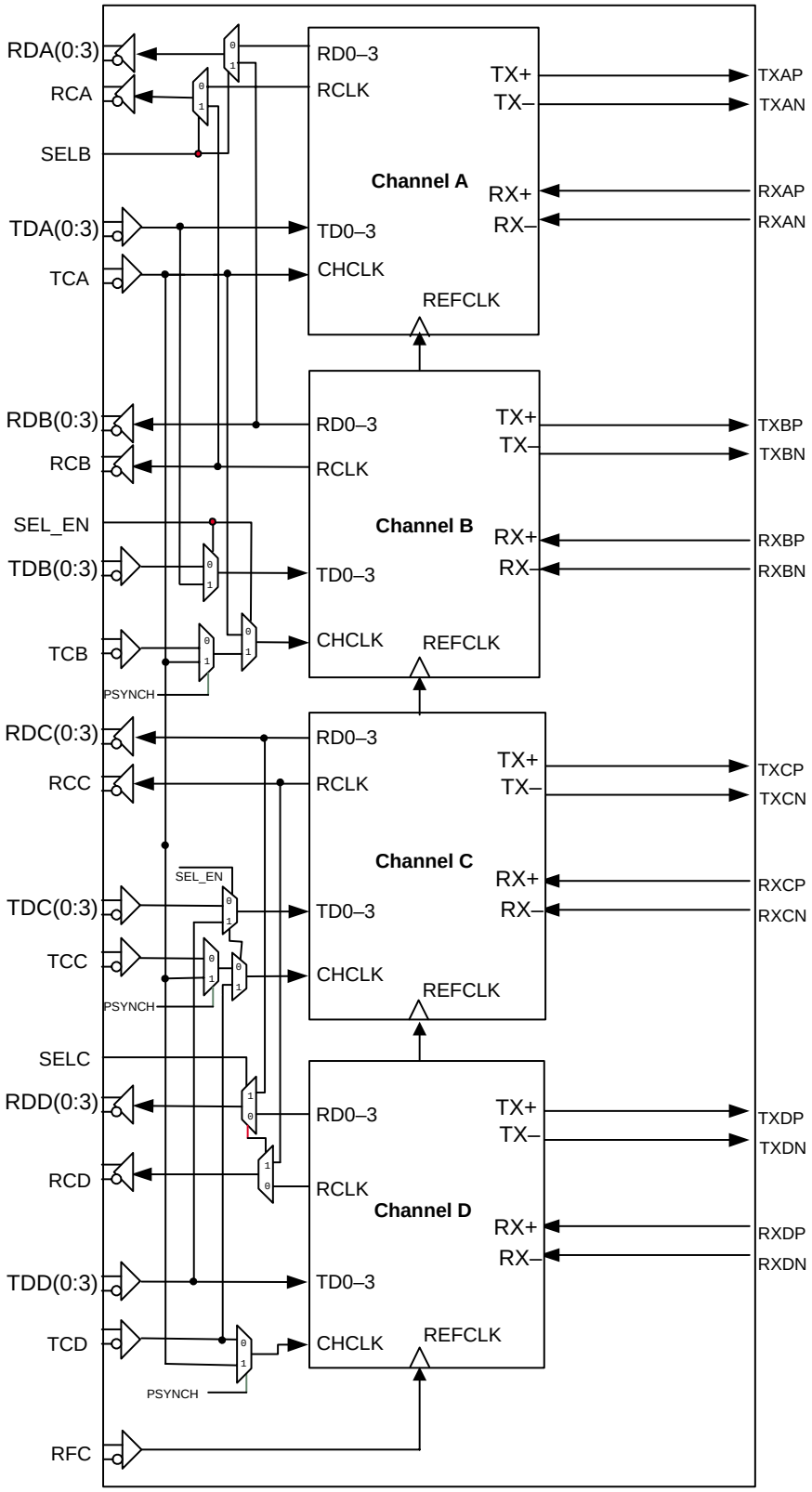

Figure 2. SLK2504 Block Diagram

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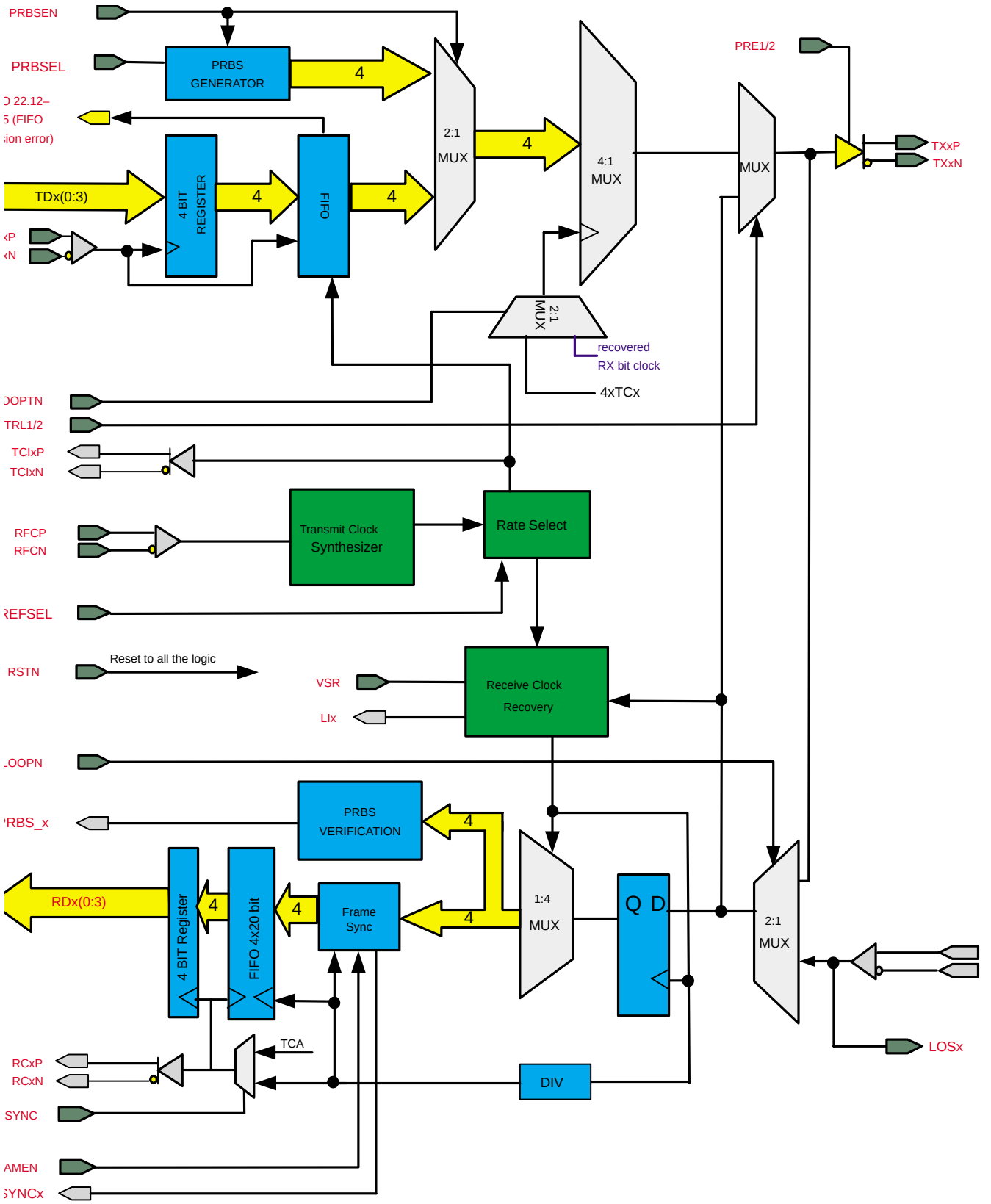

Figure 3. SLK2504 Block Diagram – One Channel

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