

SK70742

HDSL2 FEC/Framer

General Description

Level One's HDSL2 chip set provides synchronous full-duplex transmission over a single twisted pair. The SK70742 combines the functions of HDSL2 Frame Mapping and Forward Error Correction (FEC) in a single device. The IC interfaces directly to the SK70741 transceiver to provide line rates up to 2.064 Mbps over a single twisted pair cable. The device also supports fractional rates and provides a transparent framing mode.

Single stage Trellis Code Modulation (TCM) provides over 5 dB of coding gain when used with PAM 16 line code. Combined with the SK70741 transceiver, the framer is capable of recovering errors over a span of 150 symbols with less than 500 μ sec of overall loop latency at T1 line rates.

The SK70742 supports many programmable configurations that are selected with internal registers and accessed via the Motorola/Intel compatible 8-bit parallel interface.

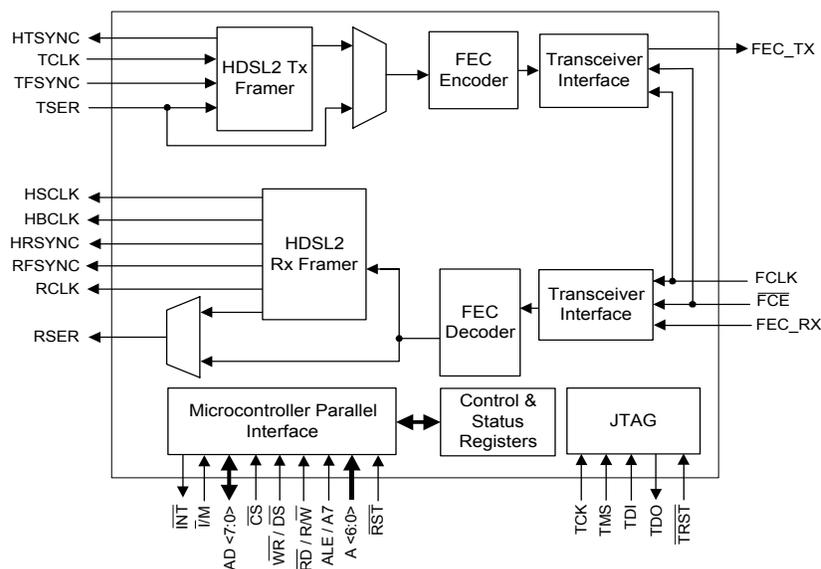
Applications

- Full rate and fractional T1/E1 transport systems
- Multichannel digital pair gain systems
- High Speed digital modems
- WAN access for LAN routers and switches

Features

- Meets requirements for ANSI T1E1.418
- HDSL2 Frame Mapping and Forward Error Correction
- Supports data rates from 144 to 2064 kbps
- Operates from a single 3.3 V supply
- 5 Volt tolerant input pins
- Data buffering and rate adaption between the T1 and HDSL2 line rate
- Less than 300 mW power consumption at 1.544 Mbps data rate
- Framer bypass mode and programmable FEC support non-standard applications
- 512 state TCM encoder and Viterbi decoder provides over 5 dB of coding gain
- Utilizes reference clock from SK70741 - no additional crystals or VCOs required
- Programmable for either central office (H2TU-C) or remote (H2TU-R) applications
- Parallel 8-bit microcontroller interface allows rapid set-up, acquisition and status monitoring
- 64-Pin QFP package

SK70742 Block Diagram



Refer to www.level1.com for most current information.

PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: Pin Assignments

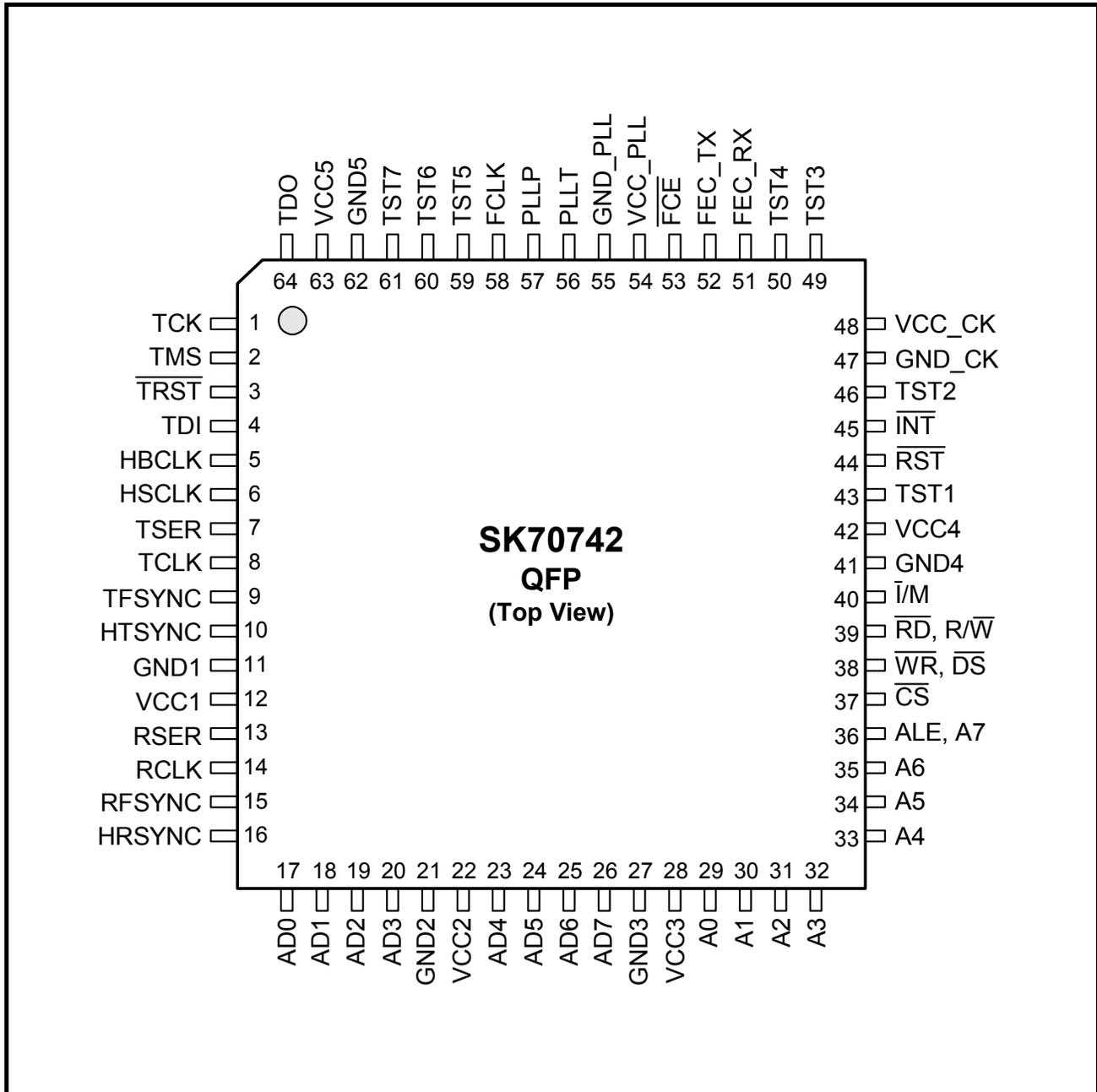


Table 1: SK70742 Signal Descriptions

Group	Pin #	Symbol	I/O ¹	Description
Power	12	VCC1	S	Logic Power Supply. +3.3 V ($\pm 5\%$).
	22	VCC2		
	28	VCC3		
	42	VCC4		
	63	VCC5		
	11	GND1	S	Ground for Logic Power. 0 V
	21	GND2		
27	GND3			
41	GND4			
62	GND5			
54	VCC_PLL	S	Phase Lock Loop Power Supply. +3.3 V ($\pm 5\%$). Connect to 3.3 V through a 49.9 Ω resistor with a 2.2 μ F capacitor between pin 54 and ground. See Application Note #110 for schematic.	
48	VCC_CK	S	Clock Power Supply. +3.3 V ($\pm 5\%$).	
47	GND_CK	S	Ground for Clock Power. 0 V	
55	GND_PLL	S	Ground for Phase Lock Loop Power. 0 V	
Misc.	44	$\overline{\text{RST}}$	DI	Reset. Pull Low to initialize internal circuits.
	56	PLLT	AO	Analog Tap for PLL Loop Filter. Connect a 10 nF capacitor in parallel with the series combination of 0.1 μ F and 576 Ω , between pins 56 and 57. See Application Note #110 for schematic.
	57	PLLP	AI	PLL Loop Filter Input. Connect a 10 nF capacitor in parallel with the series combination of 0.1 μ F and 576 Ω , between pins 56 and 57. See Application Note #110 for schematic.
Factory Test	43	TST1	–	Factory Test Pins. TST3-TST7 must not be externally connected. <i>TST1 and TST2 must be grounded.</i>
	46	TST2		
	49	TST3		
	50	TST4		
	59	TST5		
	60	TST6		
	61	TST7		
Transceiver Interface	53	$\overline{\text{FCE}}$	DI	FEC Chip Enable. Framing signal used to synchronize data transfer between the SK70741 and SK70742.
	51	FEC_RX	DI	Receive Data Input. Receive serial data from the SK70741. Sampled by the SK70742 on the rising edge of FCLK. FEC_RX is active when $\overline{\text{FCE}}$ is Low.
	52	FEC_TX	DO	Transmit Data Output. Serial encoded data is clocked into the SK70741 transmitter from the SK70742 on the rising edge of FCLK. FEC_TX is active when $\overline{\text{FCE}}$ is Low.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 1: SK70742 Signal Descriptions – continued

Group	Pin #	Symbol	I/O ¹	Description
Data Interface	7	TSER	DI	Transmit Serial Data. NRZ serial data clocked into the HDSL2 frame mapper. Data is latched on the falling edge of TCLK.
	9	TFSYNC	DI	Transmit Frame Synchronization Pulse. A Low-to-High transition indicates the start of a T1 frame. This input may be used to synchronize the HDSL2 frame to the T1 frame. Typically, the T1 and HDSL2 frames are not locked and this input is grounded.
	10	HTSYNC	DO	Transmit HDSL2 Frame Synchronization Pulse. A Low-to-High transition indicates the start of an outgoing HDSL2 frame.
	16	HRSYNC	DO	Receive HDSL2 Frame Synchronization Pulse. A Low-to-High transition indicates the start of an incoming HDSL2 frame.
	15	RFSYNC	DO	Receive Frame Synchronization Pulse. This signal goes High for one RCLK cycle every 193 RCLK cycles. When the transmit framer at the far end has synchronized the HDSL2 and T1 frames, a Low-to-High transition of this signal indicates the start of a T1 receive frame.
	13	RSER	DO	Receive Serial Data. Receive NRZ serial data from the HDSL2 frame mapper. RSER is valid on the falling edge of RCLK.
Clock and Control	8	TCLK	DI	Transmit Clock. Transmit clock signal from an external T1 framer or line interface IC. TSER is sampled on the falling edge of TCLK.
	14	RCLK	DO	Receive Clock. Receive bit clock generated by the HDSL2 frame mapper PLL. RSER is valid on the falling edge of RCLK.
	58	FCLK	DI	FEC Clock. Reference clock from the SK70741 transceiver which synchronizes the exchange of data between the SK70741 and SK70742. FCLK is 33 times the HDSL2 symbol rate.
	5	HBCLK	DO	HDSL2 Bit Clock. Bit clock for use when the HDSL2 framer mapper is bypassed. In this mode, TSER is latched on the falling edge of HBCLK and RSER is valid on the falling edge of HBCLK.
	6	HSCLK	DO	HDSL2 Symbol Clock. Used when the HDSL2 frame mapper is bypassed. This signal is Low for the first bit of every 3-bit symbol.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 1: SK70742 Signal Descriptions – continued

Group	Pin #	Symbol	I/O ¹	Description		
Parallel Processor Interface	26	AD7	DI/O	Multiplexed Data/Address Bus in Intel mode. Data Bus in Motorola mode.		
	25	AD6				
	24	AD5				
	23	AD4				
	20	AD3				
	19	AD2				
	18	AD1				
	17	AD0				
	36	ALE, A7			DI	Address Latch Enable. In Intel mode, the falling edge latches the address present on the multiplexed address/data bus. Address 7. In Motorola mode, this pin is address 7.
	35	A6			DI	Address Bus in Motorola mode. <i>In Intel mode, A0 and A2 must be grounded to disable a factory test mode and allow normal operation.</i>
34	A5					
33	A4					
32	A3					
31	A2					
30	A1					
29	A0					
45	$\overline{\text{INT}}$	DO	Interrupt. Open drain output asserted Low during an interrupt. Requires an external 10 k Ω pull up resistor.			
37	$\overline{\text{CS}}$	DI	Chip Select. Assert Low to read or write the SK70742 registers.			
38	$\overline{\text{WR}}, \overline{\text{DS}}$	DI	Write Pulse. Active Low write enable in Intel mode. Data Strobe. Active Low data strobe in Motorola mode.			
39	$\overline{\text{RD}}, \text{R}/\overline{\text{W}}$	DI	Read Pulse. Active Low read enable in Intel mode. Read-Write. Read/ $\overline{\text{Write}}$ select in Motorola mode.			
40	$\overline{\text{I}}/\text{M}$	DI	Intel / Motorola Select. When Low, the microcontroller interface is configured for Intel mode to support the 80C51 device. When High, the microcontroller interface configured for Motorola mode to support the 68000 device.			
JTAG Test	4	TDI	DI	Test Data Input. Used for loading serial instructions and data into internal test logic. Sampled on rising edge of TCLK. TDI is pulled up internally and may be left disconnected.		
	2	TMS	DI	Test Mode Select. Used to control the test logic state machine. Sampled on rising edge of TCLK. TMS is pulled up internally and may be left disconnected.		
	64	TDO	DO	Test Data Output. Three state output used for reading all serial configuration and test data from internal test logic. Updated on falling edge of TCLK.		
	1	TCK	DI	Test Data Clock. Synchronizes internal test logic operations.		
	3	$\overline{\text{TRST}}$	DI	JTAG Test Reset. Resets internal test logic operations. $\overline{\text{TRST}}$ is pulled up internally and must be pulled Low to disable JTAG.		
1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.						

FUNCTIONAL DESCRIPTION

The SK70742 is used in conjunction with the SK70741 and SK70740 to provide a complete HDSL2 physical layer interface. The device is programmable to support payloads of $N \times 64 + 8$ kbps or $N \times 64$ kbps with HDSL2 framing and overhead. Note that these are referred to as framed modes because the SK70742 adds HDSL2 framing and overhead, *not* because of any framing present in the payload data. The SK70742 framer may be disabled to configure the chipset as a transparent data pump with forward error correction. The SK70742 interfaces with industry standard T1/E1 framers and line interface ICs.

Data Interface

The SK70742 digital data interface consists of three input and three output signals whose functionality depends upon the operating mode. The interface signals and relative timing in each of these modes is described below.

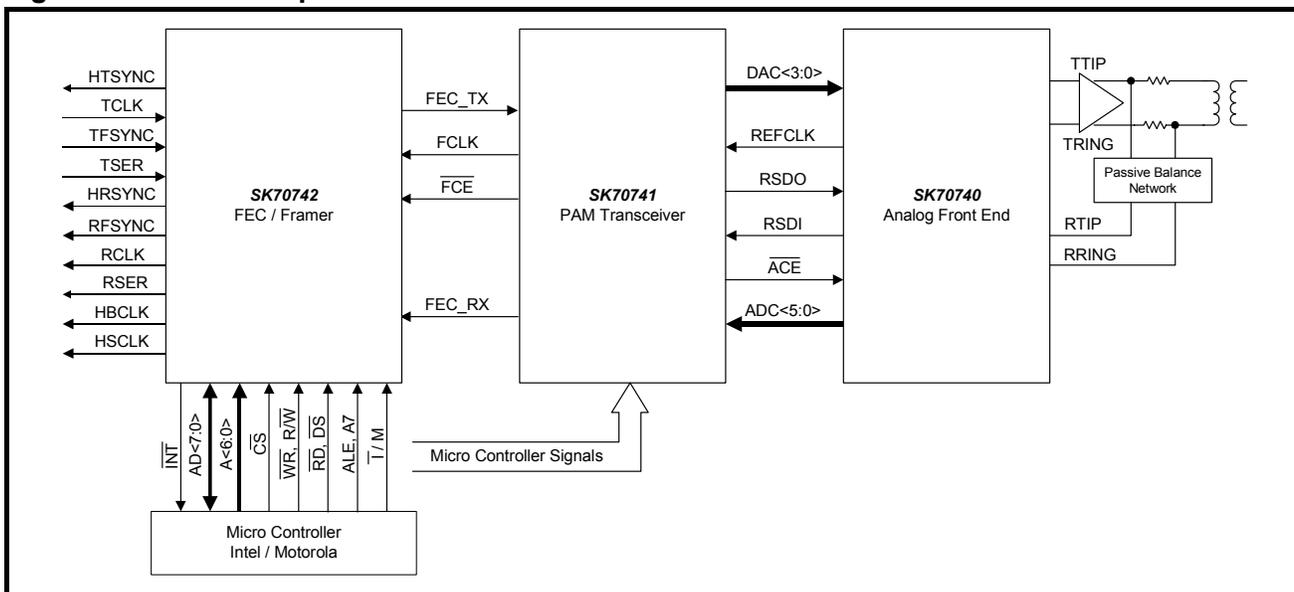
$N \times 64 + 8$ kbps (T1) Framed Mode Signals

For T1 HDSL2 transport, the SK70742 is configured for an $N \times 64 + 8$ kbps payload with 8 kbps of HDSL2 framing and overhead. In this configuration, the SK70742 may be connected to a T1 line interface IC or a T1 framer.

In the transmit direction, NRZ data and a 1.544 MHz clock from the T1 framer or line interface receiver should be externally provided on the TSER and TCLK inputs. TSER is internally latched on the falling edge of TCLK. In applications with a T1 framer, the framer receive frame sync output may be connected to the SK70742 TFSYNC input. Normally the HDSL2 and T1 frames are not aligned. However, if TFSYNC is supplied, it is possible to slave the HDSL2 transmit frame alignment to the T1 alignment under software control. This capability is not required for ANSI T1E1.418 compliant T1 transport, so TFSYNC may instead be grounded.

In the receive direction, the SK70742 generates a 1.544 MHz recovered clock (RCLK) and a serial NRZ data signal (RSER) that should be connected to the transmit clock and data inputs of a T1 framer or line interface IC. Data is clocked out on RSER at each rising edge of RCLK, and should be externally sampled on the falling edge. In most applications, the HDSL2 and T1 frames are not aligned at the transmitter, so the SK70742 T1 receive frame sync output (RFSYNC) conveys no useful information and may be left unconnected (unless the T1 framer requires it). In applications where the HDSL2 and T1 frames are aligned at the transmitter, the SK70742 RFSYNC may be connected to the T1 framer transmit frame sync input to allow the outgoing T1 frame alignment to be set from the HDSL2 receive frame sync. Figure 3 illustrates the signal timing in this mode.

Figure 2: HDSL2 Chip Set Overview



N x 64 kbps Framed Mode Signals

For applications other than T1 HDSL2 transport, the SK70742 framer is typically configured for an N x 64 kbps payload. In this mode, the payload data is combined with 8 kbps of HDSL2 framing and overhead, plus another 8 kbps of user defined overhead. The interface signals operate the same as in the T1 transport mode, except the payload rate is 8 kbps slower since the T1 “F-bit” is not used. The SK70742 TSER and TCLK inputs must be supplied with data and clock at the N x 64 kbps payload data rate. TSER is internally latched on the falling edge of TCLK. TFSYNC should be grounded in this mode. The SK70742 receiver PLL recovers the payload data rate clock which is output on RCLK. Receive data is clocked out on RSER each RCLK rising edge and should be externally sampled on the falling edge. RFSYNC should be left unconnected in this mode.

Framer Bypass Mode Signals

In transparent data pump applications, the chipset simply passes bits at the data interface without establishing a frame structure on the line. In this configuration, the SK70742 HDSL2 frame mapper is bypassed and only the Forward Error Correction (FEC) encoder and decoder are used. Each symbol period, the FEC maps three bits of payload data to and from a four-bit PAM-16 symbol on the line.

In Framer Bypass mode, the data interface consists of four signals: the HBCLK, HSCLK and RSER outputs and the TSER input. HBCLK is the bit clock output derived from the HDSL2 symbol clock (HSCLK). Every symbol period, HBCLK clocks in three bits of transmit data on TSER and clocks out three bits of receive data on RSER. TSER is latched on the falling edge of HBCLK and RSER is updated on the rising edge of HBCLK. HSCLK is Low for one HBCLK period during the first of every 3 HBCLK cycles. Figure 4 illustrates the relative signal timing in Framer Bypass mode.

Figure 3: Relative Timing for Data Interface in T1 Transport Mode

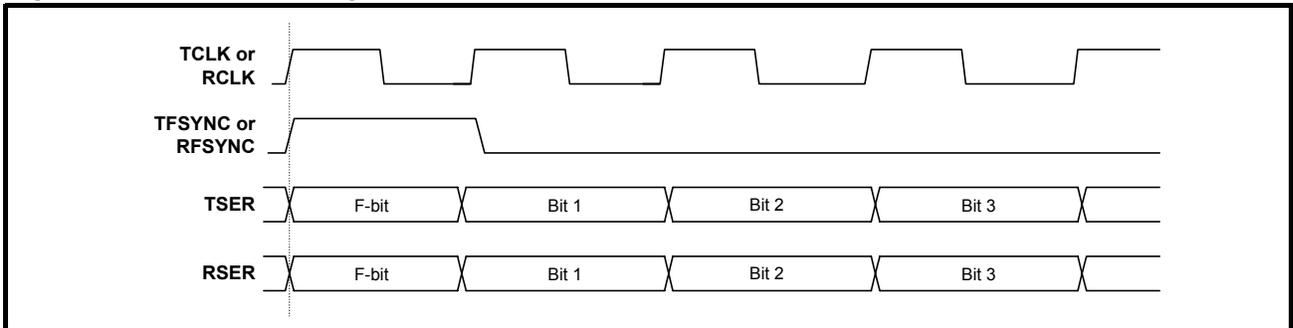
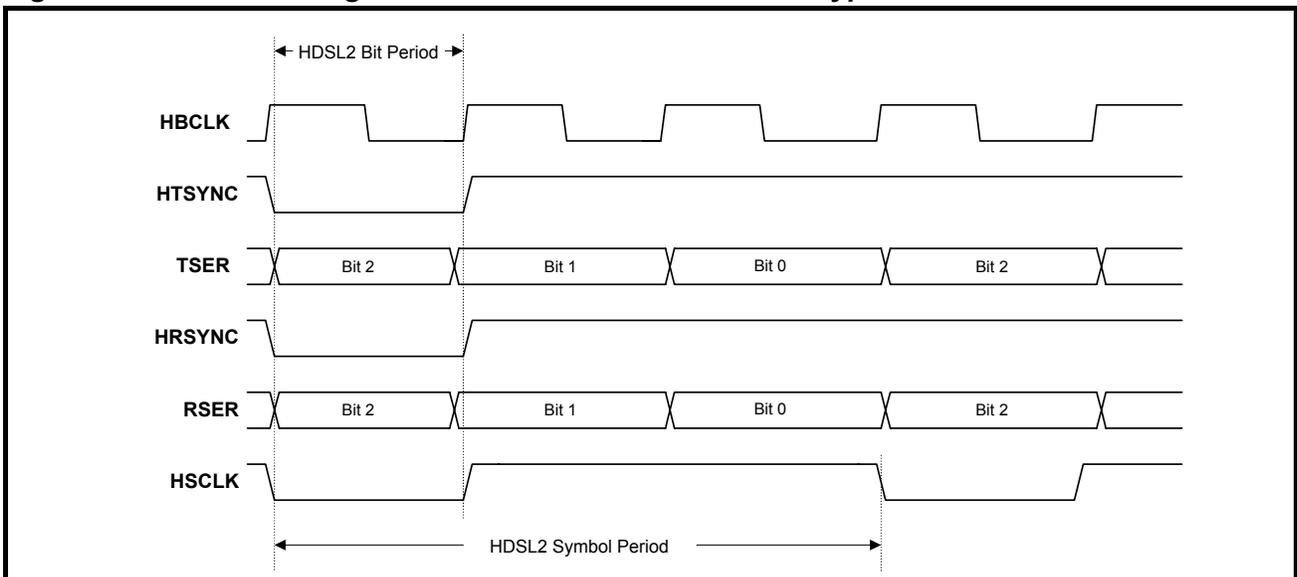


Figure 4: Relative Timing for the Data Interface in Framer Bypass Mode



Framer/Mapper

The SK70742 framer/mapper is programmable to support a payload of $N \times 64 + 8$ kbps with 8 kbps of HDSL2 framing & overhead, or a payload of $N \times 64$ kbps with 8 kbps of HDSL2 framing & overhead plus an additional 8 kbps of user-defined overhead.

The number of 64 kbps payload time slots, N , is specified in bits 5:0 of the PLRATE register (where bit 5 is the MSB). The framer supports values of N between 2 and 32. Bit 6 of the PLRATE register selects the payload size. When bit 6 is set to '1' the payload is $N \times 64$ kbps. When bit 6 = '0', the payload is $N \times 64 + 8$ kbps (to support T1 HDSL2 transport with $N=24$).

In the $N \times 64$ kbps payload configuration, 8 kbps of user defined Z-bit overhead data is accessible through registers. The Z-bits may be written to the HTFZB1-HTFZB6 registers and read from the HRFZB1-HRFZB6 registers.

The framer/mapper may be disabled (i.e. bypassed) by setting bit 5 in the HRFTR register to '1'. Note that in framer bypass mode, the scrambler and descrambler functions are not available.

T1 Frame Mapping

The SK70742 maps a 1.544 Mbps DS1 payload (consisting of 24 DS0 channels and 8 kbps of DS1 framing) into the 1.552 Mbps HDSL2 frame format shown in [Table 2 on page 9](#). Normally, the DS1 payload and HDSL2 frames are not aligned with respect to one another. The SK70742 maps T1 frames into the HDSL2 frame format.

Figure 5 shows the HDSL2 frame structure. Nominally, the frame is 6 msec in length and consists of 48 overhead bits and 4 payload blocks.

All transmit data, except the sync word and stuff bits, are scrambled prior to moving to the FEC stage. Configuration of the scramblers is accomplished through the HTFTMR register. The upstream and downstream polynomials are as follows:

- H2TU-C Scrambler = $x^{-23} + x^{-5} + 1$
- H2TU-C Descrambler = $x^{-23} + x^{-18} + 1$
- H2TU-R Scrambler = $x^{-23} + x^{-18} + 1$
- H2TU-R Descrambler = $x^{-23} + x^{-5} + 1$

Transmit Frame Mapping

The frame mapper receives data from the TDM bus and multiplexes a SYNC word, Cyclic Redundancy Check (CRC) bits, HDSL2 Over Head (HOH) and stuff bits into the HDSL2 frame. The data is scrambled prior to being sent to the FEC encoder. The 6 msec HTSYNC pulse defines HDSL2 frame boundaries. The framer automatically manages the sync, CRC, and bit stuffing functions. 24 EOC bits are accessible through the device registers.

The CRC is calculated for every frame, excluding the 10 bit SYNC word, 6 CRC bits, and any stuff bits. Each calculated CRC is inserted into the subsequent frame. The CRC Polynomial is X^6+X+1 . Check bits `crc1-crc6`, contained in the frame, are associated with the contents of the preceding frame.

When there is no preceding frame, the CRC number will be set to a default of zero. At the receive end, the CRC polynomial is multiplied by X^6 and divided by X^6+X+1 to determine if an error has occurred. Errors are reported in the HRFSR register.

The average HDSL2 frame transports 48 overhead bits. The name and function of these overhead bits is defined by ANSI T1E1.418 and are described in [Table 2 on page 9](#).

Since the upstream and downstream T1 payload rates are not synchronous with the HDSL2 symbol rate, bit stuffing is used to handle the rate adaptation between the symbol rate and the payload rate. FIFO buffers in the transmit and receive data path are used to monitor and buffer the variations in transmission rate. The insertion of stuffing bits is done automatically based on the transmit FIFO water level. By adjusting the ratio of frames with stuffing to those without stuffing, data is carried across the HDSL2 symbol stream at the payload data rate. Stuff indicator bits are added to the HDSL2 frame to improve the system's ability to recover from impulse noise during a frame sync error.

With bit stuffing, the data stream may experience a low frequency timing wander. Wander reduction may be implemented by modulating the FIFO water levels.

Figure 5: SK70742 HDSL2 Frame Structure for T1 Payload

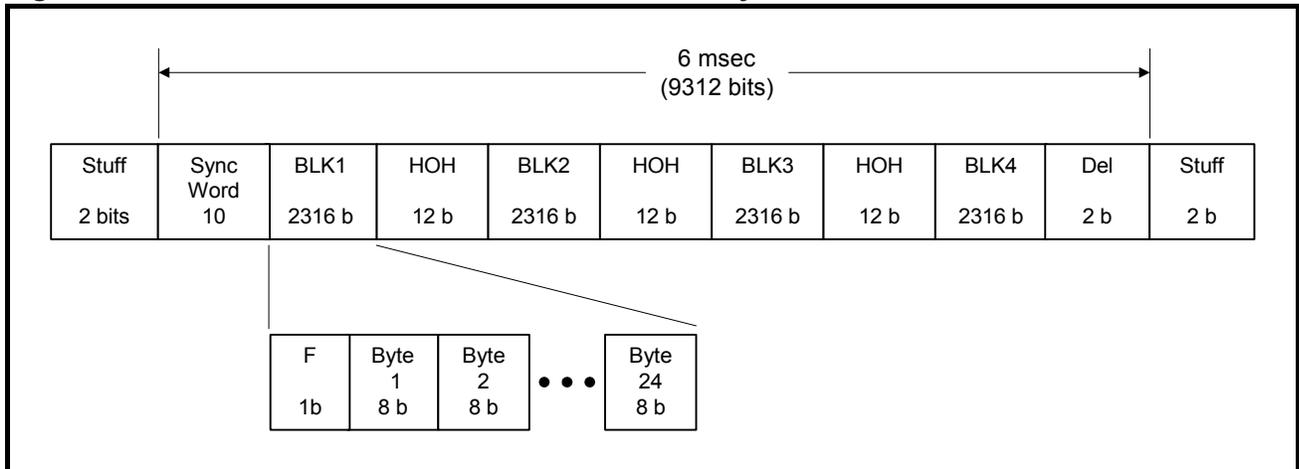


Figure 6: Transmit Framer Block Diagram

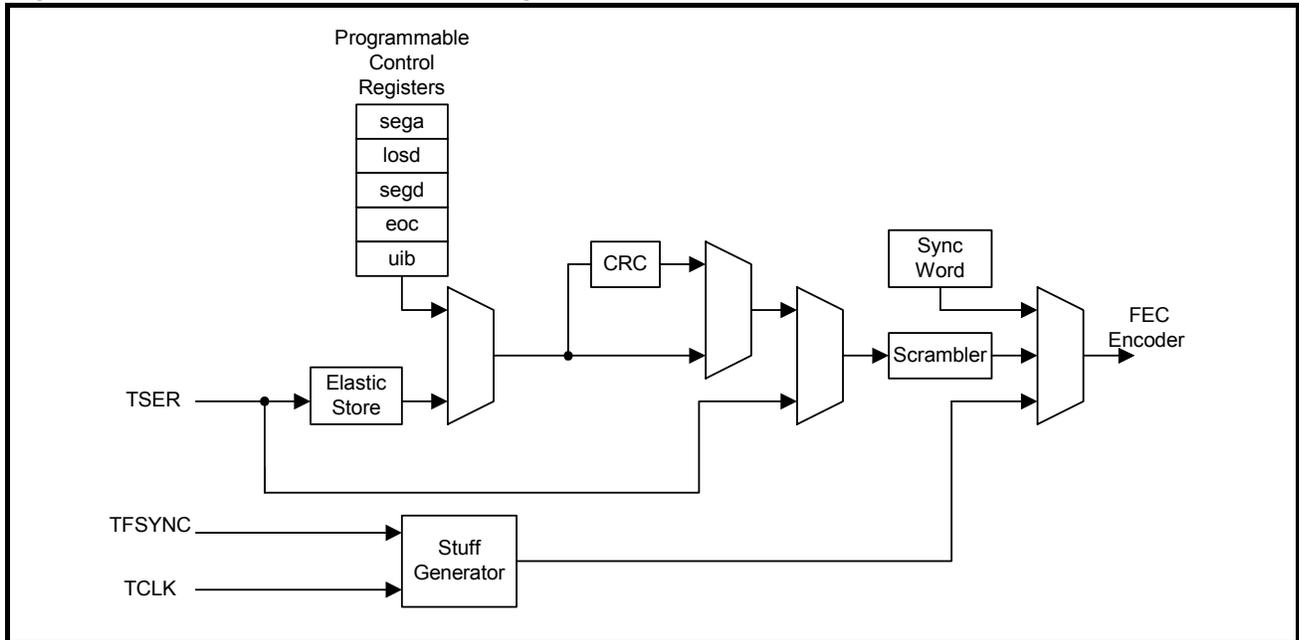


Table 2: HDSL2 Frame Structure for T1, N=24 Time Slots

Frame Bit #	HOH Bit #	Name	Description
1-10	1-10	sw1-10	Sync word, 10 bits
11-2326	-	B1	Payload Block 1
2327	11	crc1	CRC-6 bit 1 for previous frame
2328	12	crc2	CRC-6 bit 2 for previous frame
2329	13	sbid1	Stuff Bit Identification 1
2330	14	losd	DS1 loss of signal detect
2331-2338	15-22	eoc01-eoc08	EOC bit 1 - EOC bit 8
2339-4654	-	B2	Payload Block 2

Table 2: HDSL2 Frame Structure for T1, N=24 Time Slots – continued

Frame Bit #	HOH Bit #	Name	Description
4655	23	crc3	CRC-6 bit 3 for previous frame
4656	24	crc4	CRC-6 bit 4 for previous frame
4657	25	uib	Unspecified indicator bit
4658	26	sega	Segment Anomaly
4659-4666	27-34	eoc9-eoc16	EOC bit 10 through EOC bit 16
4667-6982	-	B3	Payload Block 3
6983	35	crc5	CRC-6 bit 5 for previous frame
6984	36	crc6	CRC-6 bit 6 for previous frame
6985	37	sbid2	Stuff Bit Identification 2
6986	38	segd	Segment defect
6987-6994	39-46	eoc17-eoc24	EOC bit 17 through EOC bit 24
6995-9310	-	B4	Payload Block 4
9311	47	sb1	stuff bit 1
9312	48	sb2	stuff bit 2
9313	49	sb3	stuff bit 3
9314	50	sb4	stuff bit 4

Table 3: HDSL2 Overhead Bit to Register Mapping

HOH bit#	Name	Write Register	Bit #	Read Register	Bit #
1	fsw1	HTFFSW1	7	Not available	-
2	fsw2	HTFFSW1	6	Not available	-
3	fsw3	HTFFSW1	5	Not available	-
4	fsw4	HTFFSW1	4	Not available	-
5	fsw5	HTFFSW1	3	Not available	-
6	fsw6	HTFFSW1	2	Not available	-
7	fsw7	HTFFSW1	1	Not available	-
8	fsw8	HTFFSW1	0	Not available	-
9	fsw9	HTFFSW2	1	Not available	-
10	fsw10	HTFFSW2	0	Not available	-
11	crc1	Internally generated	-	Not available	-
12	crc2	Internally generated	-	Not available	-
13	sbid1	Internally generated	-	HRFFDR	7
14	losd	HTFHOH3	5	HRFHOH3	5
15	eoc1	HTFHOH3	6	HRFHOH3	6
16	eoc2	HTFHOH1	0	HRFHOH1	0
17	eoc3	HTFHOH1	1	HRFHOH1	1

Table 3: HDSL2 Overhead Bit to Register Mapping – continued

HOH bit#	Name	Write Register	Bit #	Read Register	Bit #
18	eoc4	HTFHOH1	2	HRFHOH1	2
19	eoc5	HTFHOH1	3	HRFHOH1	3
20	eoc6	HTFHOH1	4	HRFHOH1	4
21	eoc7	HTFHOH1	5	HRFHOH1	5
22	eoc8	HTFHOH1	6	HRFHOH1	6
23	crc3	Internally generated	-	Not available	-
24	crc4	Internally generated	-	Not available	-
25	uib	HTFHOH3	7	HRFHOH3	7
26	sega	HTFHOH4	4	HRFHOH4	4
27	eoc9	HTFHOH4	5	HRFHOH4	5
28	eoc10	HTFHOH1	7	HRFHOH1	7
29	eoc11	HTFHOH2	0	HRFHOH2	0
30	eoc12	HTFHOH2	1	HRFHOH2	1
31	eoc13	HTFHOH2	2	HRFHOH2	2
32	eoc14	HTFHOH2	3	HRFHOH2	3
33	eoc15	HTFHOH2	4	HRFHOH2	4
34	eoc16	HTFHOH2	5	HRFHOH2	5
35	crc5	Internally generated	-	Not available	-
36	crc6	Internally generated	-	Not available	-
37	sbid2	Internally generated	-	HRFFDR	6
38	segd	HTFHOH4	6	HRFHOH4	6
39	eoc17	HTFHOH4	7	HRFHOH4	7
40	eoc18	HTFHOH2	6	HRFHOH2	6
41	eoc19	HTFHOH2	7	HRFHOH2	7
42	eoc20	HTFHOH3	0	HRFHOH3	0
43	eoc21	HTFHOH3	1	HRFHOH3	1
44	eoc22	HTFHOH3	2	HRFHOH3	2
45	eoc23	HTFHOH3	3	HRFHOH3	3
46	eoc24	HTFHOH3	4	HRFHOH3	4
47	sb1	HTFHOH4	3	HRFHOH4	3
48	sb2	HTFHOH4	2	HRFHOH4	2
49	sb3	HTFHOH4	1	HRFHOH4	1
50	sb4	HTFHOH4	0	HRFHOH4	0

ANSI T1E1.418 HDSL2 uses High-speed Data Link Control (HDLC) framing to transfer EOC messages between each end of the link. Each EOC frame may consist of one or more messages. Start and stop flags delineate the frame, while a 16 bit CRC is used for the Frame Check Sequence (FCS). Each EOC message is an integer number of octets and contains the following common fields.

- Message Type
- Length
- Source ID
- Information

The following message types are defined by ANSI:

- Performance Status
- Read Request
- Read Acknowledgment
- Configuration Request
- Register Status
- Priority Message

The SK70742 supports ANSI EOC messaging by providing access to the EOC bits through the HTFOH1-HTFOH4 and the HRFOH1-HRFOH4 registers. Management of these bits and the HDLC controller function is left to the system microprocessor.

Receive Frame Mapping

The receive framer aligns the frame, removes stuffing bits, and monitors error performance. From the FEC decoder, the data is first descrambled. Once a sync word is detected, the framer is able to count bits and locate the other overhead data.

CRC bits crc1-crc6 are checked, and the errors are monitored, with a counter. CRC errors are reported to the HRFCRC register. The remaining overhead bits should be read from the HRHOH1-HRHOH4 registers during each receive frame interrupt.

Figure 7: EOC Frame Format

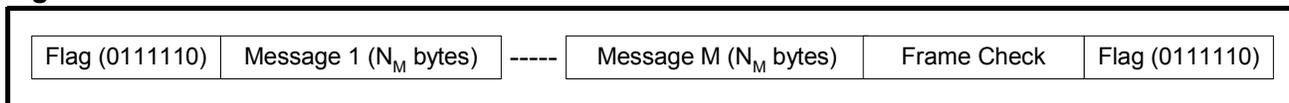
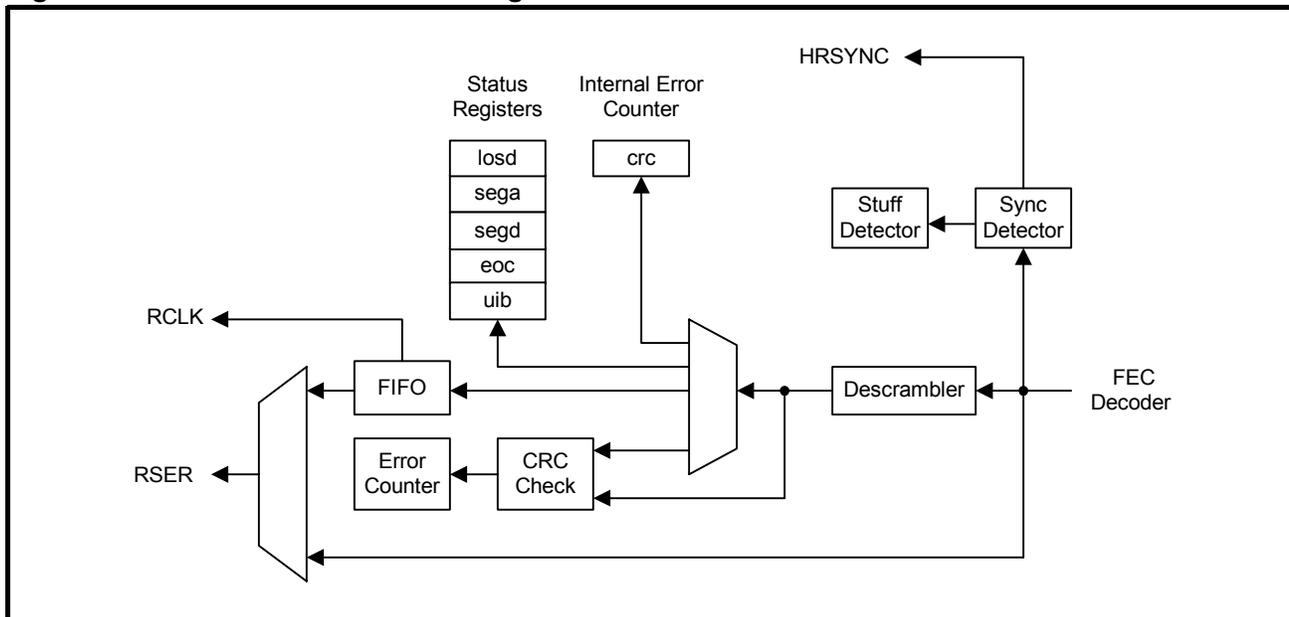


Figure 8: Receive Framer Block Diagram

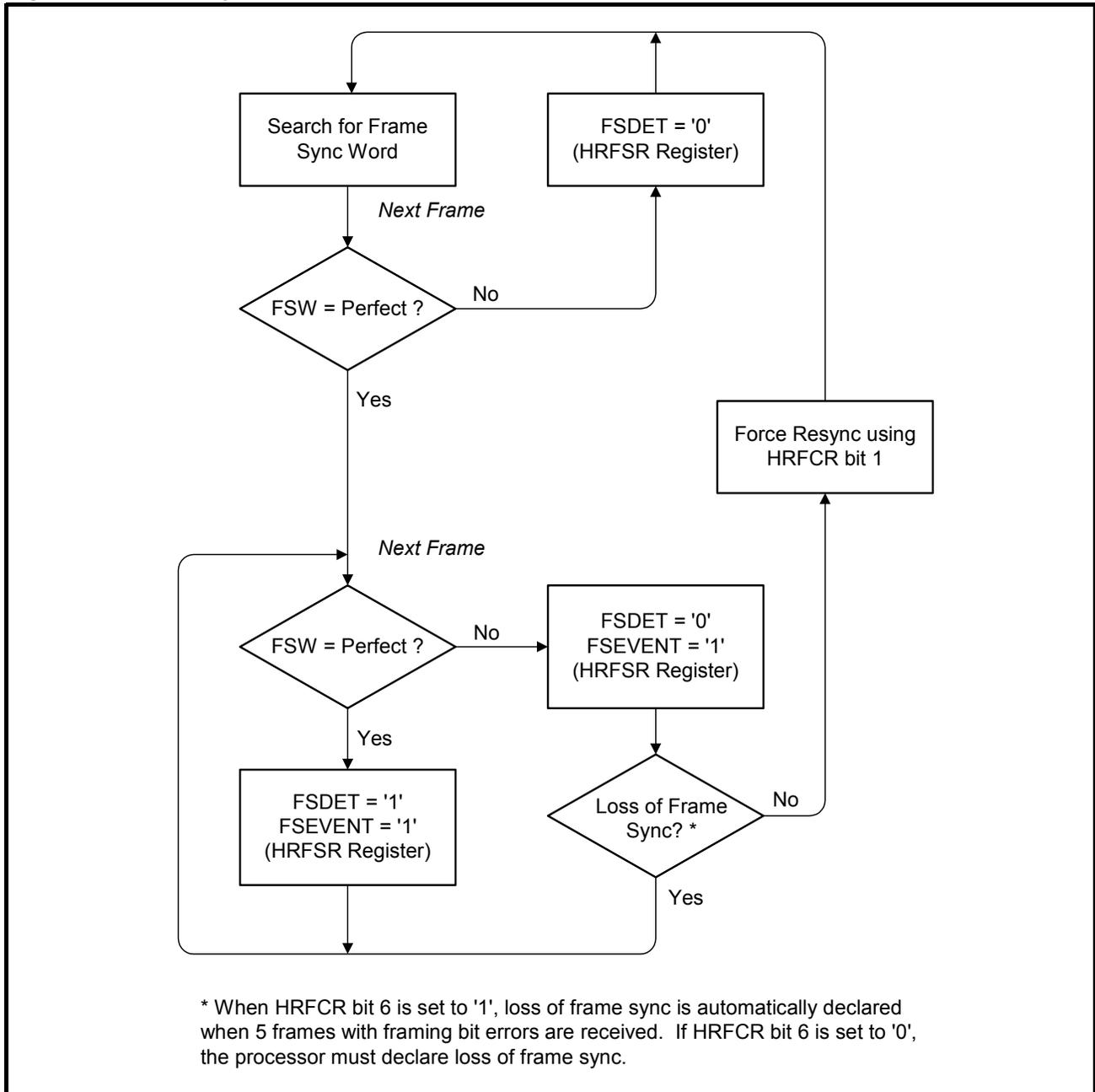


Frame Synchronization

See Figure 9. Frame synchronization may be monitored in the Receive Status register (HRFSR) with the fsevent, fcsync, and fsdet bits. Once the frame mapper receives two frames with valid framing bits, fcsysnc is set to '1' and the 6 ms receive frame interrupt is enabled. The system processor must read the HRFSR every 6 ms to monitor frame sync status and CRC errors. The fsevent bit is set to '1' during the 6 ms interrupt to indicate the start of each

HDSL2 receive frame. The HRFSR should be read during the interrupt. If no framing bit errors were detected, the fsdet bit is set to '1'. If a frame with framing bit errors was received, the fsdet bit is set to '0'. The system processor may handle loss of frame sync detection using the fsdet bit. Alternatively, the SK70742 will automatically declare loss of frame sync when the HRFCR register bit "up_syncdis" is set to '1'.

Figure 9: Frame Synchronization State Machine



Forward Error Correction (FEC)

FEC Encoder

The SK70742 utilizes Trellis Coded Modulation (TCM) to provide over 5 dB of coding gain to the HDSL2 transmission system. In the transmit direction, the HDSL2 frame mapper generates a 3 bit data vector: X[2:0]. As shown in Figure 10, bit X0 is encoded and sent to a rate 1/2 convolution encoder with a constraint length of 20. The output of the encoder is sent to the one dimensional symbol mapper, along with bits X[2:1]. The output symbol, S, is subsequently transmitted on the transmission line.

Figure 10: FEC Encoder and Symbol Mapping

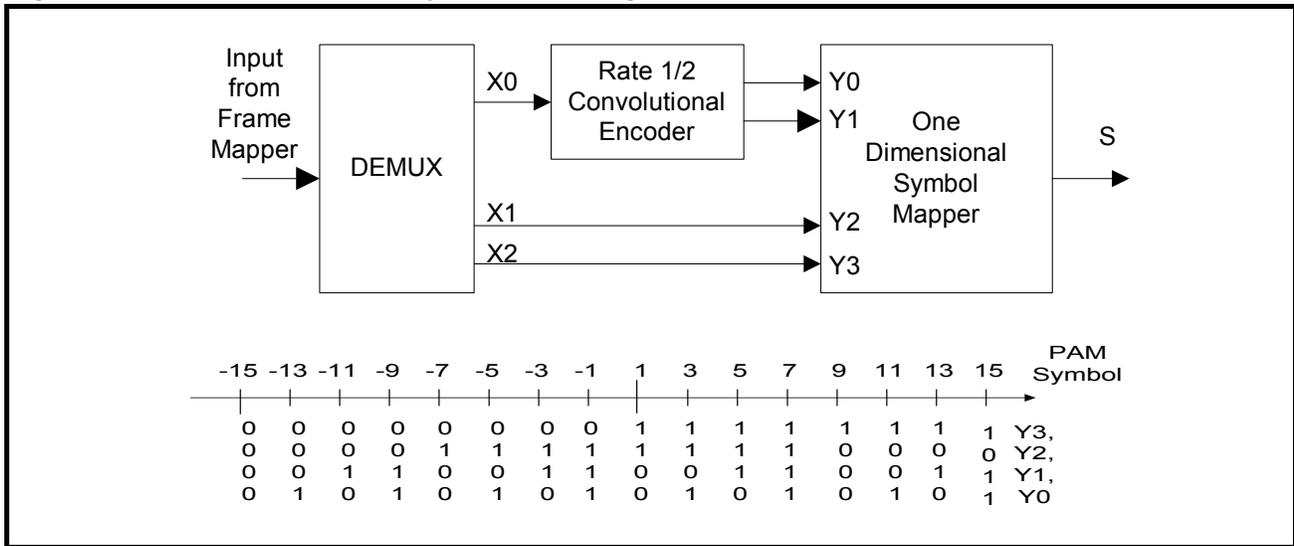


Figure 11: Convolutional Encoder

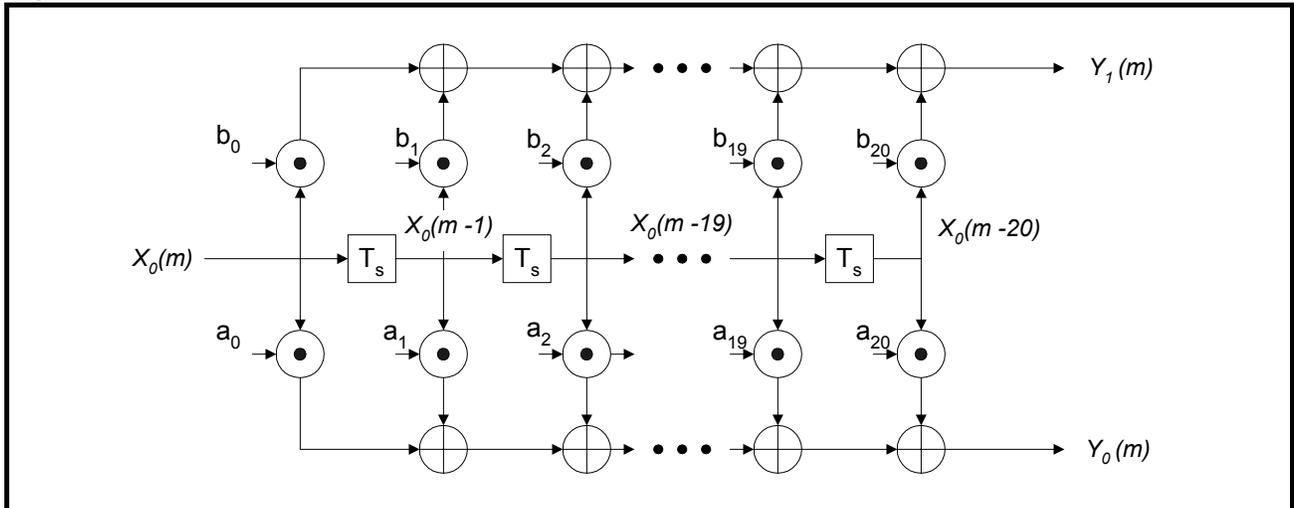


Figure 11 shows a block diagram of the feed-forward convolutional encoder. T_s is a delay of one symbol time, “ \oplus ” is a binary exclusive-OR and “ \cdot ” is a binary AND. The encoder is essentially a shift register, whereby each tap is multiplied by a binary coefficient. The numerical representation of the coefficients are A and B where:

$$A = a_{20} \cdot 2^{20} \oplus a_{19} \cdot 2^{19} \oplus a_{18} \cdot 2^{18} \dots \oplus a_0 \cdot 2^0$$

$$B = b_{20} \cdot 2^{20} \oplus b_{19} \cdot 2^{19} \oplus b_{18} \cdot 2^{18} \dots \oplus b_0 \cdot 2^0$$

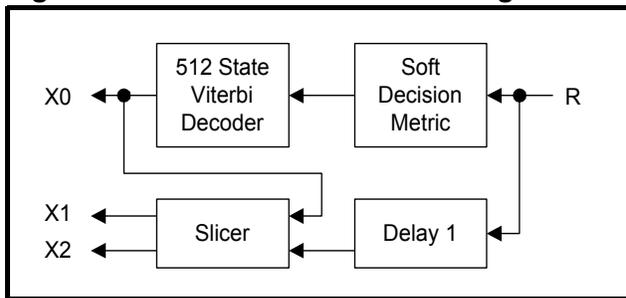
The coefficient values may be programmed through the CG0 and CG1 registers. During activation, the A and B coefficients may be passed from the H2TU-C to H2TU-R to configure the system for alternate line codes.

FEC Decoder

In the receive direction, the decoder receives 10 bit soft decision words (R) from the preceding slicer. As shown in Figure 12, outputs from the decoder are 3 bit vectors, X[2:0], passed to the subsequent framer.

A soft decision metric is first calculated from the symbol (R) before it moves to the 512 state Viterbi block. The Viterbi decoder produces the LSB (X0) of the received symbol. The R symbol is also sent to a delay and slicer block to recover the X[2:1] bits, completing the 3 bit vector. The delay block compensates for the delay of the Viterbi decoder.

Figure 12: FEC Decoder Block Diagram



SK70741 Interface

Data is passed serially between the SK70742 and SK70741 transceiver via the FEC_TX and FEC_RX lines. Bit transfers are synchronized with the rising edge of the FCLK line from the SK70741. The FCLK rate is 11 times the bit rate, or 33 times the symbol rate.

An enable signal, $\overline{\text{FCE}}$, is asserted for 16 consecutive FCLK cycles to indicate that the data on the FEC_TX and FEC_RX lines is valid. $\overline{\text{FCE}}$ then stays High for another 17 clock cycles, until the end of the HDSL symbol.

Data transfers are 16 bits in length and move across the interface LSB first and MSB last. In the transmit direction, the encoded symbol information is contained in the first 4 bits of the 16 bit word. The remaining bits are reserved. In the receive direction, the first 4 bits provide a control word from the SK70741 transceiver. A '1' in the first bit position indicates that the following bits to the FEC are a code word. A '1' in the second bit position requests the SK70742 to send out a code word in the next HDSL2 symbol. The third and fourth bits are reserved. The remaining 12 bits of the 16 bit word contain soft decision information from the SK70741 demodulator.

Test and Diagnostic Features

JTAG Interface

A JTAG test port is included in the SK70742 to enable boundary scan testing at the system manufacturing level. The JTAG port is fully compliant with the IEEE standard 1149.1-1990, "Standard Test Access Port and Boundary Scan Architecture" set by the Joint Test Actions Group (JTAG). Board connectivity can be verified at all digital pins through a set of three instructions accessible through the use of a state machine standard to all JTAG controllers. Refer to IEEE 1149.1 specification for details concerning the JTAG Instruction Register and JTAG state machine.

Loopbacks

The SK70742 provides for loopback at the Data Interface. Control register HRFTTCR selects loopback in two directions as shown in Figure 14. Remote loopback connects RSER to TSER, RCLK to TCLK, and RFSYNC to TFSYNC returning data from the HDSL2 line back toward the far-end transceiver. Local loopback connects TSER to RSER, TCLK to RCLK, and TFSYNC to RFSYNC returning data from the external framer or T1/E1 line interface back to it.

Microprocessor Interface

The microprocessor interface provides access to internal control and status registers. The interface may be configured for either Motorola 68000 series or Intel 80C51 series microprocessors. The configuration of the interface is set by the $\overline{\text{I/M}}$ (Intel/Motorola) pin.

Intel Parallel Bus

Setting the $\overline{\text{I/M}}$ line Low selects the Intel mode that uses the following four control pins to move data across the multiplexed address/data bus:

Chip Select: $\overline{\text{CS}}$ requires an active Low signal to enable transceiver read or write operations.

Data Read: $\overline{\text{RD}}$ requires an active Low pulse to enable a read transfer on the data bus. When $\overline{\text{RD}}$ is pulled Low, the data bus lines from the SK70742 go from tristate to active and output the data from the addressed register.

Data Write: $\overline{\text{WR}}$ requires an active Low pulse to enable a write transfer on the data bus. Data transfer is triggered by

the falling edge of the \overline{WR} pulse. To ensure data is written to the register addressed by AD<7:0>, valid data must be present on the SK70742 data bus lines before \overline{WR} goes Low.

Address Latch Enable: During a read or write operation, the SK70742 latches the address on AD<7:0> on the falling edge of ALE.

NOTE

In Intel mode, A0 and A2 must be grounded to disable a factory test mode.

Chip Select: \overline{CS} requires an active Low signal to enable transceiver read or write operations.

Read/Write: The R/\overline{W} pin requires an active High pulse to enable a read transfer and an active Low pulse to initiate a write transfer on the data bus.

Data Strobe: The \overline{DS} requires an active Low pulse to enable a data transfer to and from the data bus. Data transfer occurs on the falling edge of the \overline{DS} pulse. Valid data must be present on the SK70742 data bus lines (AD<7:0>) before \overline{DS} goes Low.

Interrupt

\overline{INT} is an open drain output requiring an external pull-up resistor. The \overline{INT} pin goes Low when an internal interrupt condition occurs as specified in the HRFFDR and HRFSR registers. \overline{INT} is latched and held Low until the interrupt condition is cleared.

Motorola Parallel Bus

Setting the $\overline{I/M}$ line High selects the Motorola configuration that uses the following three control pins to move data across the interface:

Figure 13: Relative Timing for FEC to Transceiver Interface

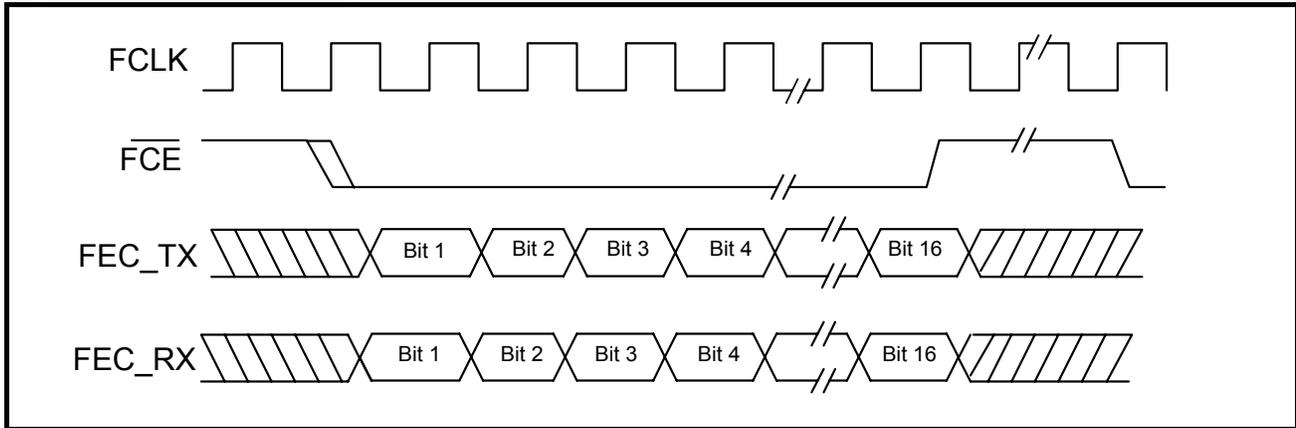
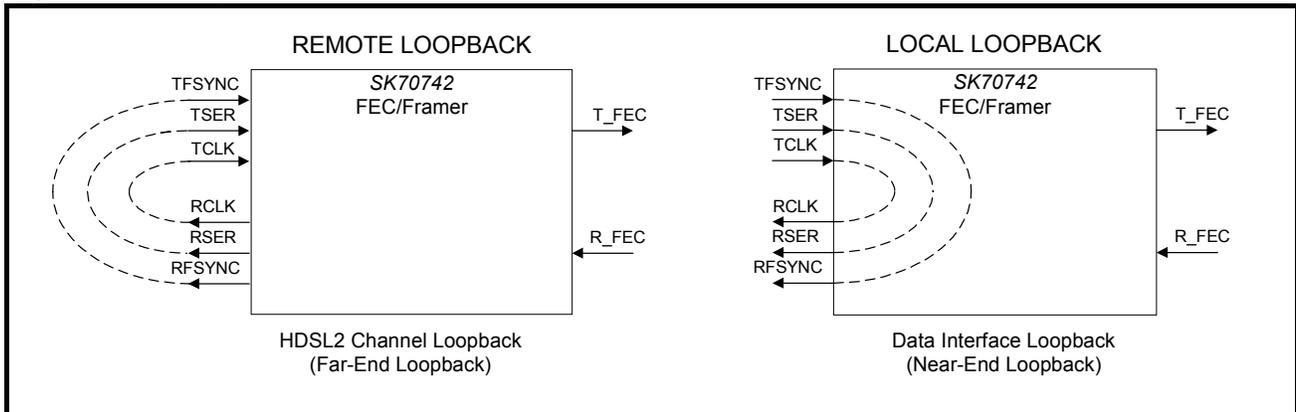


Figure 14: Loopback of the Data Interface and HDLSL2 Channel



REGISTER DESCRIPTION

The SK70742 registers are accessed through the microprocessor interface. Table 4 summarizes the registers and the following tables provide detailed descriptions.

After asserting the $\overline{\text{RST}}$ signal, the SK70742 registers are initialized to their default values. Note that multiple byte registers are assigned consecutive addresses such that the lowest address is assigned to the lowest 8 bits of the register.

Table 4: SK70742 Register Summary

Address (hex)	Register Label	Access	General Description
FEC			
80	CGSEL	R/W	Selects code generator for encoder and decoder and loopback
81, 82, 83	CG	R/W	FEC code generator register
84	FECTB	R/W	Viterbi decoder trace back depth
85	FECNS	R	FEC slicer error register - used for SNR computation
86-92	–	–	Reserved ¹
93	FECRC	R/W	FEC control register
94 - 9F	–	–	Reserved ¹
HTFM			
A0	PLRATE	R/W	Payload bit rate parameter
A1	HTFWL	R/W	Reference water level for transmit FIFO
A2	TFWL	R	Actual Water Level For Transmit FIFO
A3	HTFCR	R/W	Transmit control register
A4	HTFPCR	R/W	Transmit test control register
A5	HTFBSR	R/W	Data byte selector register
A6	HTFRSRH	R	Data read sample register (high byte)
A7	HTFRSRL	R	Data read sample register (low byte)
A8	HTFTMR	R/W	Transmit mode and HDSL2 frame control register
A9	HTFFSW1	R/W	First 8 transmit frame sync word (FSW) bits
AA	HTFFSW2	R/W	Last 2 transmit frame sync word (FSW) bits
AB	HTFZB1	R/W	Transmit Z-bit register 1 (N x 64 kbps framing mode)
AC	HTFZB2	R/W	Transmit Z-bit register 2 (N x 64 kbps framing mode)
AD	HTFZB3	R/W	Transmit Z-bit register 3 (N x 64 kbps framing mode)
AE	HTFZB4	R/W	Transmit Z-bit register 4 (N x 64 kbps framing mode)
AF	HTFZB5	R/W	Transmit Z-bit register 5 (N x 64 kbps framing mode)
B0	HTFZB6	R/W	Transmit Z-bit register 6 (N x 64 kbps framing mode)
B1	HTFHOH1	R/W	Transmit HDSL2 Overhead register 1
B2	HTFHOH2	R/W	Transmit HDSL2 Overhead register 2
B3	HTFHOH3	R/W	Transmit HDSL2 Overhead register 3
1. These registers are reserved for factory test features and must not be accessed during normal operation.			

Table 4: SK70742 Register Summary – continued

Address (hex)	Register Label	Access	General Description
B4	HTFHOH4	W	Transmit HDLSL2 Overhead register 4
B5-BF	–	–	Reserved ¹
HRFM			
C0	HRFCR	R/W	Receive control register
C1	HRFTCR	R/W	Receive test control registers
C2	HRFWL	R	Receive FIFO water level register
C3	HRFFDR	R	Receive FIFO status register
C4	HRFSR	R	Receive status register
C5	HRFTTCR	R/W	Timing and loopback control register
C6	HRFNCR1	R/W	NCO control register, MSBs
C7	HRFNCR2	R/W	NCO control register, LSBs
C8	-	-	Reserved ¹
C9	HRFCRC	R	CRC error counter register
CA	HRFPAJ	R/W	Phase adjustment parameters register
CB	HRFPAC	R/W	NCO clock division ratio register
CC	HRFZB1	R	Receive Z-bit register 1 (N x 64 kbps framing mode)
CD	HRFZB2	R	Receive Z-bit register 2 (N x 64 kbps framing mode)
CE	HRFZB3	R	Receive Z-bit register 3 (N x 64 kbps framing mode)
CF	HRFZB4	R	Receive Z-bit register 4 (N x 64 kbps framing mode)
D0	HRFZB5	R	Receive Z-bit register 5 (N x 64 kbps framing mode)
D1	HRFZB6	R	Receive Z-bit register 6 (N x 64 kbps framing mode)
D2	HRFHOH1	R	Receive HDLSL2 Overhead register 1
D3	HRFHOH2	R	Receive HDLSL2 Overhead register 2
D4	HRFHOH3	R	Receive HDLSL2 Overhead register 3
D5	HRFHOH4	R	Receive HDLSL2 Overhead register 4
D6 - DF	–	–	Reserved ¹
JTAG			
E0	TJCR	R/W	JTAG Control register

1. These registers are reserved for factory test features and must not be accessed during normal operation.

FEC Encoder/Decoder Configuration Registers

The CGSEL register controls the FEC encoder/decoder loopback and enables programming of the encoder or decoder using CG1, CG2 and CG3. The CG1, CG2 and CG3 registers specify the a and b coefficients for the decoder and the 20-tap convolutional encoder. A diagram of this encoder is shown in Figure 11 on page 14.

Table 5: Code Generator Select, CGSEL, R/W, Address = 80h, Default = 00h

Bit	Name	Description
7:2	rs	Reserved. Must be set to '0' when written.
2	fecloop	1 = loopback from encoder output to decoder input.
1:0	cgsel	Selection of code generator for encoder and decoder: 00 = Program decoder $a_9 - a_0$ and $b_9 - b_0$ using CG1, CG2 and CG3. 10 = Program encoder $a_{20} - a_0$ using CG1, CG2 and CG3. 11 = Program encoder $b_{20} - b_0$ using CG1, CG2 and CG3.

Table 6: Code Generator 1, CG1, R/W, Address = 81h, Default = DAh

Bit	Name	Description
7:4	-	Reserved. Must be '0' when written.
3:0	cg	Code generator bits: When cgsel = 00, program decoder: bit7 = a_7 , bit6 = a_6 , bit5 = a_5 , bit4 = a_4 , bit3 = a_3 , bit2 = a_2 , bit1 = a_1 , bit0 = a_0 When cgsel = 10, program encoder: bit7 = a_7 , bit6 = a_6 , bit5 = a_5 , bit4 = a_4 , bit3 = a_3 , bit2 = a_2 , bit1 = a_1 , bit0 = a_0 . When cgsel = 11, program encoder: bit7 = b_7 , bit6 = b_6 , bit5 = b_5 , bit4 = b_4 , bit3 = b_3 , bit2 = b_2 , bit1 = b_1 , bit0 = b_0 .

Table 7: Code Generator 2, CG2, R/W, Address = 82h Default = CDh

Bit	Name	Description
7:0	cg	Code generator bits When cgsel = 00, program decoder: bit7 = b_5 , bit6 = b_4 , bit5 = b_3 , bit4 = b_2 , bit3 = b_1 , bit2 = b_0 , bit1 = a_9 , bit0 = a_8 . When cgsel = 10, program encoder: bit7 = a_{15} , bit6 = a_{14} , bit5 = a_{13} , bit4 = a_{12} , bit3 = a_{11} , bit2 = a_{10} , bit1 = a_9 , bit0 = a_8 . When cgsel = 11, program encoder: bit7 = b_{15} , bit6 = b_{14} , bit5 = b_{13} , bit4 = b_{12} , bit3 = b_{11} , bit2 = b_{10} , bit1 = b_9 , bit0 = b_8 .

Table 8: Code Generator 3, CG3, R/W, Address = 83h, Default = 08h

Bit	Name	Description
7:0	cg	Code generator bits When cgsel = 00, program decoder: bit7 - bit4 must be set to '0', bit3=b ₉ , bit2=b ₈ , bit1=b ₇ , bit0=b ₆ When cgsel = 10, program encoder: bit7 - bit5 must be set to '0', bit4=a ₂₀ , bit3=a ₁₉ , bit2=a ₁₈ , bit1=a ₁₇ , bit0=a ₁₆ . When cgsel = 11, program encoder: bit7 - bit5 must be set to '0', bit4=b ₂₀ , bit3=b ₁₉ , bit2=b ₁₈ , bit1=b ₁₇ , bit0=b ₁₆ .

Viterbi Decoder Trace Back Depth

Table 9: FEC Trace Back, FECTB, R/W, Address = 84h, Default = 00h

Bit	Name	Description
7:5	rs	Reserved. Must be set to '0' when written.
4:0	fectb	Trace back depth of the Viterbi Decoder = fectb[4:0] x 4. Note that fectb is an integer ranging from 0 to 16. The maximum trace back length is 64. A lower trace back can reduce latency with a trade-off in coding gain.

FEC Noise Register

The FECNS register provides a noise estimate based on a comparison of the soft decision data to the output of the Viterbi decoder. The 8 bit format is 3 integer bits and 5 fractional bits ($2^1, 2^0, 2^{-1}, 2^{-2}, 2^{-3}, 2^{-4}, 2^{-5}$) in the range of -4 and +4. The system microprocessor can average the 2's complement of the FECNS register to determine the average noise power. The average FECNS value is then compared to the average signal power to determine the system SNR. For a PAM 16 constellation, the relationship is:

$$SNR = 10 \log \frac{85}{\frac{1}{n} \sum_1^n (FECNS)^2}$$

85 is the variance of the PAM 16 constellation (+15, +13, +11..... -11, -13, -15). Typically the power is estimated over 128 symbols, however, resolution can be increased if the noise is averaged over a longer symbol stream.

Table 10: FEC Noise, FECNS, R, Address = 85h

Bit	Name	Description
7:0	fecns	FEC slicer error. Can be used by the microcontroller to compute channel SNR as described above.

FEC Control Register

Table 11: FEC Control, FECCR, R/W, Address = 93h, Default = 00h

Bit	Name	Description
7:2	–	Reserved. Must be set to '0' when written.
1	fecht	0 = FEC operating 1 = FEC halted
0	fecbp	0 = FEC encoder and decoder included in the data path 1 = FEC encoder and decoder bypassed

HTFM Payload Bit Rate Parameters

Table 12: Framer Payload Rate, PLRATE, R/W, Address = A0h, Default = 18h

Bit	Name	Description
7	rs	Reserved. Must be set to '0' when written.
6	t1_e1	1 = (N x 64) kbps payload 0 = (N x 64+8) kbps payload (used for T1 HDSL2 transport with n=24)
5:0	n	Number of 64 kbps payload time slots. May be any integer from 2 to 32.

HTFM Water Level for Transmit FIFO

Table 13: Reference Transmit Water Level, HTFWL, R/W, Address = A1h, Default = 2Eh

Bit	Name	Description
7:0	htfwl	Water Level for Transmit FIFO. The water level has direction. The FIFO depth is 80 bits. The write pointer should be ahead of the read pointer by 40 bits. If the FIFO is loaded above the water level, no stuff bits are inserted. If the FIFO is loaded below the water level, four stuff bits are inserted.

Table 14: Actual Transmit Water Level, TFWL, R, Address = A2h

Bit	Name	Description
7:0	tfwl	Actual water level for transmit FIFO. Granularity determined by htflw_res in HTFCR register

HTFM Framer Transmit Registers

Table 15: Transmit Control Register, HTFCR, R/W, Address = A3h, Default = 08h

Bit	Name	Description
7	rs	Reserved. Must be set to '0' when written.
6	htflw_res	1 = 0.25 UI granularity of the TFLW register 0 = 0.50 UI granularity of the TFLW register
5	h_fif_rst	Set this bit to '1' and then '0' to reset the transmit FIFO pointers at initialization or whenever the HTFWL register has been reprogrammed.
4	h_frm_rst	Set this bit to '1' and then '0' to reset the transmit frame counter at initialization.
3	ds1sync_dis	1 = disable synchronization of the HDSL2 transmit frame alignment to the T1 frame alignment using TFSYNC. This configuration is recommended for HDSL2 T1 transport. 0 = force synchronization of the HDSL2 transmit frame alignment to the T1 frame alignment using TFSYNC. This configuration allows the receive T1 frame position to be recovered from the HDSL2 receive frame sync but will require HDSL2 receive framer resynchronization every time the T1 frame alignment shifts.
2	dis_frslip	Set this bit to '1' to reset the FIFO overflow/underflow alarm bits in the HRFFDR register, clear the pending interrupt, and disable future FIFO interrupts. Set this bit to '0' to enable FIFO interrupts.
1	disempt	Set this bit to '1' to reset the dleempty bit in the HRFSR register, clear the pending interrupt, and disable future 6 ms transmit frame interrupts. Set this bit to '0' to enable 6 ms transmit frame interrupts.
0	syncstuff	1 = disable automatic stuffing bit insertion and force stuffing bit insertion every other frame. 0 = enable automatic stuffing bit insertion based upon the transmit FIFO water level.

Table 16: Transmit Test Control Register, HTFTCR, R/W, Address = A4h, Default = 00h

Bit	Name	Description
7:3	rs	Reserved. Must be set to '0' when written.
2	disw_d	1 = disable writes to the transmit FIFO. The FIFO contents will be retransmitted every 80 bits. 0 = enable writes to the transmit FIFO for normal operation.
1	crc_er	Set this bit to '1' to force transmission of a corrupt CRC in one frame. This bit is automatically cleared.
0	fsw_er	Set this bit to '1' to force transmission of a corrupt frame sync word (FSW) in one frame. This bit is automatically cleared.

Table 17: Transmit Data Byte Selection Register, HTFBSR, R/W, Address = A5h, Default = 00

Bit	Name	Description
7:6	rs	Reserved. Must be set to '0' when written.
5:0	htfbsr	Timeslot monitor select register. This register selects a pair of T1 payload timeslot to be monitored using the HTFRSRH and HTFRSRL registers. This feature provides a mechanism to monitor outgoing transmit data which may be used for detecting T1 in-band loopback codes. The processor must wait one frame time after updating [htfbsr] before reading the HTFRSR and HTFRSRL registers.

Table 18: Data Read Sample (High) Register, HTFRSRH, R, Address = A6h

Bit	Name	Description
7:0	htfrsrh	Data read sample register, High. Contains the data byte in the time slot specified in the HTFBRSR register. Contents are updated when [htfbsr] is updated.

Table 19: Data Read Sample (Low) Register, HTFRSRL, R, Address = A7h

Bit	Name	Description
7:0	htfrsrl	Data read sample register, Low. Contains the data byte from the timeslot following the time slot specified in the HTFBRSR register. Contents are updated when [htfbsr] is updated.

Table 20: Transmit Frame Control Register, HTFTMR, R/W, Address = A8h, Default = 00h

Bit	Name	Description
7	tser_nml	0 = send all 1's or all 0's over the HDSL2 overhead channel. All 1's is selected when send_state=1, and all 0's is selected when send_state=0. (See Table 21) 1 = send normal HDSL2 overhead data.
6	descram_lt	1 = select H2TU-R to H2TU-C descrambler polynomial. 0 = select H2TU-C to H2TU-R descrambler polynomial.
5	descram_en	1 = enable the descrambler. 0 = disable the descrambler.
4	scram_nt	1 = select H2TU-R to H2TU-C scrambler polynomial. 0 = select H2TU-C to H2TU-R scrambler polynomial.
3	scram_en	1 = enable the scrambler. 0 = disable the scrambler.
2	frame_inh	1 = send all 1's or all 0's frame sync word. (See Table 21). 0 = transmit normal frame sync word.
1	send_state	This bit selects between all 1's or all 0's patterns for insertion into the payload and HDSL2 overhead channel in conjunction with the send_nml and tser_nml bits. (See Table 21) 1 = all 1's is selected. 0 = all 0's is selected.
0	send_nml	1 = send all 1's on the HDSL2 payload when send_state=1. Send all 0's on the HDSL2 payload when send_state=0. 0 = send normal HDSL2 payload data, overhead data and frame sync word. (See Table 21)

Table 21: All 1's / 0's Control

send_nml	frame_inh	tser_nml	Frame Sync Word and Stuff Bits	other HDSL2 overhead	payload data
0	don't care	don't care	normal	normal	normal
1	0	1	normal	normal	send_state
1	0	0	normal	send_state	send_state
1	1	don't care	send_state	send_state	send_state

Table 22: Transmit Sync Word (First 8 bits), HTFFSW1, R/W, Address = A9h Default = 00h

Bit	Name	Description
7:0	htfsw1	First 8 bits of the Frame Sync Word (FSW). Bit 7 is the first bit of the FSW.

Table 23: Transmit Sync Word (Last 2 bits), HTFFSW2, R/W, Address = AAh Default = 00h

Bit	Name	Description
7:2	rs	Reserved. Must be set to '0' when written.
1:0	htfs21	Last two bits of the Frame Sync Word (FSW). Bit 0 is the last bit of the FSW.

Table 24: Transmit Z Bit Register 1, HTFZB1, R/W, Address = ABh, Default = 00h

Bit	Name	Description
7:0	htfzb1	Transmit Z-bits 1-8 (N x 64 kbps payload mode).

Table 25: Transmit Z Bit Register 2, HTFZB2, R/W, Address = ACh, Default = 00h

Bit	Name	Description
7:0	htfzb2	Transmit Z-bits 9-16 (N x 64 kbps payload mode).

Table 26: Transmit Z Bit Register 3, HTFZB3, R/W, Address = ADh, Default = 00h

Bit	Name	Description
7:0	htfzb3	Transmit Z-bits 17-24 (N x 64 kbps payload mode).

Table 27: Transmit Z Bit Register 4, HTFZB4, R/W, Address = AEh, Default = 00h

Bit	Name	Description
7:0	htfzb4	Transmit Z-bits 25-32 (N x 64 kbps payload mode).

Table 28: Transmit Z Bit Register 5, HTFZB5, R/W, Address = AFh, Default = 00h

Bit	Name	Description
7:0	htfzb5	Transmit Z-bits 33-40 (N x 64 kbps payload mode).

Table 29: Transmit Z Bit Register 6, HTFZB6, R/W, Address = B0h, Default = 00h

Bit	Name	Description
7:0	htfzb6	Transmit Z-bits 41-48 (N x 64 kbps payload mode).

Table 30: HDLSL2 Transmit Overhead Register 1, HTFH0H1, R/W, Address = B1h, Default = 00h

Bit	Name	Description
7	eoc10	Transmit eoc bit 10
6	eoc8	Transmit eoc bit 8
5	eoc7	Transmit eoc bit 7
4	eoc6	Transmit eoc bit 6
3	eoc5	Transmit eoc bit 5
2	eoc4	Transmit eoc bit 4
1	eoc3	Transmit eoc bit 3
0	eoc2	Transmit eoc bit 2

Table 31: HDLSL2 Transmit Overhead Register 2, HTFH0H2, R/W, Address = B2h, Default = 00h

Bit	Name	Description
7	eoc19	Transmit eoc bit 19
6	eoc18	Transmit eoc bit 18
5	eoc16	Transmit eoc bit 16
4	eoc15	Transmit eoc bit 15
3	eoc14	Transmit eoc bit 14
2	eoc13	Transmit eoc bit 13
1	eoc12	Transmit eoc bit 12
0	eoc11	Transmit eoc bit 11

Table 32: HDLSL2 Transmit Overhead Register 3, HTFH0H3, R/W, Address = B3h, Default = 00h

Bit	Name	Description
7	uib	Transmit unspecified indicator bit
6	eoc1	Transmit eoc bit 1
5	losd	Transmit loss of signal defect bit
4	eoc24	Transmit eoc bit 24
3	eoc23	Transmit eoc bit 23
2	eoc22	Transmit eoc bit 22
1	eoc21	Transmit eoc bit 21
0	eoc20	Transmit eoc bit 20

Table 33: HDSL2 Transmit Overhead Register 4, HTFHOH4, W, Address = B4h, Default = 00h

Bit	Name	Description
7	eoc17	Transmit eoc bit 17
6	segd	Transmit segment defect bit
5	eoc9	Transmit eoc bit 9
4	sega	Transmit segment anomaly bit
3	sb1	Transmit stuff bit 1
2	sb2	Transmit stuff bit 2
1	sb3	Transmit stuff bit 3
0	sb4	Transmit stuff bit 4

HRFM Framer Receive Registers

Table 34: Receive Control Register, HRFCR, R/W, Address = C0h, Default 00h

Bit	Name	Description
7	rs	Reserved. Must be set to '0' when written.
6	up_syncdis	1 = enable automatic frame sync loss detection. 0 = frame sync loss detection performed in software.
5	ercnt_rst	1 = reset CRC error counter (HRFCRC).
4	detrst	1 = reset the detflg in the HRFSR register.
3	dettype	This bit selects whether a 64-bit all 1's or all 0's pattern is detected by detflg, HRFSR bit 6. 1 = detect all 1's. 0 = detect all 0's.
2	stuff_qual	1 = qualify the four stuff bits in the frame sync word detection algorithm. 0 = do not qualify the four stuff bits in the frame sync word detection algorithm.
1	syncrst	Set this bit to '1' then back to '0' to force the framer to reacquire receive frame alignment.
0	crdet	This bit should be set to '1' to reset the fsevent and fsdet bits in the HRFSR register, clear the pending interrupt and prevent future 6ms receive frame interrupts. This bit should be set to '0' again to enable the 6ms receive frame interrupt.

Table 35: Receive Test Control Register, HRFTCR, R/W, Address = C1h, Default = 00h

Bit	Name	Description
7:3	rs	Reserved. Must be set to '0' when written.
2	dis_cnt	1 = disable the DS1 counter for 8 RCLK cycles. Not latched. 0 = enable the DS1 counter for normal operation.
1	diswr_m	1 = disable writes to the receive FIFO. 0 = enable writes to the receive FIFO for normal operation.
0	rs	Reserved. Must be set to '0' when written.

HRFM Receive FIFO Water Level

The receive FIFO water level is defined as the difference between the write and read pointers. The value in HRFWL and its rate of change provide an indication of the difference between the actual receive payload data rate and the rate data is clocked out of the device using RCLK. The RCLK frequency is adjusted to match the receive payload data rate by reading the FIFO water level at every 6 ms receive frame interrupt. With this information, the RCLK frequency is then adjusted to maintain the FIFO near the ideal water level.

Table 36: HRFWL Register, R, Address = C2h

Bit	Name	Description
7:0	hrfwl	Receive channel FIFO water level. The value in this register ranges between 0 to 120 and the receive FIFO is 60 bits deep. A register value of 60 corresponds to a FIFO water level of 30 bits which is the optimum average water level.

Table 37: FIFO Depth Register, HRFFDR, R, Address = C3h

Bit	Name	Description
7	sbid1	Stuff indicator bit 1. This bit is updated every 6 ms receive frame interrupt. 1 = long frame 0 = short frame
6	sbid2	Stuff indicator bit 2. This bit is updated every 6 ms receive frame interrupt. 1 = long frame 0 = short frame
5	misaligned_rx	This bit is set to '1' when receive FIFO data is misaligned or has a parity error.
4	misaligned_tx	This bit is set to '1' when transmit FIFO data is misaligned or has a parity error.
3	underflow_rx	This bit is set to '1' when there is a receive FIFO underflow.
2	overflow_rx	This bit is set to '1' when there is a receive FIFO overflow.
1	underflow_tx	This bit is set to '1' when there is a transmit FIFO underflow.
0	overflow_tx	This bit is set to '1' when there is a transmit FIFO overflow.

Table 38: Receive Status Register, HRFSR Register, R, Address = C4h

Bit	Name	Description
7	rs	Reserved.
6	detflg	This bit is set to '1' when the last 64 bits meet the criteria set up by dettype in HRFCR.
5	rs	Reserved.
4	crcerr	This bit is set to '0' when a CRC error has been detected.
3	fcsync	This bit is set to '1' when the receive framer establishes frame synchronization. Frame sync is declared automatically after detection of two frames with correct frame sync and stuff id bits (and stuff bits when HRFCR bit 2 is set to '1'). When HRFCR bit 6 is set to '1', fcsync will be automatically set to '0' upon loss of frame synchronization after receiving 5 consecutive frames with framing bit errors. When HRFCR bit 6 is set to '0', the processor must detect frames with framing bit errors and force the framer to reacquire frame alignment.
2	fsdet	This bit is set to '1' when all framing bits in the current frame are correct and should be read during the 6 ms receive frame interrupt service routine (indicated by fsevent=1).
1	fsevent	This bit transitions from '0' to '1' to indicate a 6ms receive frame sync interrupt. When this interrupt occurs, fsdet is updated to indicate whether there are framing bit errors in the current frame. The fsevent bit and the pending interrupt are cleared when HRFCR bit 0 is set to '1'.
0	dlempty	This bit transitions from '0' to '1' to indicate a 6ms transmit frame interrupt. When this interrupt occurs, the transmit overhead registers (and Z-bit registers in N x 64k mode) should be loaded with new data. The dlempty bit and the pending interrupt are cleared when HTFCR bit 1 is set to '1'.

Table 39: Receive Timing & Loopback Register, HRFTTCR, R/W, Address = C5h, Default = 00h

Bit	Name	Description
7:6	rs	Reserved. Must be set to '0' when written.
5	bpfrm	1 = bypass the framer/mapper. 0 = enable the framer/mapper.
4	hloop	1 = loop the framer/mapper output back to the framer/mapper input. 0 = disable the framer/mapper loopback for normal operation.
3	rlb	1 = enable remote loopback (RSER to TSER, RFSYNC to TFSYNC, and RCLK to TCLK) 0 = disable the remote loopback for normal operation.
2	llb_clk	1 = enable the clock local loopback (TCLK to RCLK) 0 = disable the clock local loopback for normal operation.
1	llb	1 = enable the data local loopback (TSER to RSER and TFSYNC to RFSYNC) 0 = disable the data local loopback for normal operation.
0	tclk_disbl	1 = disable the RCLK output. 0 = enable the RCLK output for normal operation.

HRFM PLL Synthesizer Registers

The SK70742 has an internal digital phase lock loop (DPLL) synthesizer that generates a receive clock at the payload data rate. Figure 15 is a block diagram of the PLL circuit. Three variables are necessary to set the PLL to the required line rate. “ α ” is the phase adjustment variable and is set in the associated HRFPAJ register. “ β ” is the NCO clock division ratio variable and is set in the HRFPAJ register. CW is a 16 bit control word that is set in the HRFNCR1 and HRFNCR2 registers. Table 44 lists typical settings for these variables for different line rates.

Table 40: NCO Control Register (MSB), HRFNCR1, R/W, Address = C6h, Default = 17h

Bit	Name	Description
7:0	hrfnrc1[7:0]	NCO control register MSBs. High byte of 16 bit signed value; transferred to the NCO accumulator when high byte is written.

Table 41: NCO Control Register (LSB), HRFNCR2, R/W, Address = C7h, Default = 5Ah

Bit	Name	Description
7:0	hrfnrc2[7:0]	NCO control register LSBs. Low byte of 16 bit signed value; transferred to the NCO accumulator when high byte is written.

Table 42: DPLL Clock Division Ratio, HRFPAJ, R/W, Address = CBh, Default = 15h

Bit	Name	Description
7:6	rs	Reserved. Must be set to '0' when written.
5:0	beta	NCO clock division ratio, beta.

Table 43: DPLL Phase Adjustment Register, HRFPAJ, R/W, Address = CAh, Default = 2Ch

Bit	Name	Description
7:6	rs	Reserved. Must be set to '0' when written.
5:0	hrfpaj	Phase adjustment parameters. This register holds values for alpha up to 63.

Figure 15: RCLK Generation Circuit

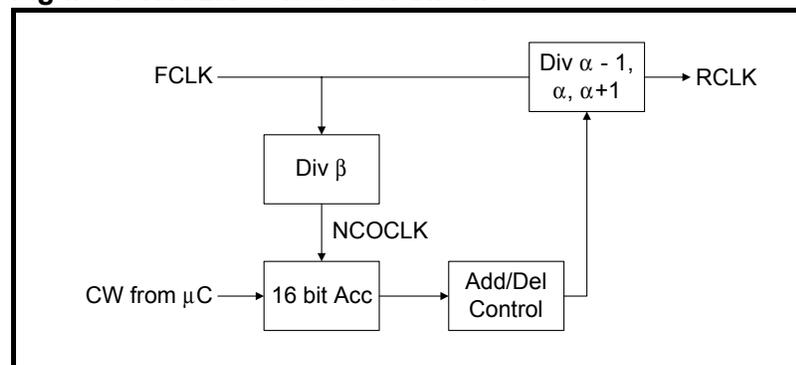


Table 44: PLL Settings for Common Line Rates

Payload Time Slots	HDSL2 Line Rate (kbps)	Payload Rate (kbps)	Phase Adjustment Variable (α)	NCO Clock Divider Variable (β)	Control Word (MSB) HRFNCR1	Control Word (LSB) HRFNCR2
12	784	768	2Ch	15h	78h	2Eh
14	912	896	2Ch	15h	67h	50h
16	1040	1024	2Ch	15h	5Ah	9Ah
18	1168	1152	2Ch	15h	50h	ACh
24	1552	1536	2Ch	15h	3Ch	B7h
24	1552	1544	2Ch	15h	1Eh	5Ah
32	2064	2048	2Ch	15h	20h	A9h

HRFM CRC Counter Register

Table 45: CRC Counter Register, HRFNCR, R, Address = C9h

Bit	Name	Description
7:0	hrfcrc	CRC error counter. The counter saturates at FFh and is reset with ercnt_rst in HRFNCR.

HRFM Receive Overhead Registers

Table 46: Receive Z Bit Register 1, HRFZB1, R, Address = CCh

Bit	Name	Description
7:0	hrfzb1	Receive Z-bits 1-8 (N x 64 kbps payload mode).

Table 47: Receive Z Bit Register 2, HRFZB2, R, Address = CDh

Bit	Name	Description
7:0	hrfzb2	Receive Z-bits 9-16 (N x 64 kbps payload mode).

Table 48: Receive Z Bit Register 3, HRFZB3, R, Address = CEh

Bit	Name	Description
7:0	hrfzb3	Receive Z-bits 17-24 (N x 64 kbps payload mode).

Table 49: Receive Z Bit Register 4, HRFZB4, R, Address = CFh

Bit	Name	Description
7:0	hrfzb4	Receive Z-bits 25-32 (N x 64 kbps payload mode).

Table 50: Receive Z Bit Register 5, HRFZB5, R, Address = D0h

Bit	Name	Description
7:0	hrfzb5	Receive Z-bits 33-40 (N x 64 kbps payload mode).

Table 51: Receive Z Bit Register 6, HRFZB6, R, Address = D1h

Bit	Name	Description
7:0	hrfzb6	Receive Z-bits 41-48 (N x 64 kbps payload mode).

Table 52: HDLSL2 Receive Overhead Register 1, HRFHOH1, R, Address = D2h

Bit	Name	Description
7	eoc10	Receive eoc bit 10
6	eoc8	Receive eoc bit 8
5	eoc7	Receive eoc bit 7
4	eoc6	Receive eoc bit 6
3	eoc5	Receive eoc bit 5
2	eoc4	Receive eoc bit 4
1	eoc3	Receive eoc bit 3
0	eoc2	Receive eoc bit 2

Table 53: HDLSL2 Receive Overhead Register 2, HRFHOH2, R, Address = D3h

Bit	Name	Description
7	eoc19	Receive eoc bit 19
6	eoc18	Receive eoc bit 18
5	eoc16	Receive eoc bit 16
4	eoc15	Receive eoc bit 15
3	eoc14	Receive eoc bit 14
2	eoc13	Receive eoc bit 13
1	eoc12	Receive eoc bit 12
0	eoc11	Receive eoc bit 11

Table 54: HDLSL2 Receive Overhead Register 3, HRFHOH3, R, Address = D4h

Bit	Name	Description
7	uib	Receive unspecified indicator bit
6	eoc1	Receive eoc bit 1
5	losd	Receive loss of signal defect bit
4	eoc24	Receive eoc bit 24
3	eoc23	Receive eoc bit 23
2	eoc22	Receive eoc bit 22
1	eoc21	Receive eoc bit 21
0	eoc20	Receive eoc bit 20

Table 55: HDLSL2 Receive Overhead Register 4, HRFHOH4, R, Address = D5h

Bit	Name	Description
7	eoc17	Receive eoc bit 17
6	segd	Receive segment defect bit
5	eoc9	Receive eoc bit 9
4	sega	Receive segment anomaly bit
3	sb1	Receive stuff bit 1
2	sb2	Receive stuff bit 2
1	sb3	Receive stuff bit 3
0	sb4	Receive stuff bit 4

JTAG Control Register

Table 56: JTAG Control Register, TJCR, R/W, Address = E0h, Default = DFh

Bit	Name	Description
7	rs	Reserved. Must be set to '0' when written.
6	mmode	Set mmode = 1 to reset all memory blocks in normal mode. Set mmode = 0 to set all memory blocks to access mode.
5	pllt	Test control bit for the PLL. Reset to '0' by asserting the $\overline{\text{RST}}$ pin low.
4:3	pllf	f control bits for the PLL in the clock multiplier (0 through 3); Resets to all 1's.
2:0	plld	Control the divide ratio (m) of the PLL. Reset to all 1's.

TEST SPECIFICATIONS

NOTE

Tables 57 through 64 and Figures 16 through 20 represent the performance specifications of the SK70742 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Tables 59 through 64 are guaranteed over the recommended operating conditions specified in [Table 58](#).

Table 57: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage ¹ (reference to ground ²)	VCC1, VCC2, VCC3, VCC4, VCC5, VCC_PLL, VCC_CK	-0.3	+4.0	V
Input voltage ² , any input pin	–	- 0.3	5.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	T _{STOR}	-65	+150	°C
CAUTION				
<p>Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.</p>				
<p>1. The maximum potential between any VCC pins must never exceed ±0.3 V. 2. All Ground pins must be kept at 0 V.</p>				

Table 58: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
DC supply ¹ (reference to ground ^{2,3})	VCC1, VCC2, VCC3, VCC4, VCC5, VCC_PLL, VCC_CK	3.14	3.30	3.46	V
Ambient operating temperature	T _A	-40		+85	°C
<p>1. The maximum potential between any VCC pins must never exceed ±0.3 V. 2. Differential voltage between any Ground pin must be less than 0.3 V. 3. All Ground pins must be kept at 0 V.</p>					

Table 59: DC Electrical Characteristics

Parameter	Sym	Min	Typ ¹	Max	Unit	Test Conditions
Supply current	ICC	–	60	65	mA	
Input Low voltage	VIL	–	–	0.8	V	
Input High voltage	VIH	2.0	–	–	V	
Output Low voltage	VOL	–	–	GND +0.3	V	I _{OUT} = 1.6 mA
Output High voltage	VOH	2.4	–	–	V	I _{OUT} = 400 μA
Input leakage current ²	IIL	–	–	±10	μA	0 < V _{IN} < V _{CC}
Tristate leakage current ³	ITOL	–	–	±30	μA	0 < V < V _{CC}
Input capacitance (individual pins)	CIN	–	12	–	pF	
Load capacitance Data and Transceiver outputs.	CLREF	–	15	–	pF	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to pins AD0 through AD7 when configured as inputs.
3. Applies to pins AD0 through AD7 when tristated.

Table 60: Data Interface Timing Specifications (See Figure 16)

Parameter	Symbol	Min	Typ ¹	Max	Unit
TCLK, RCLK frequency (PLRATE =24)	–	–	1.544	–	MHz
TCLK Duty Cycle	–	40	–	60	%
TFSYNC pulse width	T _{TFS}	–	1/f _{TCLK}	–	ns
RFSYNC pulse width	T _{RFS}	–	1/f _{RCLK}	–	ns
TSER setup time to TCLK falling edge	T _{DS}	10	–	–	ns
TSER hold time from TCLK falling edge	T _{DH}	20	–	–	ns
RSER delay from RCLK rising edge	T _{RD}	–	–	10	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 16: Data Interface Relative Timing for T1 Transport Mode

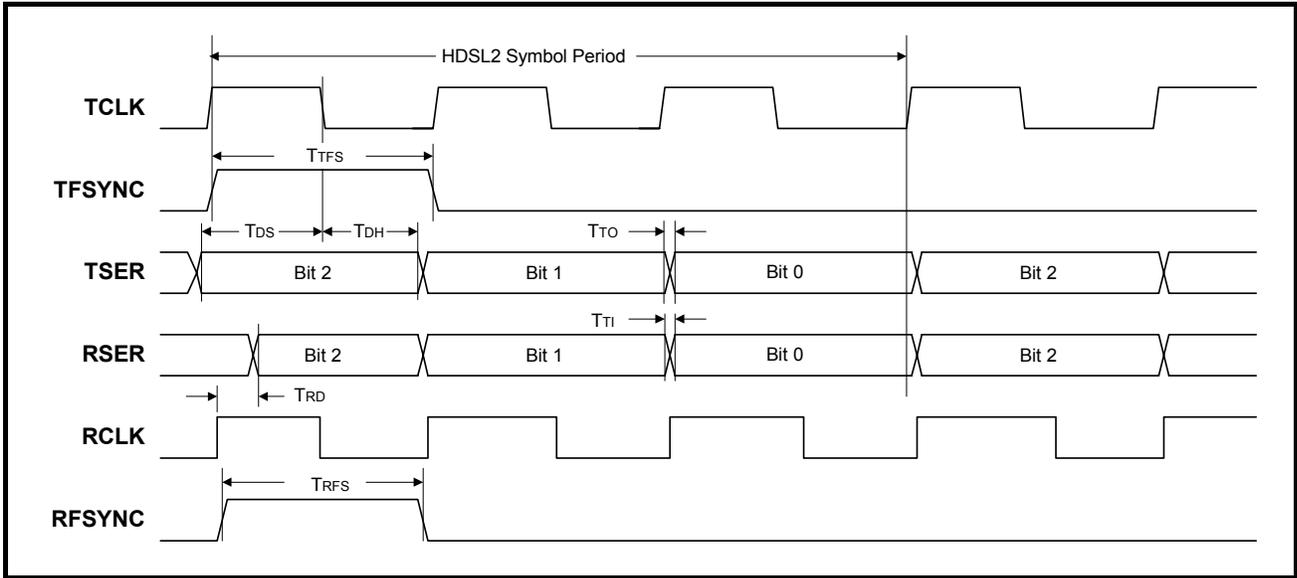


Table 61: Framer Bypass Mode Timing Specifications (See Figure 17)

Parameter	Symbol	Min	Typ ¹	Max	Unit
HBCLK frequency ² (PLRATE = 24)	–	–	1.552	–	MHz
HSCLK pulse width	TFSW	–	1/f _{HBCLK}	–	ns
TSER setup time to HBCLK falling edge	TVDS	10	–	–	ns
TSER hold time from HBCLK falling edge	TDH	20	–	–	ns
RSER delay from HBCLK rising edge	TRD	–	–	10	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
 2. HBCLK is 3X the symbol rate.

Figure 17: Data Interface Relative Timing for Framer Bypass Mode

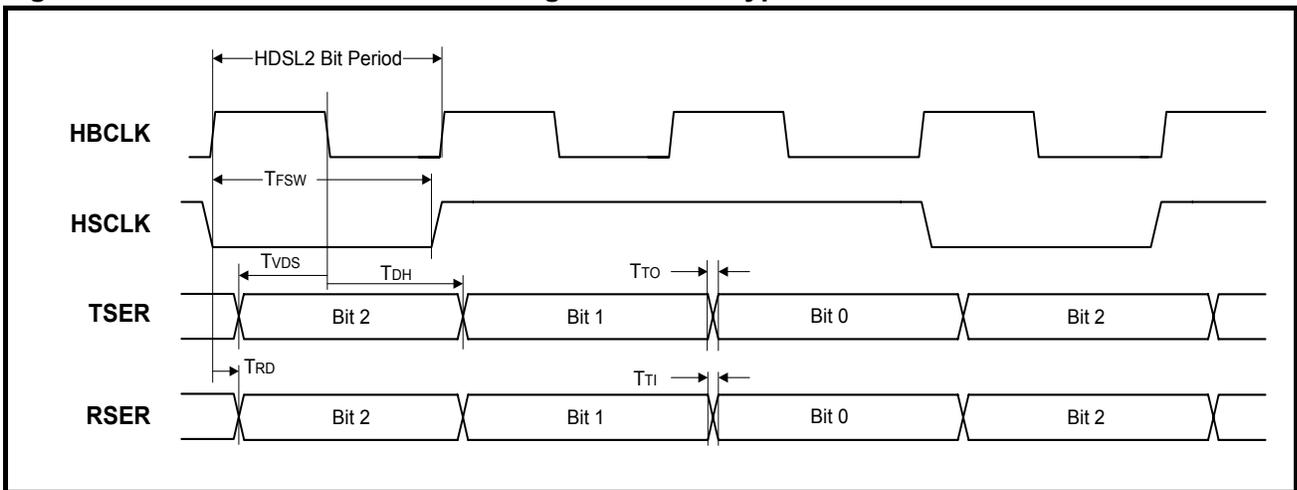


Table 62: Transceiver Interface Timing Specification (See Figure 18)

Parameter	Sym	Min	Typ ¹	Max	Unit	Test Conditions
FCLK frequency	–	–	baud rate x 33	–	MHz	See Note 2
FEC_RX setup time to FCLK falling edge	TTS	30	–	–	ns	
FEC_RX hold time from FCLK falling edge	TTH	+5	–	–	ns	
FEC_TX delay from FCLK rising edge	TCD	-3	–	15	ns	
FCE falling edge from FCLK falling edge	TCE	3	–	–	ns	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
 2. Measured with 15 pF load.

Figure 18: Transceiver Interface Relative Timing

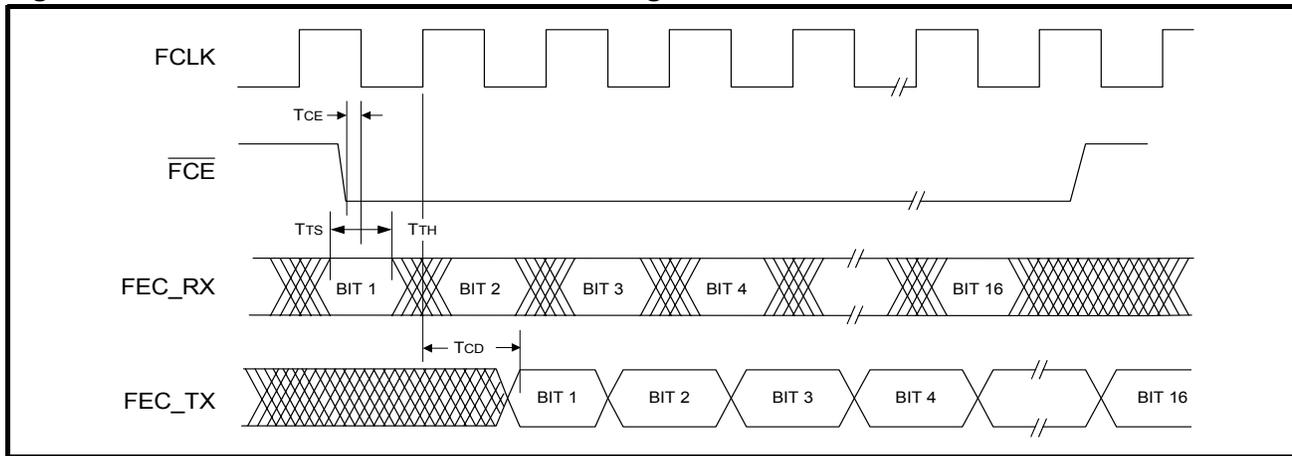


Figure 19: Input Jitter Tolerance and Output Jitter, T1

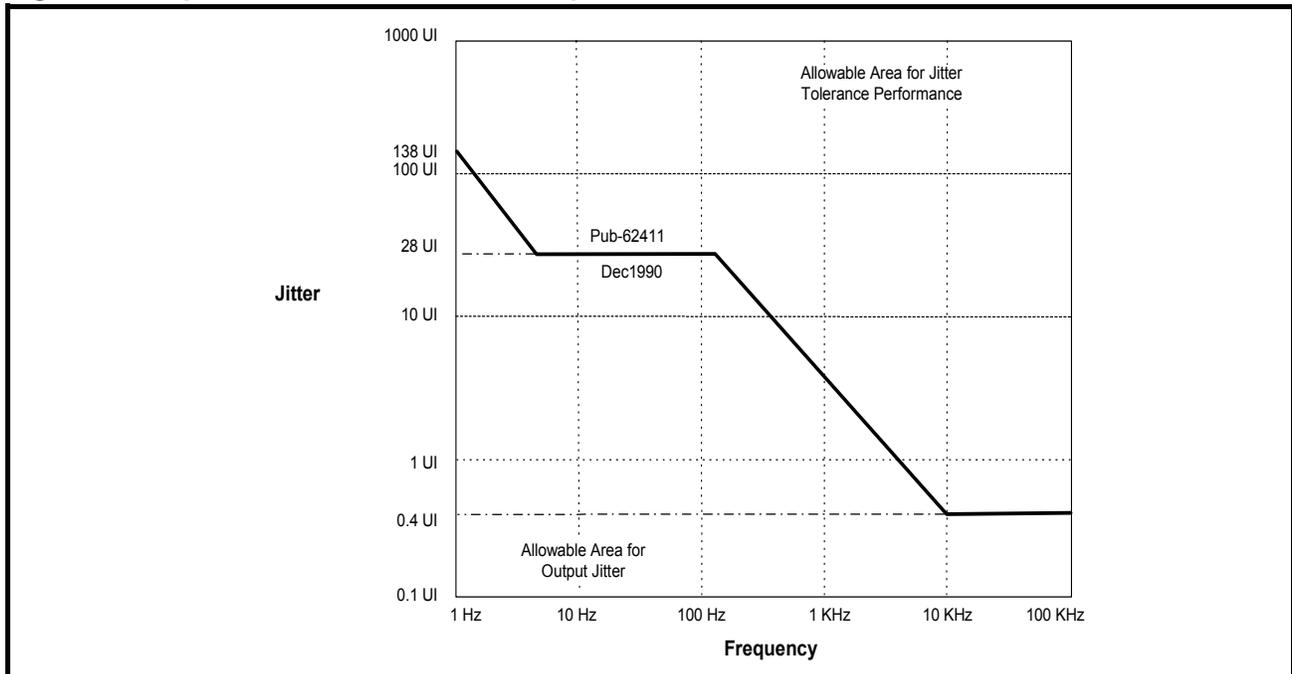


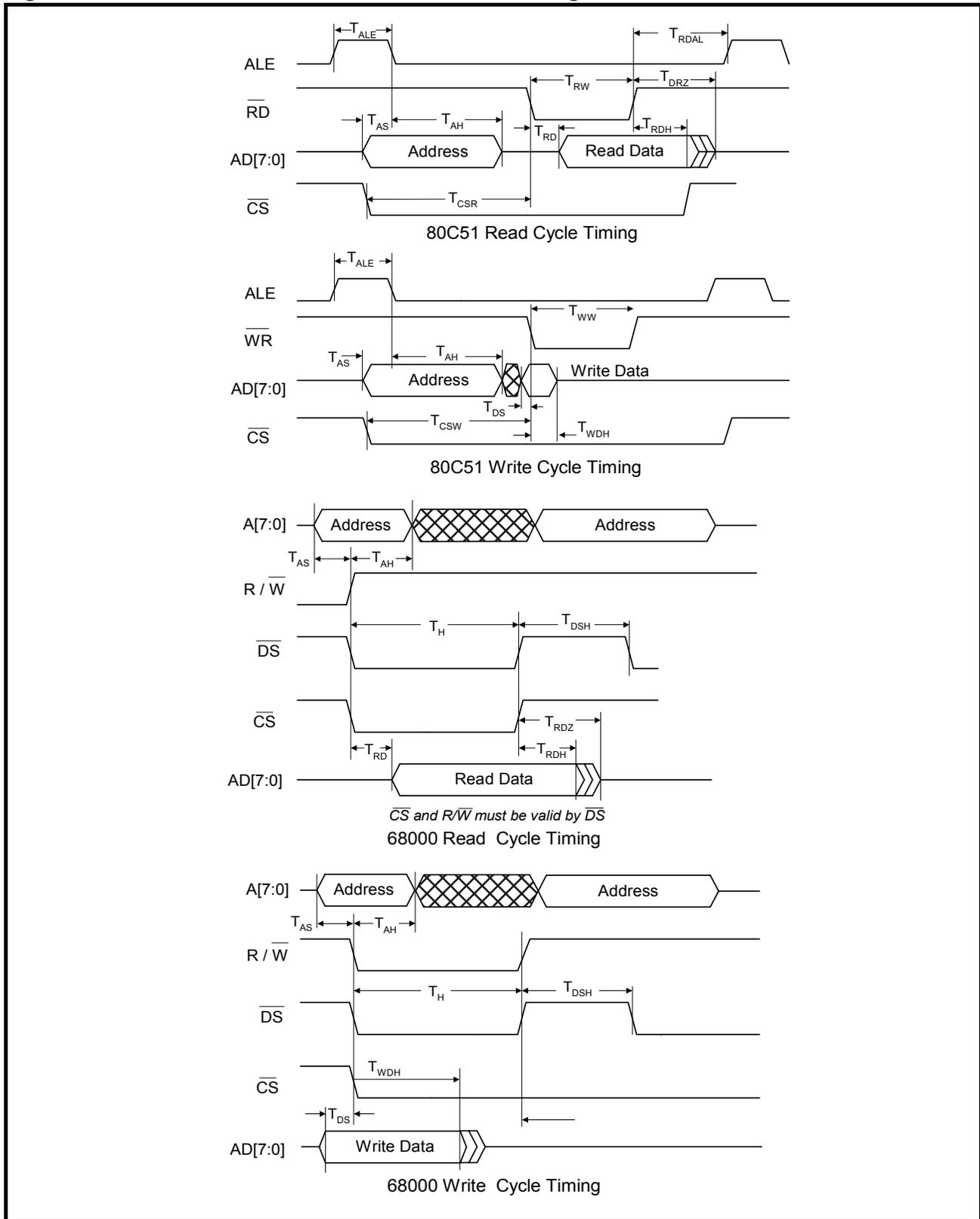
Table 63: Intel Bus Parallel I/O Timing Characteristics (See Figure 20)

Parameter	Sym	Min	Max	Units	Test Conditions
ALE pulse width	TALE	10	–	ns	
Address valid to ALE falling edge setup time	TAS	10	–	ns	
ALE falling edge to address hold time	TAH	10	–	ns	
\overline{CS} falling edge to \overline{RD} falling edge	TCSR	40	–	ns	
\overline{CS} falling edge to \overline{WR} falling edge	TCSW	40	–	ns	
\overline{RD} Low pulse width	TRW	80	–	ns	
\overline{RD} falling edge to data valid	TRD	–	80	ns	
Data high impedance after \overline{RD} rising edge	TDRZ	–	30	ns	
\overline{WR} Low pulse width	TWW	80	–	ns	
Data setup time before \overline{WR} falling edge	TDS	10	–	ns	
Read data hold time after \overline{RD} rising edge	TRDH	0	–	ns	
Write data hold time after \overline{WR} falling edge	TWDH	10	–	ns	
\overline{RD} rising edge to ALE rising edge	TRDAL	40	–	ns	

Table 64: Motorola Bus Parallel I/O Timing Characteristics (See Figure 20)

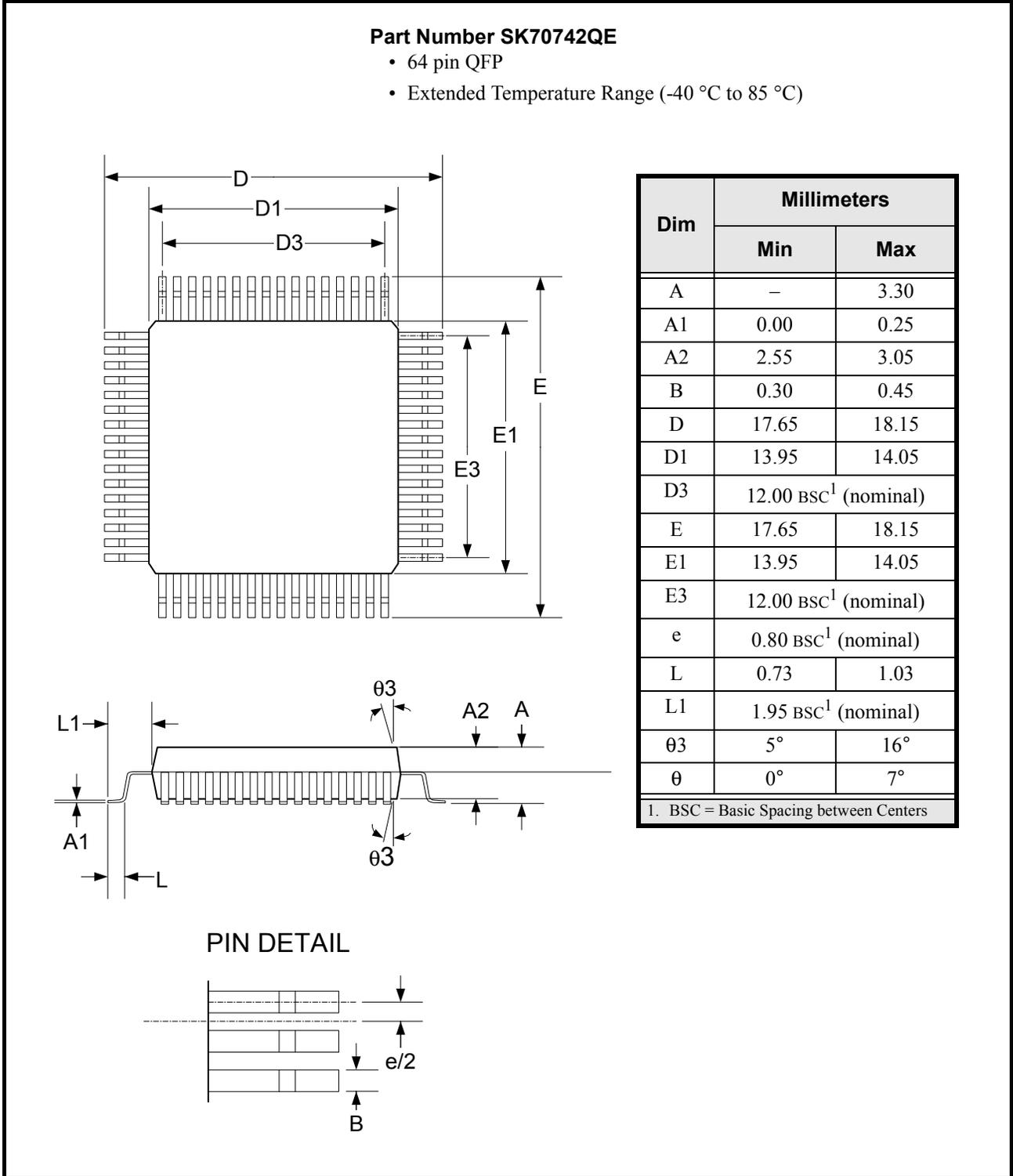
Parameter	Symbol	Min	Max	Units	Test Conditions
\overline{DS} Low pulse width	TH	130	–	ns	
Read data valid time after \overline{DS} rising edge	TRDH	0	–	ns	
\overline{DS} falling edge to write data hold time	TWDH	5	–	ns	
Valid address to \overline{DS} falling edge	TAS	10	–	ns	
\overline{DS} falling edge to valid address hold time	TAH	10	–	ns	
Data setup time before \overline{DS} falling edge	TDS	10	–	ns	
\overline{DS} falling edge to valid Data	TRD	–	120	ns	
Data high impedance after \overline{CS} or \overline{DS} are asserted High	TRDZ	–	40	ns	
Required High time of \overline{DS}	TDSH	60	–	ns	

Figure 20: Parallel Microcontroller Bus Interface Timing



MECHANICAL SPECIFICATIONS

Figure 21: Quad Flat Pack



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2.3	03/2000	Update ANSI standard references, update register definitions, minor editorial changes.
2.2	10/99	Minor typographical errors

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5,204,880; 5,249,183; 5,257,286; 5,267,269; 5,267,746; 5,461,661; 5,493,243; 5,534,863; 5,574,726; 5,581,585; 5,608,341; 5,671,249; 5,666,129; 5,701,099