# S44233 A-Law Asynchronous Codec

February 1993

## Single Chip Codecs With Filters

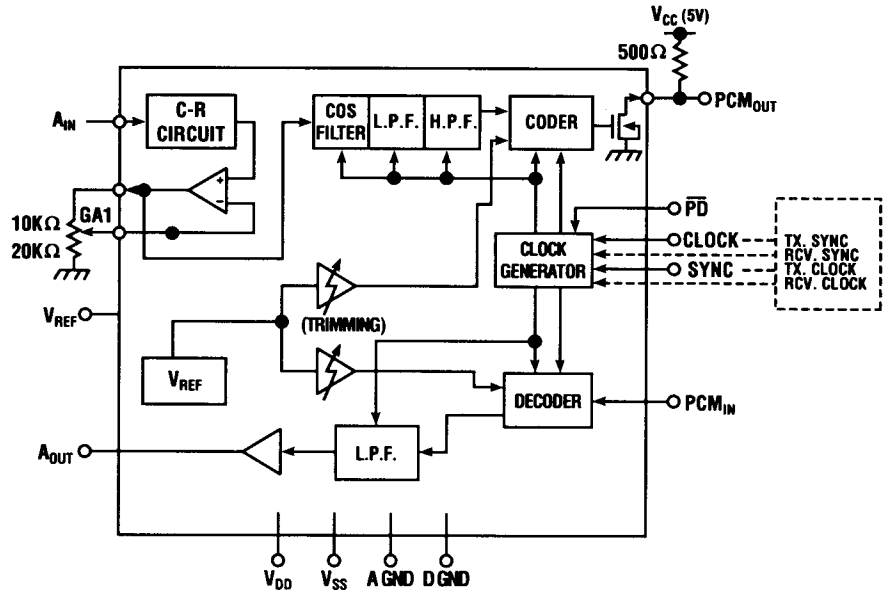
## Features

- Exceeds AT&T D3, CCITT G.711, G.712, and G.733 Specifications
- Available with A-Law Signal Companders
- Input Op Amp for Gain Adjustment and Anti-aliasing Filtering
- Asynchronous Operation for 2048/1544/1536 kHz PCM Data Rates
- Auto-Zero Circuitry Requires No External Components
- Energy Saving Power Down Mode

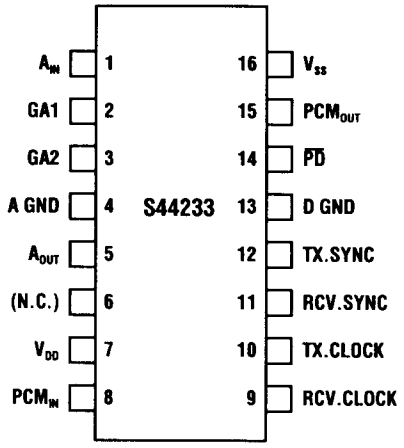
## General Description

The S44233 is a high quality monolithic CMOS Codec suitable for use in telephone central offices and PBXs. This codec provides the interface between the analog signals of the subscriber loop and the digital signals of the PCM high ways in telephone switching systems. This codec contains band-limiting filters, the A/D and D/A conversion circuits, and the PCM encoder/decoder. The S44233 conforms to European A-Law signal companding characteristics.

### Functional Block Diagram




### Pin Configuration



### Pin Function Description

| Pin Name | Number | Function |
|---|---|---|
| $A_{IN}$ | 1 | These three pins make up the basic analog input section. $A_{IN}$ is the Analog Input pin and GA1/GA2 are the Gain Adjustment and Gain Adjustment feedback pins. The maximum input to the analog section is $+V_{REF}$ and the minimum input is $-V_{REF}$ where $V_{REF}$ is approximately 2 to 3 volts. The operational amplifier may be tied directly to provide a unity gain input or it may be configured for negative feedback to facilitate system calibration. When configured for negative feedback, the load on the op amp should be less than 100pF with approximately 10K to 20K ohms of resistance. |
| GA1 | 2 | |
| GA2 | 3 | |
| $A_{GND}$ | 4 | Analog Ground should be separate from digital ground in order to minimize crosstalk and noise. |
| $A_{OUT}$ | 5 | Analog Out is the smoothed output from the low pass filter after it has been decoded from the PCM input. For minimum distortion, pin 5 should be loaded with at least 3K ohms and no more than 100pF. |
| NC | 6 | No connect. |
| $V_{DD}$ | 7 | Positive supply voltage. Normally +5 volts. |
| $D_{GND}$ | 13 | Digital Ground reference point for digital input signals. Normally connected to ground. |
| $\overline{PD}$ | 14 | Power Down Mode. The power down mode will be activated when this TTL compatible input is held low even if the SYNC lines continue to strobe. The chip will also power down if the SYNCs stop strobing. The strobes can be either high, low, or floating, but as long as they are static, the power mode is in effect. |
| $PCM_{OUT}$ | 15 | PCM out is the output of the PCM encoder filtering and the A-D conversion. This is a LS-TTL compatible open-drain output. It is active only during transmission of digital PCM output for 8 bit periods of the transmit clock signal following a positive edge on the transmit SYNC input. Data is clocked out by the positive edge of the transmit clock. This pin should have a pull up to $V_{DD}$ of approximately 500 ohms, although only one 500 ohm resistor is required for eight codecs. |
| $V_{SS}$ | 16 | Negative supply voltage. Normally -5 volts. |
| $PCM_{IN}$ | 8 | This is a TTL compatible input for supplying digital PCM data to the codec decoder for conversion into analog form. The PCM data is clocked in by the negative edge of the receive (RCV) clock. |
| TX.CLK | 9 | TX.CLK/Transmit clock, RCV.CLK/Receive Clock |
| RCV.CLK | 10 | Any one of three different clock frequencies (1.536 MHz, 1.544 MHz, and 2.048 MHz) will be accepted by this pin. The input clock frequency will automatically be divided down to provide all the necessary internal clocks.<br>The TX.CLK shifts PCM data out of the coder on the positive going edge and the RCV.CLK shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the TX.SYNC or RCV.SYNC input respectively. |
| RCV.SYNC | 11 | RCV.SYNC/Receive Sync, TX.SYNC/Transmit Sync |
| TX.SYNC | 12 | These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the clocking of PCM output from the coder and initiating the clocking of PCM input data into the decoder. The width of these signals is not critical. An internal bit counter generates the necessary timing for PCM output and input. |

## Absolute Maximum Rating

| Item | Rating |
|---|---|
| $V_{DD}$ | -0.3 to +6V |
| $V_{SS}$ | +0.3 to -6V |
| Storage Temperature | -55°C to 125°C |
| Power Dissipation | 0.5W |
| Digital Input Voltage | $-0.3V < V_{IN} < V_{DD} +0.3V$ |
| Analog Input Voltage | $V_{SS} -0.3V < V_{IN} < V_{DD} +0.3V$ |

## Electrical Characteristics

1) Static Characteristics ($V_{DD}$ = 5 ± 0.25V, $V_{SS}$ = -5 ± 0.25V, $V_{CC}$ = 5 ± 0.25V, $T_A$ = 0 – 70°C)

| Symbol | S44233 Pin | Descriptions | Specifications | | | | Note/Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max | Unit | |
| $I_{DD}$ | 7 | $V_{DD}$ Current (Open) | | 5.5 | 10 | mA | |
| $I_{SS}$ | 16 | $V_{SS}$ Current (Open) | -10 | -4.5 | | mA | |
| $I_{DDST}$ | 7 | $V_{DD}$ Current (Standby) | | 0.3 | 1.0 | mA | |
| $I_{SSST}$ | 16 | $V_{SS}$ Current (Standby) | -0.2 | | | mA | |
| $I_L$ | 1,2,8,<br>9,10 | Leak Current | -10.0<br>-10.0 | | 10.0<br>10.0<br>10.0 | µA<br>µA<br>µA | VM = 0.8V<br>VM = 2.0V<br>$V_{DD}$ = VM = 5.25V |
| $I_{PL}$ | 11,12 | Pull Up Current | -100 | | 0.0 | µA | |
| $I_{DL}$ | 15 | Leak Current | | | 10.0 | µA | $V_{DD}$ = VM = 5.25V |
| $C_{AIN2}$ | 1,2 | Analog Input Capacitance | | | 10 | pF | at 1MHz Vbias = 0V |
| $CD_{IN}$ | 8,9,10,<br>11,12,14 | Input Capacitance | | | 10 | pF | at 1MHz Vbias = 0V |
| $R_{OUTA}$ | 5 | $A_{OUT}$ Resistance | | 1 | 10 | Ω | |
| $R_{OUTG}$ | 3 | GA2 Resistance | | 1 | 10 | Ω | |
| $V_{GSW}$ | | GA2 Output Swing | -3.0 | | 3.0 | V | RL = 10kΩ |
| $V_{OFFIN}$ | | Analog Offset Input | -500 | | -500 | mV | Note 1 |
| $V_{OFFG}$ | | GA2 Offset Output | -50 | | 50 | mV | Note 1 |
| $V_{OFFA}$ | | $A_{OUT}$ Offset Output | -50 | | 50 | mV | $PCM_{IN}$ = +0-Code |
| $CD_{OUT}$ | 15 | $PCM_{OUT}$ Capacitance | | | 15.0 | pF | at 1MHz Vbias = 0V |
| $V_{OL}$ | 15 | $PCM_{OUT}$ Low Voltage | | | 0.4 | V | RL = 500Ω + $I_{OL}$ = 0.8mA |
| $V_{OH}$ | 15 | $PCM_{OUT}$ High Voltage | $V_{CC}$-0.3 | | | V | $I_{OH}$ = - 150µA |
| $V_{IH}$ | 10,11,<br>9,12,14 | Digital Input High Voltage | 2.0 | | | V | |
| $V_{IL}$ | 10,11,<br>9,12,14 | Digital Input Low Voltage | | | 0.8 | V | |

**NOTE:** 1. Analog Input Amplifier Gain = 0dB (GA1 is connected to GA2)

### 2) Dynamic Characteristics ($V_{DD}$ = 5 ± 0.25V, $V_{SS}$ = -5 ± 0.25V, $V_{CC}$ = 5 ± 0.25V, $T_A$ = 0 – 70°C)

| Symbol | Descriptions | Specifications | | | | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| FS | Synchronization Rate | | 8 | | kHz | |
| FC | PCM Bit Clock Rate | | 1536/1544/2048 | | kHz | |
| $t_{WC}$ | Clock Pulse Width | 200 | | | ns | |
| $t_{WSH}$ | SYNC Pulse High Width | 200 | | | ns | |
| $t_{WSL}$ | SYNC Pulse Low Width | 8 | | | µS | |
| $t_r$ | Logic Input Rise Time | | | 50 | ns | |
| $t_f$ | Logic Input Fall Time | | | 50 | ns | |
| $t_{BCS}$ | Previous Clock to SYNC Delay | 40 | | 100 | ns | Note 1 |
| $t_{cs}$ | Clock to SYNC Delay | | | 100 | ns | Note 1,3 |
| $t_{cdl}$ | Clock to $PCM_{MSB}$ Delay | | | 170 | ns | Note 1,2,4 |
| $t_{cd}$ | Clock to $PCM_{OUT}$ Delay | | | 180 | ns | Note 1,2,5 |
| $t_{su}$ | $PCM_{IN}$ Setup Time | 65 | | | ns | Note 1 |
| $t_{hd}$ | $PCM_{IN}$ Hold Time | 120 | | | ns | Note 1 |
| $t_{sd}$ | Sync to $PCM_{MSB}$ Delay | | | 170 | ns | Note 1,2,4 |

**Notes:**

1. $t_r$, $t_f$ of digital input or clock is assumed 5ns for timing measurement.
2. $PCM_{OUT}$ LOAD CONDITION: 500Ω 165 pF + two LS-TTL Equivalent ($I_{IL}$ = 0.8mA, $I_{IH}$ = -150µA) Threshold Level ($V_{OH}$ = 2.4V, $V_{OL}$ = 0.4)
3. Positive value shows SYNC delay from Clock.
4. $t_{cdl}$, $t_{sd}$ are specified by Clock or SYNC, which has slower rise time.
5. $t_{cd}$ specification is valid for the data exept MSB.

### 3) System Related Characteristics – S44233 A-Law Codec ($V_{DD}$ = 5 ± 0.25V, $V_{SS}$ = -5 ± 0.25V, $V_{CC}$ = 5 ± 0.25V, $T_A$ = 0 - 70°C, Input Amplifier Gain = 0dB, GA2 Load = 10KΩ, $A_{OUT}$ Load = 600Ω)

| Symbol | Descriptions | Test Conditions | | Specifications | | | | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Unit | |
| SDA | Signal to Dist. (A to A) | 820Hz tone | -45dBm0 | 24 | | | dB | p-wgt |
| | | | -40 | 30 | | | dB | |
| | | | -30 to + 3 | 35 | | | dB | NOTE 1 |
| SNA | Signal to Dist. (A to A) | Noise | -55 dBm0 | 14 | | | dB | |
| | | | -40 | 29 | | | dB | |
| | | | -34 | 34 | | | dB | |
| | | | -27 to -6 | 36 | | | dB | |
| | | | -3 | 28 | | | dB | |
| SDX | Signal to Dist. (A to D) | 820Hz tone | -45 dBm0 | 26 | | | dB | p-wgt |
| | | | -40 | 31 | | | dB | |
| | | | -30 to +3 | 36 | | | dB | NOTE 1 |

## 3) System Related Characteristics – S44233 A-Law Codec ($V_{DD}$ = 5 ± 0.25V, $V_{SS}$ = -5 ± 0.25V, $V_{CC}$ = 5 ± 0.25V, $T_A$ = 0 - 70°C, Input Amplifier Gain = 0dB, GA2 Load = 10KΩ, $A_{OUT}$ Load = 600Ω)

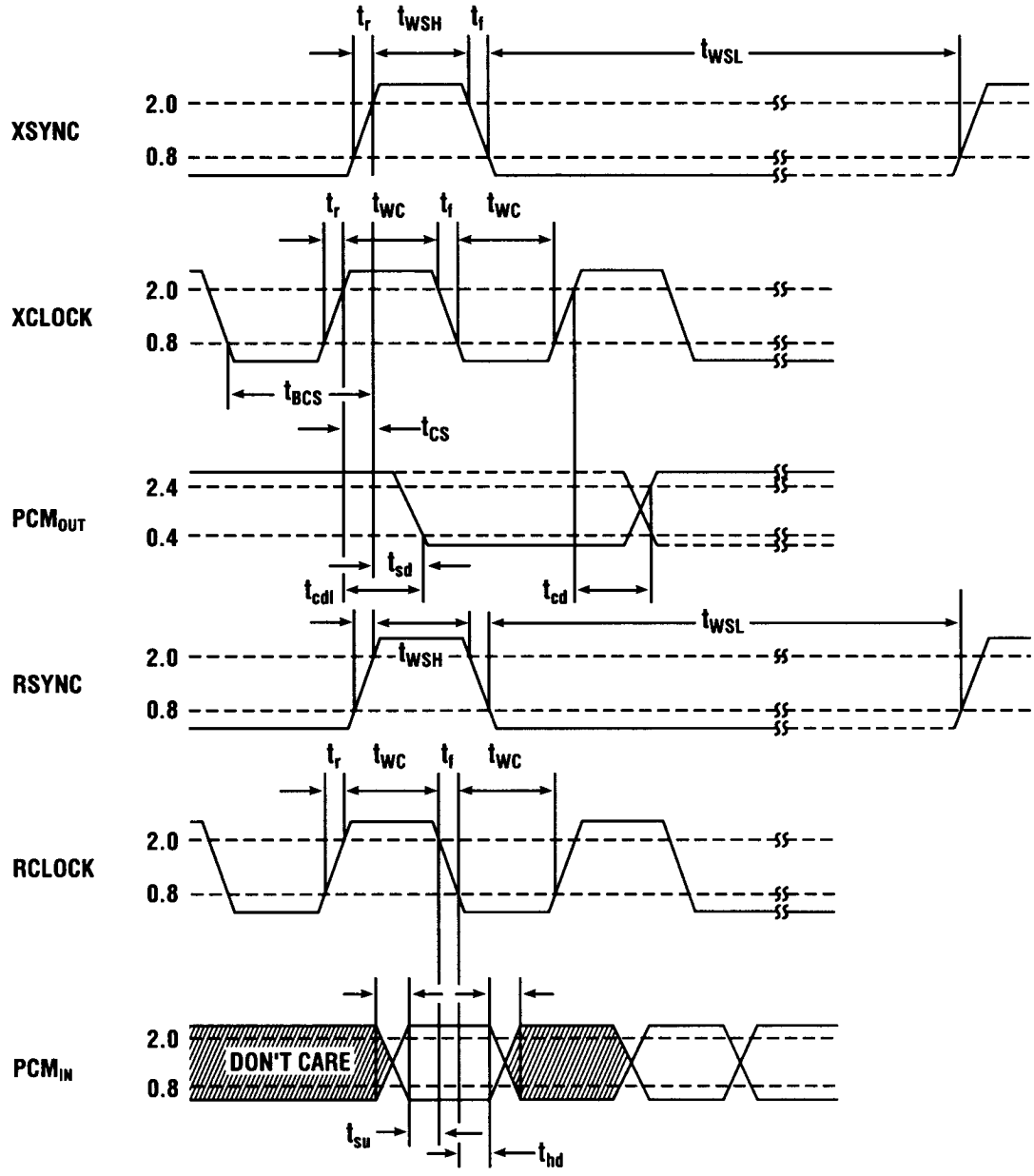
| Symbol | Descriptions | Test Conditions | | Specifications | | | | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Unit | |
| SNX | Signal to Dist. (A to D) | Noise | -55 dBm0 | 15 | | | dB | |
| | | | -40 | 30 | | | dB | |
| | | | -34 | 35 | | | dB | |
| | | | -27 to -6 | 37 | | | dB | |
| SDR | Signal to Dist. (D to A) | 820Hz tone | -45 dBm0 | 25 | | | dB | p-wgt |
| | | | -40 | 30 | | | dB | |
| | | | -30 to +3 | 35 | | | dB | NOTE 1 |
| SNR | Signal to Dist. (D to A) | Noise | -55 dBm0 | 15 | | | dB | |
| | | | -40 | 30 | | | dB | |
| | | | -34 | 35 | | | dB | |
| | | | -27 to -6 | 37 | | | dB | |
| GTA | Gain Track (A to A) | 820Hz tone | -55 to -50 dBm0 | -1.0 | | 1.0 | dB | |
| | | | -50 to -40 | -0.5 | | 0.5 | dB | |
| | | | -40 to +3 | -0.4 | | 0.3 | dB | NOTE 1 |
| GNA | Gain Track (A to A) | Noise | -60 to -55 dBm0 | -0.8 | | 0.8 | dB | |
| | | | -55 to -10 | -0.4 | | 0.4 | dB | |
| GTX | Gain Track (A to D) | 820Hz tone | -55 to -50 dBm0 | -0.8 | | 0.8 | dB | |
| | | | -50 to -40 | -0.4 | | 0.4 | dB | |
| | | | -40 to +3 | -0.2 | | 0.2 | dB | NOTE 1 |
| GNX | Gain Track (A to D) | Noise | -60 to -55 dBm0 | -0.6 | | 0.6 | dB | |
| | | | -55 to -40 | -0.4 | | 0.4 | dB | |
| | | | -40 to -10 | -0.2 | | 0.2 | dB | |
| GTR | Gain Track (D to A) | 820Hz tone | -55 to -50 dBm0 | -0.8 | | 0.8 | dB | |
| | | | -50 to -40 | -0.4 | | 0.4 | dB | |
| | | | -40 to +3 | -0.2 | | 0.2 | dB | NOTE 1 |
| GNR | Gain Track (D to A) | Noise | -60 to -55 dBm0 | -0.4 | | 0.4 | dB | |
| | | | -55 to -40 | -0.2 | | 0.2 | dB | |
| FRX | Freq. Response (A to D) (Loss) | Relative to 820Hz 0dBm0 | 0.06kHz | 24 | | | dB | NOTE 1 |
| | | | 0.2 | 0.0 | | 2.0 | | |
| | | | 0.3 to 3 | -0.15 | | 0.15 | | |
| | | | 3.18 | -0.15 | | 0.65 | | |
| | | | 3.4 | 0.0 | | 0.8 | | |
| | | | 3.78 | 6.5 | | | | |
| FRR | Freq. Response (D to A) (Loss) | Relative to 820Hz 0dBm0 | 0 to 3kHz | -0.15 | | 0.15 | dB | NOTE 1 |
| | | | 3.18 | -0.15 | | 0.65 | | |
| | | | 3.4 | 0.0 | | 0.8 | | |
| | | | 3.78 | 6.5 | | | | |
| AIL | Analog Input Level | 820Hz 0dBm0 | 25°C nom. P.S. | 1.217 | 1.231 | 1.246 | Vrms | NOTE 1 |
| AOL | Analog Output Level | 820Hz 0dBm0 | 25°C nom. P.S. | 1.217 | 1.231 | 1.246 | Vrms | NOTE 1 |

**NOTE 1:** Total variation of GAIN including the initial fluctuation temperature variation and power supply dependence (0-70°C, $V_{DD}/V_{SS}$ = ± 5V ±)

### 3) System Related Characteristics – S44233 A-Law Codec ($V_{DD}$ = 5 ± 0.25V, $V_{SS}$ = -5 ± 0.25V, $V_{CC}$ = 5 ± 0.25V, $T_A$ = 0 - 70°C, Input Amplifier Gain = 0dB, GA2 Load = 10KΩ, $A_{OUT}$ Load = 600Ω)

| Symbol | Descriptions | Test Conditions | | Specifications | | | | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Unit | |
| AT | AIL, AOL Variation with temp. | Relative to 25°C nominal P.S. | | | ±20 | | ppm/°C | |
| AP | AIL, AOL Variation with P.S. | 25°C, Supplies ±5% | | | ± 0.01 | | dB | |
| ALS | GAIN Variation over Temp. P.S. | A to D<br>D to A | INITIAL | -0.2 | | 0.2 | dB | |
| AIP | Peak Analog Input | | | 3.0 | | | V | |
| AOP | Peak Analog Output | | | 2.5 | | | V | |
| PDL | Propagation Delay | A to A | 0dBm0 | | 450 | 480 | µS | |
| DD | Delay Distortion | A to A<br>0dBm0 | 0.5 to 0.6kHz<br>0.6 to 1.0<br>1.0 to 2.6<br>2.6 to 2.8 | | | 1.4<br>0.7<br>0.2<br>1.4 | ms | rel. to min. delay |
| PSRR | PSRR | A to A<br>$A_{IN}$=$A_{GND}$<br>0.3 -50kHz | +5V +100mV op | 30 | | | dB | |
| | | | –5V +100mV op | 30 | | | | |
| ICNA | Idle Ch. Noise | A to A | $A_{IN}$ = $A_{GND}$ | | | -70 | dBm0P | A-Law |
| ICNX | Idle Ch. Noise | A to D | $A_{IN}$ = $A_{GND}$ | | | -72 | dBm0P | A-Law |
| ICNR | Idle Ch. Noise | D to A | $PCM_{IN}$=+0-CODE | | | -78 | dBm0P | A-Law |
| IM1 | Intermodulation | A to A (2a-b)<br>a;0.47kHz, -4 dBm0<br>b;0.32, -4 | | | | -38 | dBm0 | |
| IM2 | Intermodulation | A to A (a-b)<br>a;1.02kHz, -4 dBm0<br>b;0.05, -23 | | | | -52 | dBm0 | |
| ICS | Single Freq. Noise | A to A<br>$A_{IN}$ = $A_{GND}$ | 8,16,24,32, 40kHz | | | -50 | dBm0 | |
| DIS | Discrimination | A to A<br>0dBm0 | 4.6 to 200kHz | 30 | | | dB | |
| XTKA | $A_{IN}$ to $A_{OUT}$ Crosstalk | 1020Hz 0dBm0 | | | | -65 | dB | |
| XTKD | $PCM_{IN}$ to $PCM_{OUT}$ | 1020HZ 0dBm0 | | | | -65 | dB | |

## S44233 Timing Chart



# S44233 A-Law Asynchronous Codec

AMI STANDARD PRODUCTS

## Single Chip Codecs With Filters

February 1993

### Codecs Bridge the Analog/Digital Worlds

Single chip CMOS Codec Combos, with their A/D and D/A converters and all the necessary analog filtering, are a powerful tool for the systems designer. Typically, codecs have three major uses. The traditional use of a codec is as a gateway between the analog subscriber loop and the digital pathways of a central telephone office. In the newer digital PBXs, the single chip codec is found in the telephone handset itself and thus is the key in bringing out the power of voice/data integration to the latest PBX generation. The third major application of codecs is in smart instrumentation where digital signal processing is required, and the codec replaces separate A/D and D/A converters and associated filters.

### Operation

**PCM to Analog (Receive Section)**–The PCM data is shifted into the decoder's input buffer register once every sampling period. Once the PCM data has been shifted into the decoder register, a charge proportional to the received PCM data word value appears on the decoder's capacitor array. A sample and hold circuit integrates to the charge value and holds that value for the rest of the sampling period. Then a low pass switched capacitor filter smooth the signal and performs loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The low pass filter's output is then buffered and available for driving electronic hybrids directly.

**Analog to PCM (Transmit Section)**–The analog input signal is placed on the uncommitted op amp's terminals. The op amp allows for input gain adjustment, if necessary, to either 0dB or the system's 0 level. The op amp also acts as a 2nd order analog anti-aliasing filter by bandlimiting the input to less than half of the sampling frequency per the Nyquist Rate Theorem. To meet CCITT G.712 specifications, the analog signal is filtered by a cosine filter, a 6th order low pass filter, and the high pass filter before being sampled. The sampling is performed by a capacitor array at a rate of 8kHz and the value fed into the encoder. From the encoder the 8-bit PCM data is clocked out by the shift clock.

Lastly, an auto-zero loop (without any external capacitor) provides cancellation of any DC offset by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator, and a sign bit fixation circuitry reduces idle channel noise during quiet periods.

**Timing Requirements**–The 8kHz transmit and receive sampling strobes need not be exactly 8 bit periods wide. The codec has an internal bit counter that counts the number of data bits shifted and forces the PCM output into a high impedance state after the 8th bit has been shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and the shift clock is synchronized to it and the clock rate is either 1.536MHz, 1.544MHz, or 2.048MHz. Note that all internal clocks for the switched capacitor filters and timing conversions are automatically derived; no external control signal for clock selection is required.

**Power Down Circuitry**–The codec can be powered in two ways. The most direct power down command is to force the $\overline{PD}$ (pin 14) mode select low. This will shut down the chip regardless of the strobes. The second way is to stop strobing with the SYNC (pin 11) input. The SYNC can be held high, low, or floating, as long as its state is not changed. After the chip has been shut down, the $PCM_{OUT}$ is locked into a high impedance state and the $A_{OUT}$ is connected to $A_{GND}$ to avoid output noise to the system.

**A-Law Characteristics**–Compression (refer to figure 1) allows more channels to be multiplexed on a given transmission media by reducing the bandwidth of each individual channel. Figure 2 shows the A-Law companding transfer function used in telephony to convert the speaker's analog voice signal into PCM. Figure 3 shows the expansion transfer function used to convert the digital PCM signal back into an analog signal for the end telephone user to hear.

**Response Characteristics**–Figure 4 shows the very flat (less than ± .25dB) response of a typical S44233 receiver filter, while figure 5 shows the very flat response of a typical S44233 transmit filter. Figure 6 shows the gain tracking curve of a typical S44233 codec, and figure 7 shows the signal to distortion ratio of a typical S44233 codec. Together the flat filter response, excellent gain tracking, and low distortion make the S44233 an excellent choice for telephony's demanding quality needs.

**Figure 1**

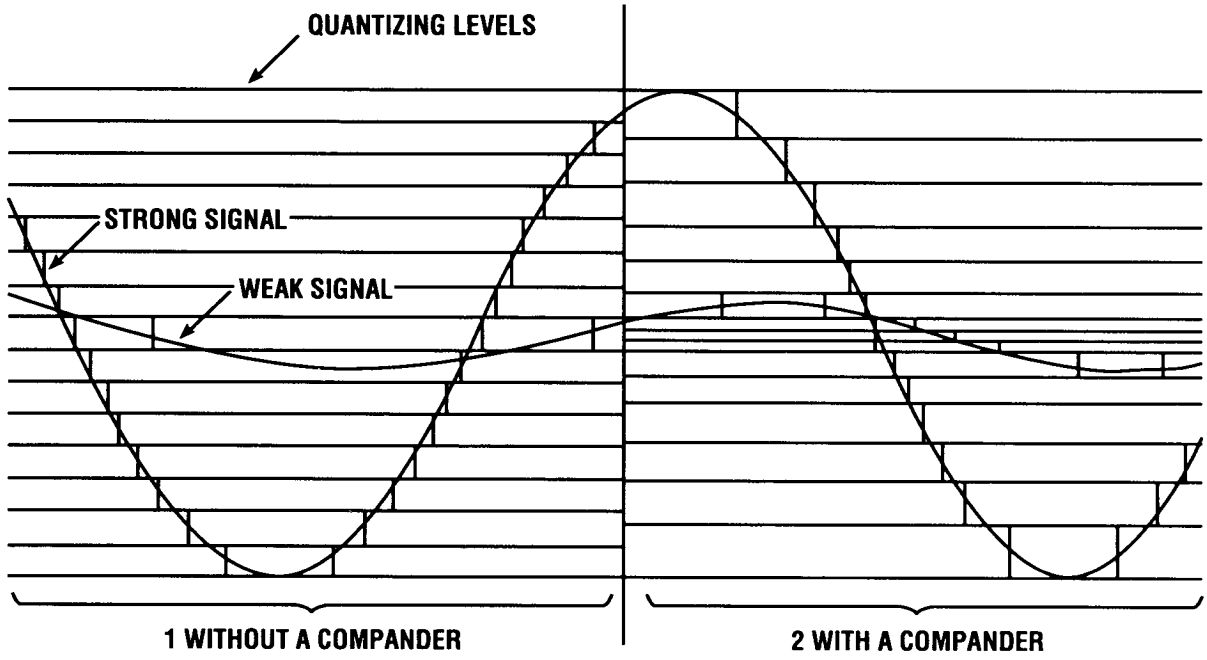

QUANTIZING LEVELS
STRONG SIGNAL
WEAK SIGNAL
1 WITHOUT A COMPANDER
2 WITH A COMPANDER

**Figure 2: The A-Law A/D Companding Transfer Function**

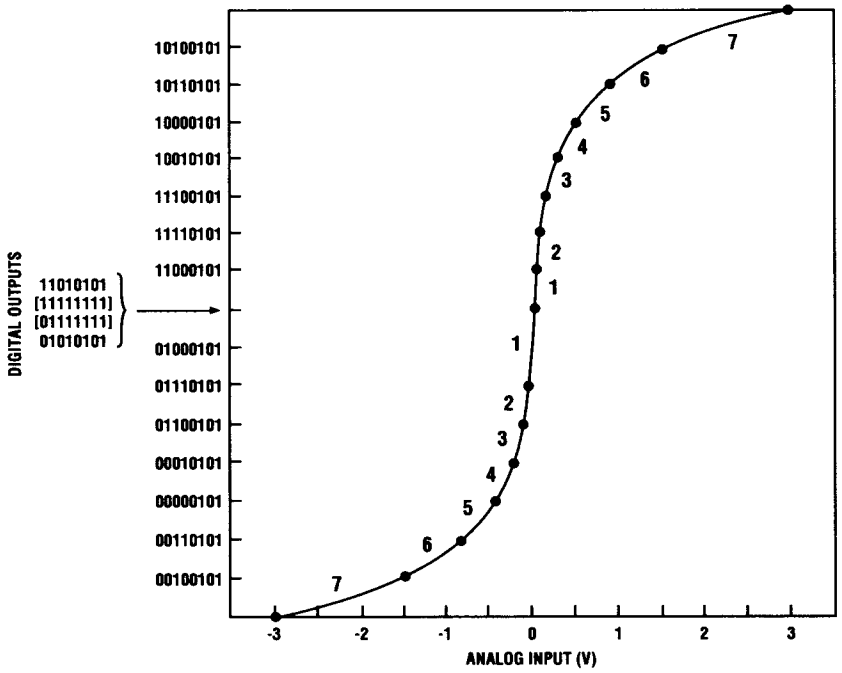
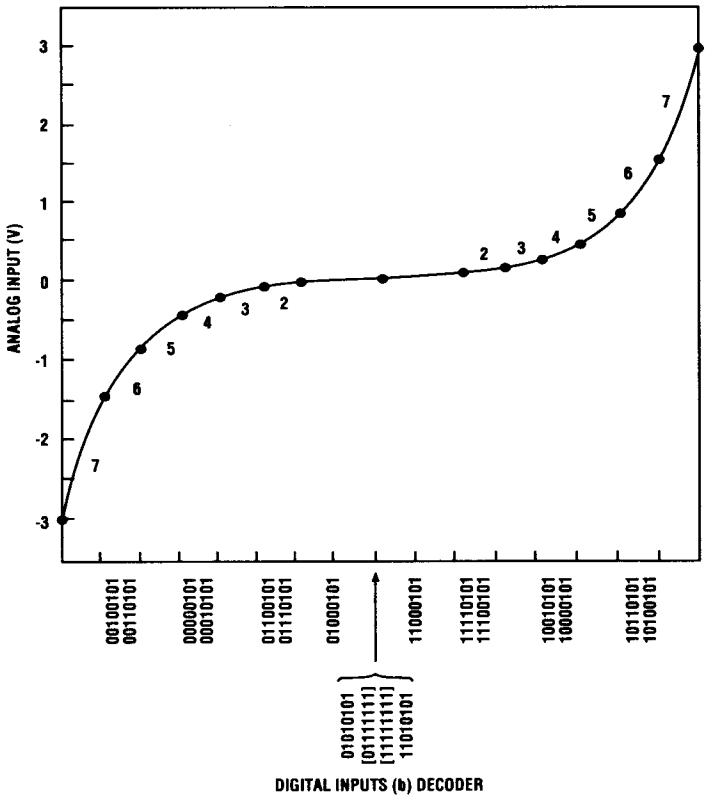
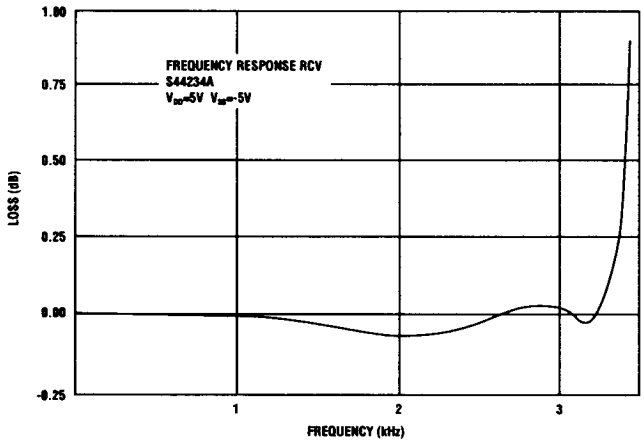


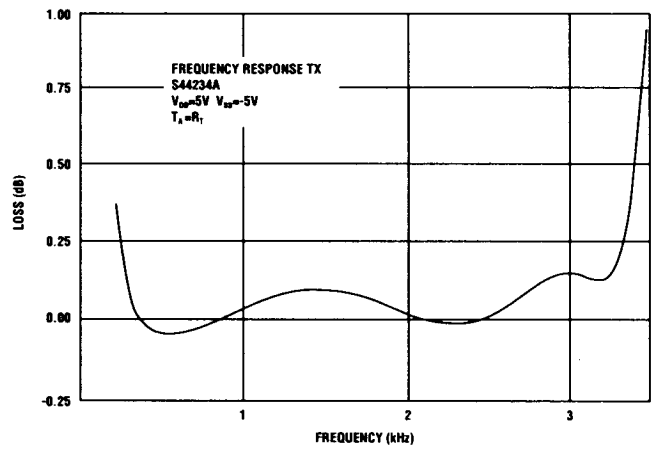

**Figure 3: The A-Law D/A Companding Transfer Function**



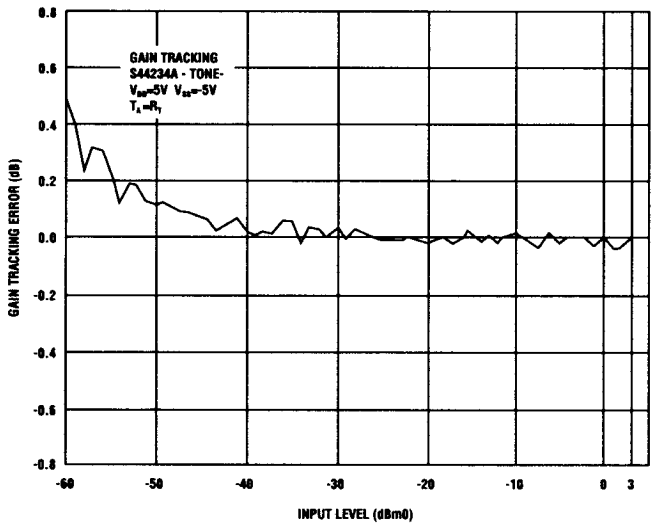
## Figure 4




## Figure 5




## Figure 6




## Figure 7