QUAD GIGABIT ETHERNET DEVICE S2204

FEATURES

- 1250 MHz (Gigabit Ethernet) operating rate
  - 1/2 Rate Operation
- IEEE 802.3z Gigabit Ethernet Compatible
- Quad Transmitter with phase-locked loop (PLL) clock synthesis from low speed reference
- Quad Receiver PLL provides clock and data recovery
- Internally series terminated TTL outputs
- Low-jitter serial PECL interface
- Individual local loopback control
- JTAG 1149.1 Boundary scan on low speed I/O signals
- Interfaces with coax, twinax, or fiber optics
- Single +3.3V supply, 2.5 W power dissipation
- Compact 23mm x 23mm 208 TBGA package

APPLICATIONS

- Ethernet Backbones
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

GENERAL DESCRIPTION

The S2204 facilitates high-speed serial transmission of data in a variety of applications including Gigabit Ethernet, serial backplanes, and proprietary point to point links. The chip provides four separate transceivers which can be operated individually for a data capacity of >4 Gbps.

Each bi-directional channel provides parallel to serial and serial to parallel conversion, clock generation/recovery, and framing. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip quad receive PLL is used for clock recovery and data re-timing on the four independent data inputs. The transmitter and receiver each support differential PECL-compatible I/O for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a 3.3V power supply and dissipates 2.5 watts.

Figure 1 shows the S2204 and S2004 in a Gigabit Ethernet application. Figure 2 combines the S2204 with a crosspoint switch to demonstrate a serial backplane application. Figure 3 is the input/output diagram. Figures 4 and 5 show the transmit and receive block diagrams, respectively.

Figure 1. Typical Quad Gigabit Ethernet Application

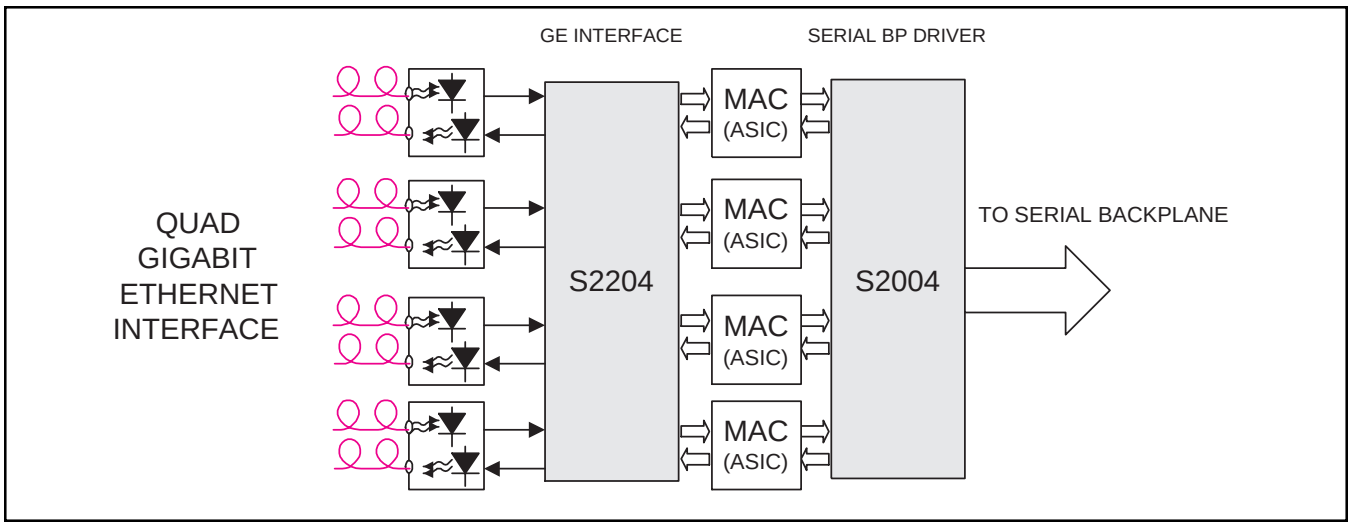


Figure 2. Typical Backplane Application

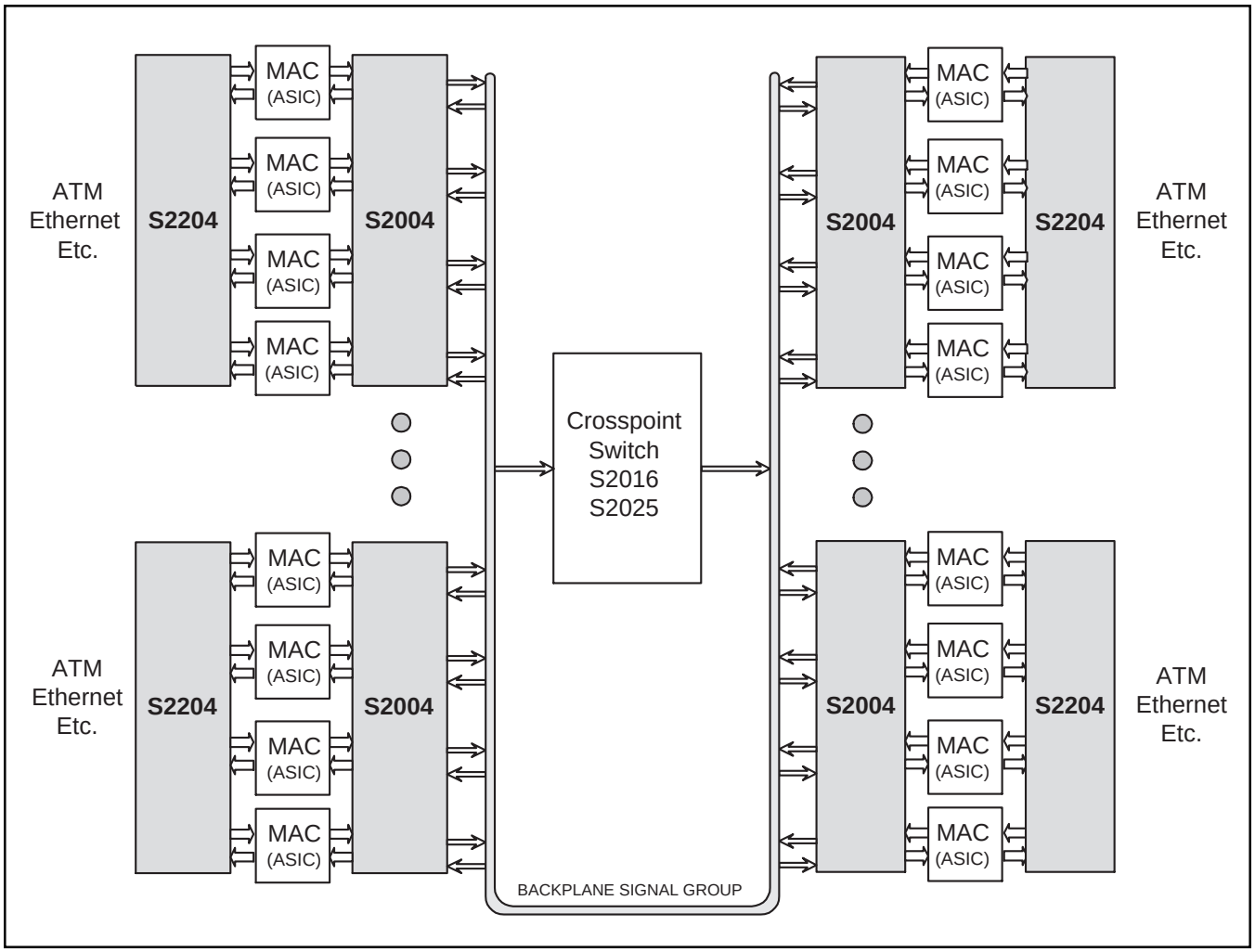


Figure 3. S2204 Input/Output Diagram

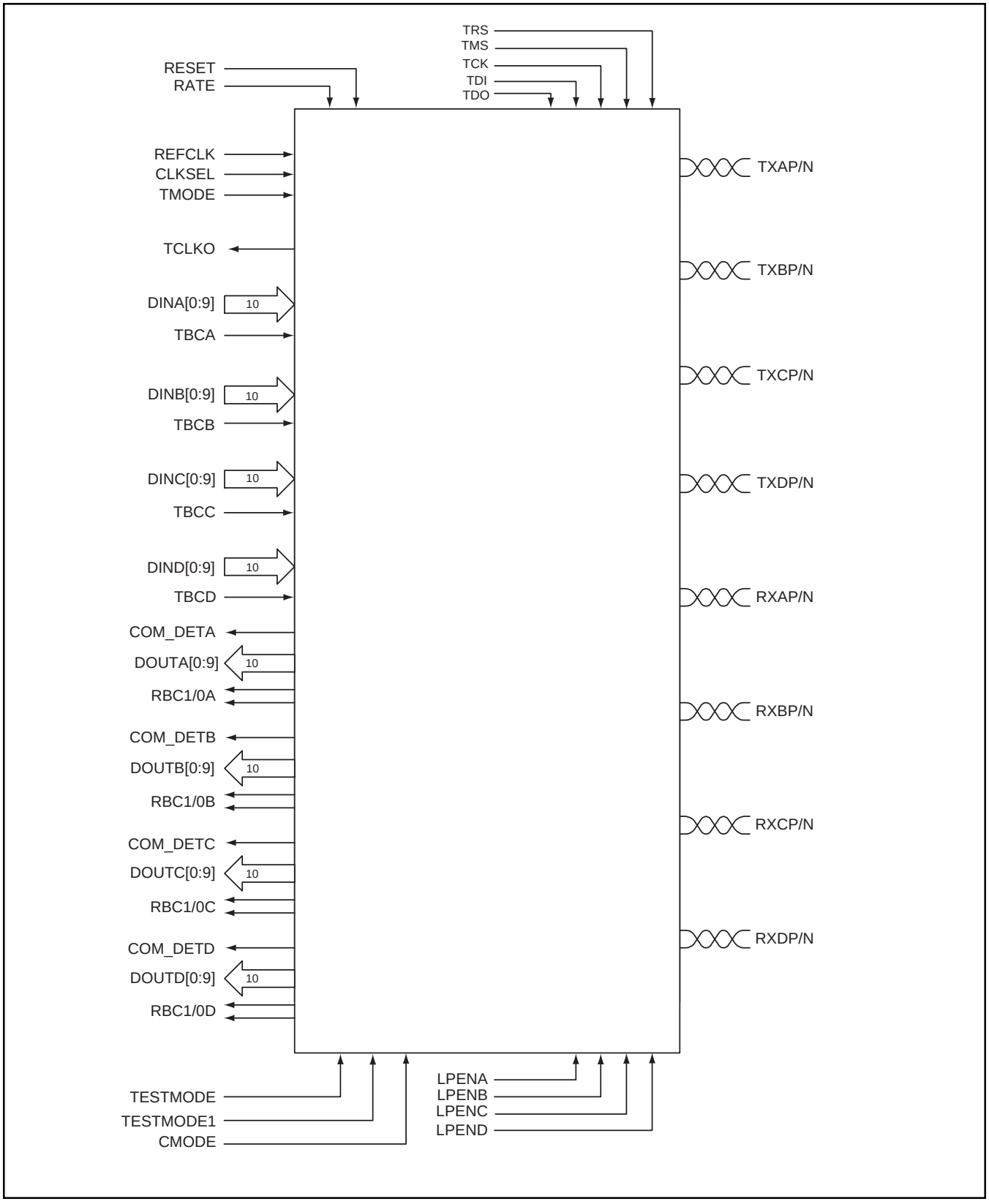


Figure 4. Transmitter Block Diagram

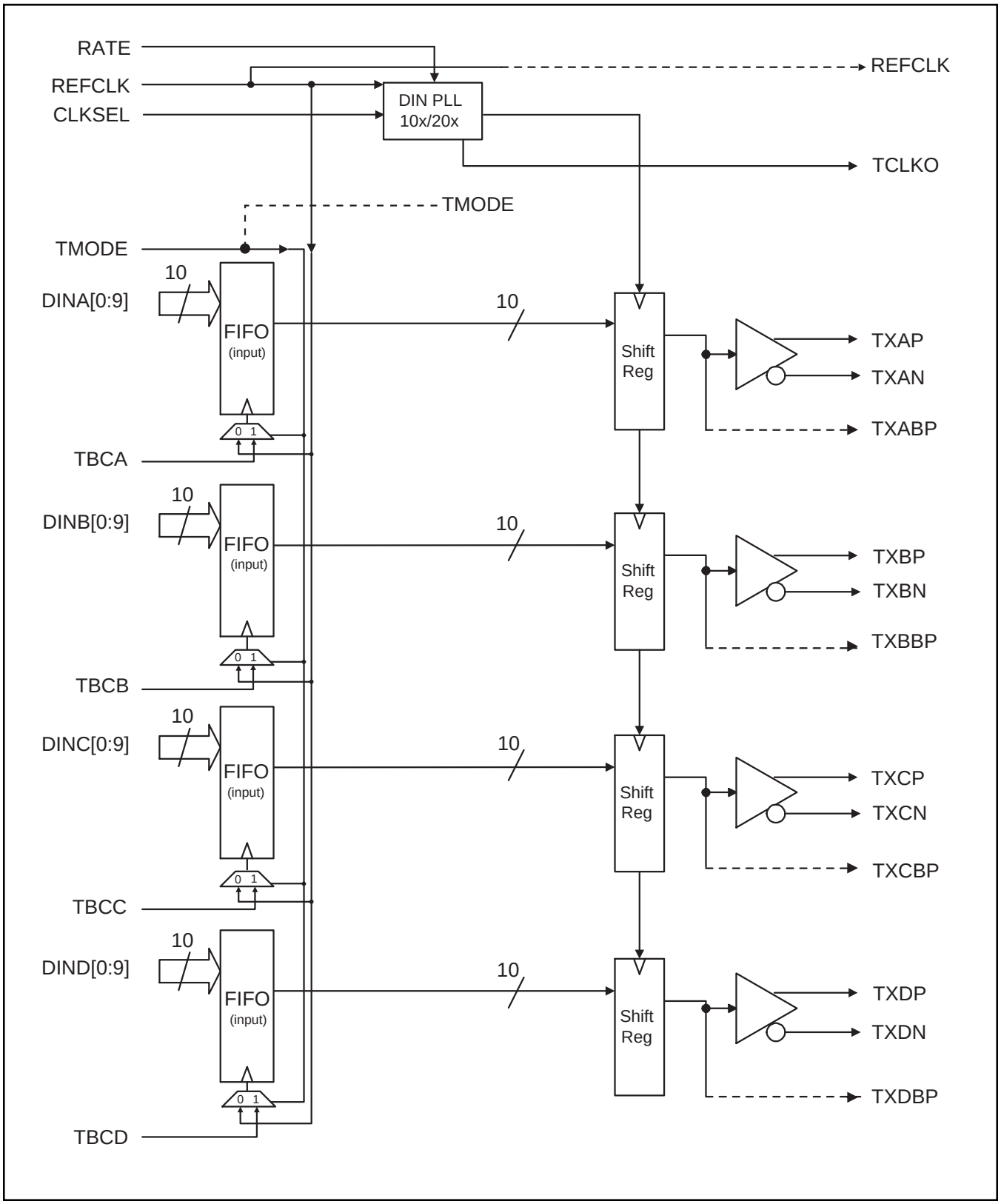
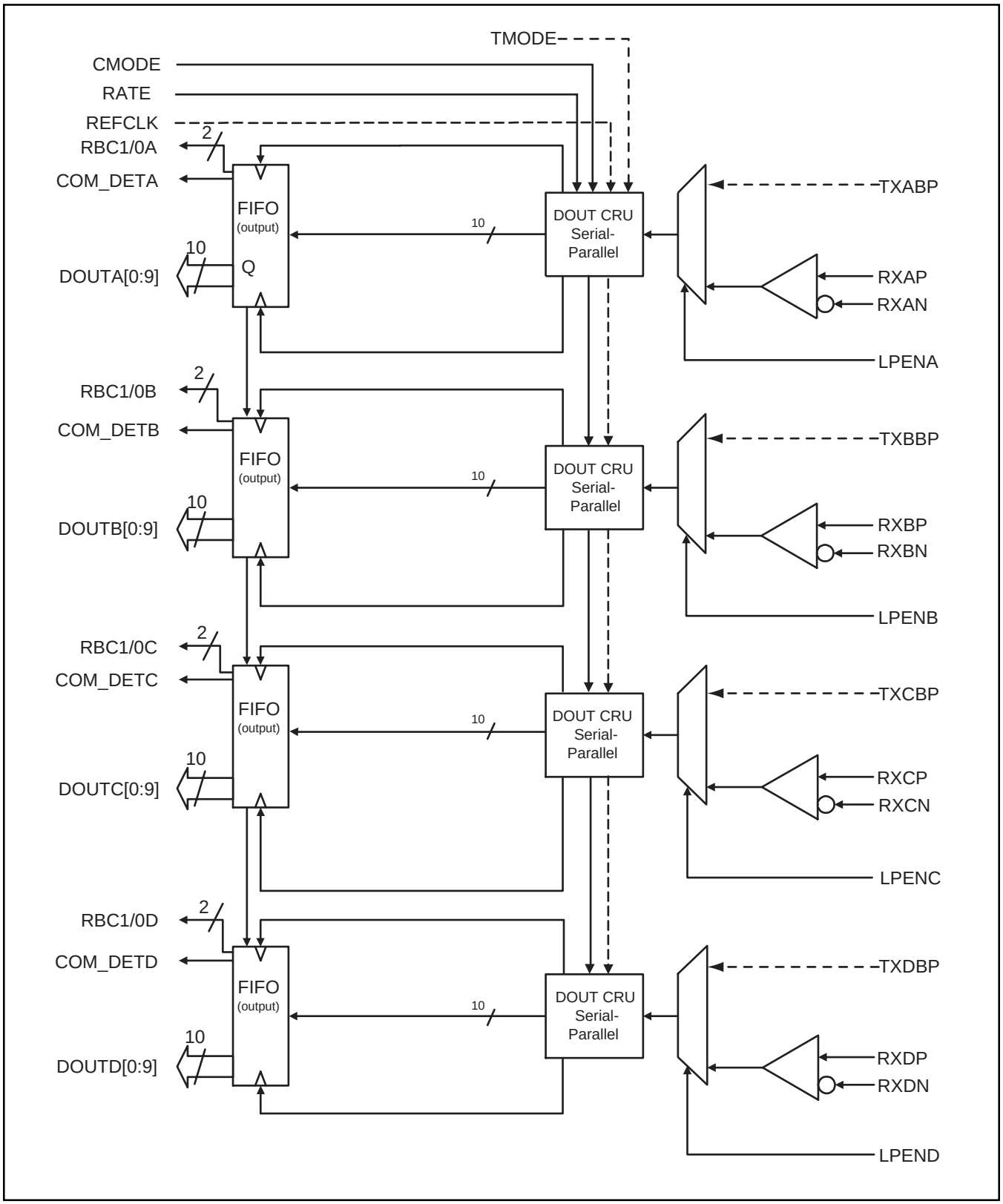


Figure 5. Receiver Block Diagram



TRANSMITTER DESCRIPTION

The transmitter section of the S2204 contains a single PLL which is used to generate the serial rate transmit clock for all transmitters. Four channels are provided with a variety of options regarding input clocking and loopback. The transmitters operate at 1.250 GHz, 10 or 20 times the reference clock frequency.

Data Input

The S2204 has been designed to simplify the parallel interface data transfer and provides the utmost in flexibility regarding clocking of parallel data. The S2204 incorporates a unique FIFO structure on both the parallel inputs and the parallel outputs which enables the user to provide a “clean” reference source for the PLL and to accept a separate external clock which is used exclusively to reliably clock data into the device.

Data is input to each channel of the S2204 nominally as a 10 bit wide word. An input FIFO and a clock input, TBCx, are provided for each channel of the S2204. The device can operate in two different modes. The S2204 can be configured to use either the TBCx (TBC MODE) input or the REFCLK input (REFCLK MODE). Table 1 provides a summary of the input modes for the S2204.

Operation in the TBC MODE makes it easier for users to meet the relatively narrow setup and hold time window required by the 125 Mbps 10-bit interface. The TBC signal is used to clock the data into an internal holding register and the S2204 synchronizes its internal data flow to insure stable operation. However, regardless of the clock mode, REFCLK is always the VCO reference clock. This facilitates the provision of a clean reference clock resulting in minimum jitter on the serial output. The TBC must be frequency locked to REFCLK, but may have an arbitrary phase relationship. Adjustment of internal timing of the S2204 is performed during reset. Once synchronized, the user must insure that the timing of the TBC signal does not change by more than ± 3 ns relative to the REFCLK.

Figure 6 demonstrates the flexibility afforded by the S2204. A low jitter reference is provided directly to the S2204 at either 1/10 or 1/20 the serial data rate. This insures minimum jitter in the synthesized clock used for serial data transmission. A system clock output at the parallel word rate, TCLKO, is derived from the PLL and provided to the upstream circuit as a system clock. The frequency of this output is constant at the parallel word rate, 1/10 the serial data rate, regardless of whether the reference is provided at 1/10 or 1/20 the serial data rate. This clock can be buffered as required without concern about added delay. There is no phase requirement between TCLKO and TBCx, which is provided back to the S2204, other than that they remain within ±3 ns of the phase relationship established at reset.

The S2204 also supports the traditional REFCLK clocking found in many Gigabit Ethernet applications and is illustrated in Figure 7.

Half Rate Operation

The S2204 supports full and 1/2 rate operation for all modes of operation. When RATE is LOW, the S2204 serial data rate equals the VCO frequency. When RATE is HIGH, the VCO is divided by 2 before being provided to the chip. Thus the S2204 can support Gigabit Ethernet and serial backplane functions at both full and 1/2 the VCO rate. See Table 3.

Parallel to Serial Conversion

The 10-bit parallel data handled by the S2204 device should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded, 8 bits at a time, into a 10-bit transmission character and must be compliant with IEEE 802.3z Gigabit Ethernet.

The 8B/10B transmission code includes serial encoding and decoding rules, special characters, and error control. Information is encoded, 8 bits at a time, into a 10 bit transmission character. The characters defined by this code ensure that short run lengths and enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple errors that might occur during the transmission and reception of data[1].

1. A.X. Widner and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC9391, May 1982.

Table 2 identifies the mapping of the 8B/10B characters to the data inputs of the S2204. The S2204 will serialize the parallel data for each channel and will transmit bit “a” or DIN[0] first.

Frequency Synthesizer (PLL)

The S2204 synthesizes a serial transmit clock from the reference signal. Upon startup, the S2204 will obtain phase and frequency lock within 2500 bit times after the start of receiving reference clock inputs. Reliable locking of the transmit PLL is assured, but a lock-detect output in NOT provided.

Table 1. Input Modes

TMODE	Operation
0	REFCLK MODE. REFCLK used to clock data into FIFOs for all channels.
1	TBC MODE. TBCx used to clock data into FIFOs for all channels.

1. Note that internal synchronization of FIFOs is performed upon de-assertion of RESET.

Figure 6. DIN Data Clocking with TBC

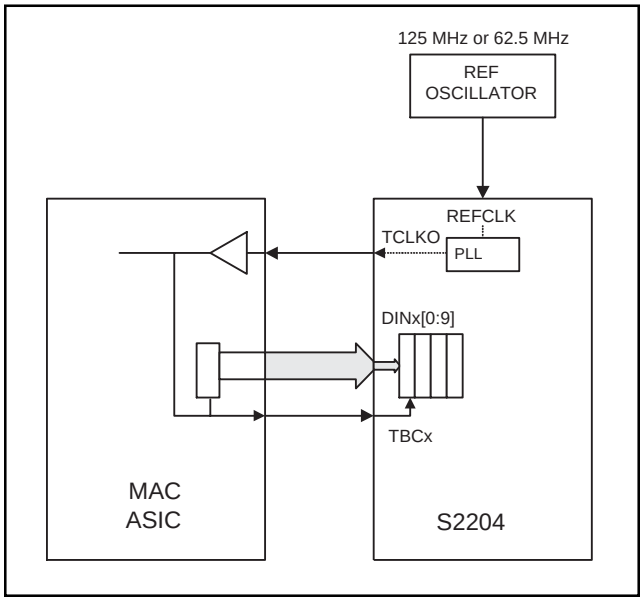


Figure 7. DIN Clocking with REFCLK

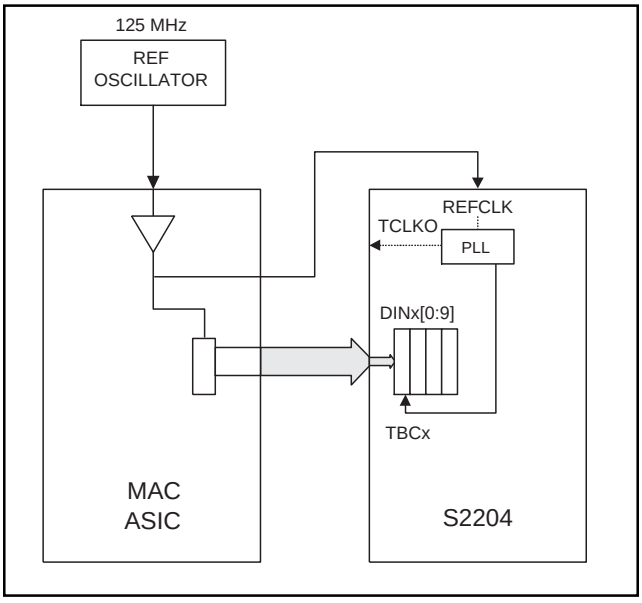


Table 2. Data to 8B/10B Alphabetic Representation

	Data Byte									
DIN[0:9] or DOUT[0:9]	0	1	2	3	4	5	6	7	8	9
8B/10B Alphanumeric Representation	a	b	c	d	e	i	f	g	h	j

Reference Clock Input

The reference clock input must be supplied with a low-jitter clock source. All reference clocks in a system must be within 200 ppm of each other to insure that the clock recovery units can lock to the serial data.

The frequency of the reference clock must be either 1/10 the serial data rate, CLKSEL = 0, or 1/20 the serial data rate, CLKSEL=1. In both cases the frequency of the parallel word rate output, TCLKO, is constant at 1/10 the serial data rate. See Table 3.

Table 3. Operating Rates

RATE	CLKSEL	REFCLK Frequency	Serial Output Rate	TCLKO Frequency
0	0	125 MHz	1250 MHz	125 MHz
0	1	62.5 MHz	1250 MHz	125 MHz
1	0	62.5 MHz	625 MHz	62.5 MHz
1	1	31.25 MHz	625 MHz	62.5 MHz

Serial Data Outputs

The S2204 provides LVPECL level serial outputs. The serial outputs do not require output pulldown resistors. Outputs are designed to perform optimally when AC-coupled.

Transmit FIFO Initialization

The transmit FIFO must be initialized after stable delivery of data and TBC to the parallel interface, and before entering the normal operational state of the circuit. FIFO initialization is performed upon the de-assertion of the RESET signal. TCLKO will operate normally regardless of the state of RESET.

RECEIVER DESCRIPTION

Each receiver channel is designed to implement a Serial Backplane receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 5.

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. After acquiring bit synchronization, the S2204 searches the serial bit stream for the occurrence of a K28.5 character on which to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the word-aligned data on its parallel outputs.

Data Input

A differential input receiver is provided for each channel of the S2204. Each channel has a loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function for each channel is enabled by its respective LPEN input.

The high speed serial inputs to the S2204 are internally biased to VDD-1.3V. All that is required externally are AC-coupling and line-to-line differential termination.

Clock Recovery Function

Clock recovery is performed on the input data stream for each channel of the S2204. The receiver PLL has been optimized for the anticipated needs of Serial Backplane systems. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the serial data inputs. If at any time the frequency or run length checks are violated, the state machine forces the VCO to lock to the reference clock. This allows the VCO to maintain the correct frequency in the absence of data.

Table 4. Lock to Reference Frequency Criteria

Current Lock State	PLL Frequency (vs. REFCLK)	New Lock State
Locked	< 488 ppm	Locked
	488 to 732 ppm	Undetermined
	> 732 ppm	Unlocked
Unlocked	< 244 ppm	Locked
	244 to 366 ppm	Undetermined
	> 366 ppm	Unlocked

The “lock to reference” frequency criteria ensure that the S2204 will respond to variations in the serial data input frequency (compared to the reference frequency). The new Lock State is dependent upon the current lock state, as shown in Table 4.

The run-length criteria insure that the S2204 will respond appropriately and quickly to a loss of signal. The run-length checker flags a condition of consecutive ones or zeros across 12 parallel words. Thus 119 or less consecutive ones or zeros does not cause signal loss, 129 or more causes signal loss, and 120 - 128 may or may not, depending on how the data aligns across byte boundaries.

If both the off-frequency detect circuitry test and the run-length test are satisfied, the CRU will attempt to lock to the incoming data. It is possible for the run length test to be satisfied due to noise on the inputs, even if no signal is present. In this case the receiver VCO will maintain frequency accuracy to within 100 ppm of the target rate as determined by REFCLK.

In any transfer of PLL control from the serial data to the reference clock, the RBC1/0x outputs remain phase continuous and glitch free, assuring the integrity of downstream clocking.

Reference Clock Input

A single reference clock, which serves both transmitter and receiver, must be provided from a low jitter clock source. The frequency of the received data stream (divided-by -10 or -20) must be within 200 ppm of the reference clock to insure reliable locking of the receiver PLL.

Serial to Parallel Conversion

Once bit synchronization has been attained by the S2204 CRU, the S2204 must synchronize to the 10 bit word boundary. Word synchronization in the S2204 is accomplished by detecting and aligning to the 8B/10B K28.5 codeword. The S2204 will detect and byte-align to either polarity of the K28.5. Each channel of the S2204 will detect and align to a K28.5 anywhere in the data stream. The presence of a K28.5 is indicated for each channel by the assertion of the COM_DETx signal.

Data Output

Data is output on the DOUT[0:9] outputs. The COM_DET signal is used to indicate the reception of a valid K28.5 character.

The S2204 TTL outputs are optimized to drive 65Ω line impedances. Internal source matching provides good performance on unterminated lines of reasonable length.

Parallel Output Clock Rate

Two output clock modes are supported, as shown in Table 5. When CMODE is High, a complementary TTL clock at the data rate is provided on the RBC1/0x outputs. Data should be clocked on the rising edge of RBC1x. When CMODE is Low, a complementary TTL clock at 1/2 the data rate is provided. Data should be latched on the rising edge of RBC1x and the rising edge of RBC0x.

In Gigabit Ethernet applications, multiple consecutive K28.5 characters cannot be generated. However, for serial backplane applications this can occur. The S2204 must be able to operate properly when multiple K28.5 characters are received. After the first K28.5 is detected and aligned, the RBC1/0x clock will operate without glitches or loss of cycles.

Receiver Output Clocking

The S2204 parallel output clock source is determined by the TMODE selection. When REFCLK clocking is selected (TMODE = Low), the parallel output clocks (RCxP/N) are sourced from the TCLKA input. When TCLK clocking is selected (External Clocking Mode), the parallel output clocks are derived from the recovered clock from each channel. Table 5A describes the receiver output clocking options available.

When TCLKA is the output clock source, REFCLK and TCLKA must equal the parallel word rate (CLKSEL = Low). Additionally, the recovered clocks and the clock input on TCLKA must be frequency locked in order to avoid overflow/underflow of the internal FIFOs. The propagation delay between TCLKA and DOUTx, listed in Table 21, shows that the phase delay between TCLKA and the RCxP/N outputs may vary more than a bit time based on process variation.

The recommended clocking configuration for external clocking mode (REFCLK input clocking) is shown in Figure 8. TCLKA is sourced from TCLKO, which is frequency locked to the Reference clock input.

Figure 8. External Receiver Clocking

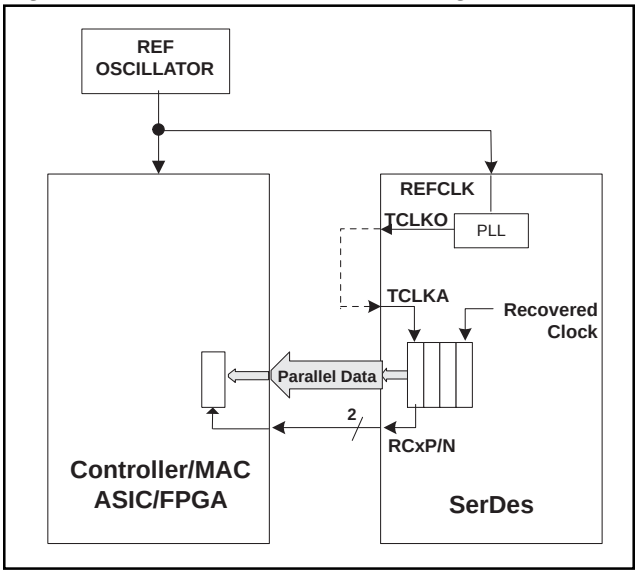


Table 5. Output Clock Mode (TMODE = 1)

Mode	CMODE	RBC1/0x Freq
Half Clock Mode	0	62.5 MHz
Full Clock Mode	1	125 MHz

Table 5A. S2204 Data Clocking

TMODE	Input Clock Source	Output Clock Source
0	REFCLK	TBCA
1	TBCx	RBCx

OTHER OPERATING MODES

Operating Frequency Rate

The S2204 is designed to operate at the Gigabit Ethernet rate of 1.250 GHz.

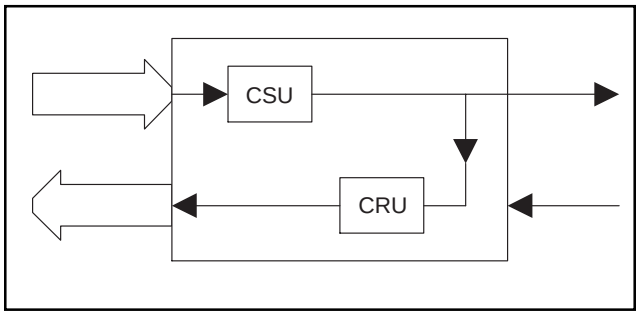
Loopback Mode

When loopback mode is enabled, the serial data from the transmitter is provided to the serial input of the receiver, as shown in Figure 9. This provides the ability to perform system diagnostics and off-line testing of the interface to verify the integrity of the serial channel. Loopback mode is enabled independently for each channel using its respective loopback-enable input, LPEN.

TEST MODES

The RESET pin is used to initialize the Transmit FIFOs and must be asserted (LOW) prior to entering the normal operational state (see section Transmit FIFO Initialization).

Figure 9. S2204 Diagnostic Loopback Operation



Note: Serial output data remains active during loopback operation to enable other system tests to be performed.

JTAG TESTING

The JTAG implementation for the S2204 is compliant with the IEEE1149.1 requirements. JTAG is used to test the connectivity of the pins on the chip. The TAP, (Test Access Port), provides access to the test logic of the chip. When TRST is asserted the TAP is initialized. TAP is a state machine that is controlled by TMS. The test instruction and data are loaded through TDI on the rising edge of TCK. When TMS is high the test instruction is loaded into the instruction register. When TMS is low the test data is loaded into the data register. TDO changes on the falling edge of TCK. All input pins, including clocks, that have boundary scan are observe only. They can be sampled in either normal operational or test mode. All output pins that have boundary scan, are observe and control. They can be sampled as they are driven out of the chip in normal operational mode, and they can be driven out of the chip in test mode using the Extest instruction. Since JTAG testing operates only on digital signals there are some pins with analog signals that JTAG does not cover. The JTAG implementation has the three required instruction, Bypass, Extest, and Sample/Preload.

Instruction	Code
BYPASS	11
EXTEST	00
SAMPLE/PRELOAD	01
ID CODE	10

JTAG Instruction Description:

The BYPASS register contains a single shift-register stage and is used to provide a minimum-length serial path between the TDI and TDO pins of a component when no test operation of that component is required. This allows more rapid movement of test data to and from other components on a board that are required to perform test operations.

The EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.

The SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register prior to selection of the other boundary-scan test instructions.

The following table provides a list of the pins that are JTAG tested. Each port has a boundary scan register (BSR), unless otherwise noted. The following features are described: the JTAG mode of each register (input, output2, or internal (refers to an internal package pin)), the direction of the port if it has a boundary scan register (in or out), and the position of this register on the scan chain.

Table 6. JTAG Pin Assignments

S2204 Pin Name	Core_Scan Port Name	JTAG Mode	Routing In	Routing Out
TESTMODE1	sync	Input	0	-
CMODE	cmode	Input	1	-
TESTMODE	chan_lock	Input	2	-
LPEND	lpend	Input	3	-
LPENC	lpenc	Input	4	-
LPENB	lpenb	Input	5	-
LPENA	lpena	Input	6	-
CLKSEL	clksel	Input	7	-
TMODE	tmode	Input	8	-
		Internal	9	-
RESET	reset	Input	10	-
REFCLK	refclk	Input	11	-
TCLKO	transmit_clk_ buf_out	Output2	-	12
DIND9	dnd	Input	13	-
DIND8	kgend	Input	14	-
DIND7	tdatain_d (7)	Input	15	-
DIND6	tdatain_d (6)	Input	16	-
DIND5	tdatain_d (5)	Input	17	-
DIND4	tdatain_d (4)	Input	18	-
DIND3	tdatain_d (3)	Input	19	-
DIND2	tdatain_d (2)	Input	20	-
DIND1	tdatain_d (1)	Input	21	-
DIND0	tdatain_d (0)	Input	22	-
TBCD	tclkd	Input	23	-
DINC9	dnc	Input	24	-
DINC8	kgenc	Input	25	-
DINC7	tdatain_c (7)	Input	26	-
DINC6	tdatain_c (6)	Input	27	-
DINC5	tdatain_c (5)	Input	28	-
DINC4	tdatain_c (4)	Input	29	-
DINC3	tdatain_c (3)	Input	30	-
DINC2	tdatain_c (2)	Input	31	-
DINC1	tdatain_c (1)	Input	32	-
DINC0	tdatain_c (0)	Input	33	-
TBCC	tclkc	Input	34	-
DINB8	kgenb	Input	35	-
DINB9	dnb	Input	36	-
DINB7	tdatain_b (7)	Input	37	-
DINB6	tdatain_b (6)	Input	38	-
DINB5	tdatain_b (5)	Input	39	-

Table 6. JTAG Pin Assignments (Continued)

S2204 Pin Name	Core_Scan Port Name	JTAG Mode	Routing In	Routing Out
DINB4	tdatain_b (4)	Input	40	-
DINB3	tdatain_b (3)	Input	41	-
DINB2	tdatain_b (2)	Input	42	-
DINB1	tdatain_b (1)	Input	43	-
DINB0	tdatain_b (0)	Input	44	-
TBCB	tclkb	Input	45	-
DINA9	dna	Input	46	-
DINA8	kgena	Input	47	-
DINA7	tdatain_a (7)	Input	48	-
DINA6	tdatain_a (6)	Input	49	-
DINA5	tdatain_a (5)	Input	50	-
DINA4	tdatain_a (4)	Input	51	-
DINA3	tdatain_a (3)	Input	52	-
DINA2	tdatain_a (2)	Input	53	-
DINA1	tdatain_a (1)	Input	54	-
DINA0	tdatain_a (0)	Input	55	-
TBCA	tclka	Input	56	-
RBC1D	rcdp	Output2	-	57
RBC0D	rcdn	Output2	-	58
DOUTD7	rdataout_d (7)	Output2	-	59
DOUTD6	rdataout_d (6)	Output2	-	60
DOUTD5	rdataout_d (5)	Output2	-	61
DOUTD4	rdataout_d (4)	Output2	-	62
DOUTD3	rdataout_d (3)	Output2	-	63
DOUTD2	rdataout_d (2)	Output2	-	64
DOUTD1	rdataout_d (1)	Output2	-	65
DOUTD0	rdataout_d (0)	Output2	-	66
COM_DETD	eofd_d	Output2	-	67
DOUTD8	kflagd_d	Output2	-	68
DOUTD9	errd_d	Output2	-	69
RBC1C	rccp	Output2	-	70
RBC0C	rccn	Output2	-	71
DOUTC7	rdataout_c (7)	Output2	-	72
DOUTC6	rdataout_c (6)	Output2	-	73
DOUTC5	rdataout_c (5)	Output2	-	74
DOUTC4	rdataout_c (4)	Output2	-	75
DOUTC3	rdataout_c (3)	Output2	-	76
DOUTC2	rdataout_c (2)	Output2	-	77
DOUTC1	rdataout_c (1)	Output2	-	78
DOUTC0	rdataout_c (0)	Output2	-	79

Table 6. JTAG Pin Assignments (Continued)

S2204 Pin Name	Core_Scan Port Name	JTAG Mode	Routing In	Routing Out
DOUTC9	errd_c	Output2	-	80
COM_DETC	eofd_c	Output2	-	81
DOUTC8	kflag_c	Output2	-	82
RBC1B	rcbp	Output2	-	83
RBC0B	rcbn	Output2	-	84
DOUTB8	kflagd_b	Output2	-	85
DOUTB7	rdataout_b (7)	Output2	-	86
DOUTB6	rdataout_b (6)	Output2	-	87
DOUTB5	rdataout_b (5)	Output2	-	88
DOUTB4	rdataout_b (4)	Output2	-	89
DOUTB3	rdataout_b (3)	Output2	-	90
DOUTB2	rdataout_b (2)	Output2	-	91
DOUTB1	rdataout_b (1)	Output2	-	92
DOUTB0	rdataout_b (0)	Output2	-	93
COM_DETB	eofd_b	Output2	-	94
DOUTB9	errd_b	Output2	-	95
RBC1A	rcap	Output2	-	96
RBC0A	rcan	Output2	-	97
DOUTA9	errd_a	Output2	-	98
DOUTA7	rdataout_a (7)	Output2	-	99
DOUTA6	rdataout_a (6)	Output2	-	100
DOUTA5	rdataout_a (5)	Output2	-	101
DOUTA4	rdataout_a (4)	Output2	-	102
DOUTA3	rdataout_a (3)	Output2	-	103
DOUTA2	rdataout_a (2)	Output2	-	104
DOUTA1	rdataout_a (1)	Output2	-	105
DOUTA0	rdataout_a (0)	Output2	-	106
COM_DETA	eofd_a	Output2	-	107
DOUTA8	kflagd_a	Output2	-	108
		Internal	-	109

Table 6. JTAG Pin Assignments (Continued)

S2204 Pin Name	Core_Scan Port Name	JTAG Mode	Routing In	Routing Out
JTAG Control Pins (Ports that do not have a Boundary Scan Register)				
TCK	jtag_tck	-	-	-
TDI	jtag_tdi	-	-	-
TDO	jtag_tdo	-	-	-
TMS	jtag_tms	-	-	-
TRS	jtag_trs	-	-	-
Pins not JTAG Tested				
TXAP	-	-	-	-
TXAN	-	-	-	-
TXBP	-	-	-	-
TXBN	-	-	-	-
TXCP	-	-	-	-
TXCN	-	-	-	-
TXDP	-	-	-	-
TXDN	-	-	-	-
RATE	-	-	-	-
RXAP	-	-	-	-
RXAN	-	-	-	-
RXBP	-	-	-	-
RXBN	-	-	-	-
RXCP	-	-	-	-
RXCN	-	-	-	-
RXDP	-	-	-	-
RXDN	-	-	-	-

Table 7. Transmitter Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DINA9 DINA8 DINA7 DINA6 DINA5 DINA4 DINA3 DINA2 DINA1 DINA0	TTL	I	U15 U14 P12 R12 T13 T12 U13 P11 R11 T11	Transmit Data for Channel A. Parallel data on this bus is clocked in on the rising edge of TBCA or REFCLK. (See Table 1.)
TBCA	TTL	I	U12	Transmit Byte Clock A. When TMODE is High, this signal is used to clock Data on DINA[0:9] into the S2204. When TMODE is Low, TBCA is ignored.
DINB9 DINB8 DINB7 DINB6 DINB5 DINB4 DINB3 DINB2 DINB1 DINB0	TTL	I	R16 T16 R15 P14 T15 R14 U17 U16 P13 T14	Transmit Byte for Channel B. Parallel data on this bus is clocked in on the rising edge of TBCB or REFCLK. (See Table 1.)
TBCB	TTL	I	R13	Transmit Byte Clock B. When TMODE is High, this signal is used to clock Data on DINB[0:9] into the S2204. When TMODE is Low, TBCB is ignored.
DINC9 DINC8 DINC7 DINC6 DINC5 DINC4 DINC3 DINC2 DINC1 DINC0	TTL	I	N17 P17 M15 N16 M14 R17 P16 N15 T17 N14	Transmit Data for Channel C. Parallel data on this bus is clocked in on the rising edge of TBCC or REFCLK. (See Table 1.)
TBCC	TTL	I	P15	Transmit Byte Clock C. When TMODE is High, this signal is used to clock Data on DINC[0:9] into the S2204. When TMODE is Low, TBCC is ignored.

Table 7. Transmitter Signal Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DIND9 DIND8 DIND7 DIND6 DIND5 DIND4 DIND3 DIND2 DIND1 DIND0	TTL	I	J16 K17 L17 K16 K15 K14 M17 L16 M16 L15	Transmit Data for Channel D. Parallel data on this bus is clocked in on the rising edge of TBCD or REFCLK. (See Table 1.)
TBCD	TTL	I	L14	Transmit Byte Clock D. When TMODE is High, this signal is used to clock Data on DIND[0:9] into the S2204. When TMODE is Low, TBCD is ignored.

Table 8. Transmitter Output Signals

Pin Name	Level	I/O	Pin #	Description
TXAP TXAN	Diff. LVPECL	O	A17 B17	High speed serial outputs for Channel A.
TXBP TXBN	Diff. LVPECL	O	C17 D17	High speed serial outputs for Channel B.
TXCP TXCN	Diff. LVPECL	O	E17 F16	High speed serial outputs for Channel C.
TXDP TXDN	Diff. LVPECL	O	F17 G17	High speed serial outputs for Channel D.
TCLKO	TTL	O	J14	TTL Output Clock at the Parallel data rate. This clock is provided for use by up-stream circuitry.

Table 9. Mode Control Signals

Pin Name	Level	I/O	Pin #	Description
TESTMODE	TTL	I	E4	Test Mode Control. Keep Low for normal operation.
TESTMODE1	TTL	I	D4	Test Mode Control. Keep Low for normal operation.
TMODE	TTL	I	B13	Transmit Mode Control. Controls the source of the clock used to input and output data to and from the S2204. When TMODE is Low, REFCLK is used to clock data on DINx[0:9] into the S2204. TBCA is used to clock parallel data DOUTx[0:9] out of the device. When TMODE is High, the TBCx inputs are used to clock data into their respective channels. The output clocks are derived from the receiver's CRUs.
CLKSEL	TTL	I	C12	REFCLK Select Input. This signal configures the PLL for the appropriate REFCLK frequency. When CLKSEL = 0, the REFCLK frequency equals the parallel word rate. When CLKSEL = 1, the REFCLK frequency is 1/2 the parallel data rate.
REFCLK	TTL	I	H17	Reference Clock is used for the transmit VCO and frequency check for the clock recovered from the receiver serial data. Also used to clock parallel data into the device when in REFCLK mode.
RESET	TTL	I	C15	When Low, the S2204 is held in reset. The receiver PLL is forced to lock to the REFCLK. The FIFOs are initialized on the rising edge of RESET. When High, the S2204 operates normally.
RATE	TTL	I	D12	When Low, the S2204 operates with the serial output rate equal to the VCO frequency. When High, the S2204 operates with the VCO internally divided by 2 for all functions.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 10. Receiver Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DOUTA9 DOUTA8 DOUTA7 DOUTA6 DOUTA5 DOUTA4 DOUTA3 DOUTA2 DOUTA1 DOUTA0	TTL	O	G1 G3 J1 J3 J2 H1 H2 H3 F1 G2	Channel A Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1A in full clock mode and valid on the rising edge of both RBC1A and RBC0A in half clock mode.
COM_DETA	TTL	O	F2	Channel A Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTA[0:9].
RBC1A RBC0A	TTL	O	K2 K1	Receive Byte Clocks. Parallel receive data, DOUTA[0:9] and COM_DETA are valid on the rising edge of RBC1A when in full clock mode and valid on the rising edge of both RBC1A and RBC0A in half clock mode.
DOUTB9 DOUTB8 DOUTB7 DOUTB6 DOUTB5 DOUTB4 DOUTB3 DOUTB2 DOUTB1 DOUTB0	TTL	O	K3 P2 R1 P1 M3 N2 M2 N1 L2 M1	Channel B Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1B in full clock mode and valid on the rising edge of both RBC1B and RBC0B in half clock mode.
COM_DETB	TTL	O	L1	Channel B Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTB[0:9].
RBC1B RBC0B	TTL	O	U1 T1	Receive Byte Clocks. Parallel receive data, DOUTB[0:9] and COM_DETB are valid on the rising edge of RBC1B when in full clock mode and valid on the rising edge of both RBC1B and RBC0B in half clock mode.
DOUTC9 DOUTC8 DOUTC7 DOUTC6 DOUTC5 DOUTC4 DOUTC3 DOUTC2 DOUTC1 DOUTC0	TTL	O	T2 P3 R7 R6 T5 U3 T4 R5 U2 T3	Channel C Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1C in full clock mode and valid on the rising edge of both RBC1C and RBC0C in half clock mode.
COM_DETC	TTL	O	R2	Channel C Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTC[0:9].

Table 10. Receiver Output Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
RBC1C RBC0C	TTL	O	U5 U4	Receive Byte Clocks. Parallel receive data, DOUTC[0:9] and COM_DETC are valid on the rising edge of RBC1C when in full clock mode and valid on the rising edge of both RBC1C and RBC0C in half clock mode.
DOUTD9 DOUTD8 DOUTD7 DOUTD6 DOUTD5 DOUTD4 DOUTD3 DOUTD2 DOUTD1 DOUTD0	TTL	O	T6 T7 U11 R10 U9 R9 T9 U8 U7 T8	Channel D Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1D in full clock mode and valid on the rising edge of both RBC1D and RBC0D in half clock mode.
COM_DETD	TTL	O	U6	Channel D Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTD[0:9].
RBC1D RBC0D	TTL	O	T10 U10	Receive Byte Clocks. Parallel receive data, DOUTD[0:9] and COM_DETD are valid on the rising edge of RBC1D when in full clock mode and valid on the rising edge of both RBC1D and RBC0D in half clock mode.

Table 11. Receiver Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RXAP RXAN	Diff. LVPECL	I	A2 A3	Differential LVPECL compatible inputs for channel A. RXAP is the positive input, RXAN is the negative. Internally biased to VDD -1.3V for AC coupled applications.
RXBP RXBN	Diff. LVPECL	I	A5 B5	Differential LVPECL compatible inputs for channel B. RXBP is the positive input, RXBN is the negative. Internally biased to VDD -1.3V for AC coupled applications.
RXCP RXCN	Diff. LVPECL	I	A8 A9	Differential LVPECL compatible inputs for channel C. RXCP is the positive input, RXCN is the negative. Internally biased to VDD -1.3V for AC coupled applications.
RXDP RXDN	Diff. LVPECL	I	B11 B12	Differential LVPECL compatible inputs for channel D. RXDP is the positive input, RXDN is the negative. Internally biased to VDD -1.3V for AC coupled applications.

Table 12. Receiver Control Signals

Pin Name	Level	I/O	Pin #	Description
LPENA LPENB LPENC LPEND	TTL	I	D14 G14 G15 H14	Loopback Enable. When Low, input source is the high speed serial input for each channel. When High, the serial output for each channel is looped back to its input.
CMODE	TTL	I	C2	Clock Mode Control. When Low, the parallel output clocks (RBC1/0x) rate is equal to 1/2 the data rate. When High, the parallel output clocks (RBC1/0x) rate is equal to the data rate.

Note: All TTL inputs except REFCLKhave internal pull-up networks.

Table 13. Power and Ground Signals

Pin Name	Qty.	Pin #	Description
VDDA	5	A1, A6, A13, A16, C8	Analog Power (VDD) low noise.
VSSA	5	B7, B8, B15, C4, D11	Analog Ground (VSS).
VDD	6	A12, A15, B4, B6, C6, D9	Power for High Speed Circuitry (VDD).
VSS VSSSUB	10	A4, A7, A11, A14, B10, B14, C13, D5, D6, D8	Ground for High Speed Circuitry (VSS).

Table 13. Power and Ground Signals (Continued)

Pin Name	Qty.	Pin #	Description
PECLPWR	4	D15, E15, E16, G16	PECL Power (VDD)
PECLGND	2	C16 H16	PECL Ground (VSS)
DIGPWR	6	B1, B2, E3, J17, L4, P9	Core Circuitry Power (VDD)
DIGGND	8	C1, C3, D2, F4, J15, N4, P10, R3	Core Circuitry Ground (VSS)
TTLPWR	8	E1, G4, H4, K4, N3, P5, P7, P8	Power for TTL I/O (VDD)
TTLGND	10	D1, E2, F3, J4, L3, M4 P4, P6, R4, R8	Ground for TTL I/O (VSS)
PWR	2	B16 D3	Power
CAP1 CAP2	2	D13 C14	Pins for external loop filter capacitor
NC	10	B9, C5, C7, C9, C11, D7, D16, E14, F14, F15	Not Connected. Used as Test Pins. Do Not Connect.

Table 14. JTAG Test Signals

Pin Name	Level	I/O	Pin #	Description
TMS	TTL	I	A10	Test Mode Select. Enables JTAG testing of device.
TCK	TTL	I	C10	Test Clock. JTAG test clock.
TDI	TTL	I	D10	Test Data In. JTAG data input.
TDO	TTL	O TRISTATE	H15	Test Data Out. JTAG data output. Can be high impedance under JTAG controller command.
TRS	TTL	I	B3	Test Reset. Resets JTAG test state machine.

Figure 10. S2204 Pinout (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	VDDA	DIGPWR	DIGGND	TTLGND	TTLPWR	DOUTA1	DOUTA9	DOUTA4	DOUTA7	RBC0A	COM_ DETB	DOUTB0	DOUTB2	DOUTB6	DOUTB7	RBC0B	RBC1B
2	RXAP	DIGPWR	CMODE	DIGGND	TTLGND	COM_ DETA	DOUTA0	DOUTA3	DOUTA5	RBC1A	DOUTB1	DOUTB3	DOUTB4	DOUTB8	COM_ DETC	DOUTC9	DOUTC1
3	RXAN	TRS	DIGGND	PWR	DIGPWR	TTLGND	DOUTA8	DOUTA2	DOUTA6	DOUTB9	TTLGND	DOUTB5	TTLPWR	DOUTC8	DIGGND	DOUTC0	DOUTC4
4	VSS	VDD	VSSA	TEST MODE1	TEST MODE	DIGGND	TTLPWR	TTLPWR	TTLGND	TTLPWR	DIGPWR	TTLGND	DIGGND	TTLGND	TTLGND	DOUTC3	RBC0C
5	RXBP	RXBN	NC	VSSSUB										TTLPWR	DOUTC2	DOUTC5	RBC1C
6	VDDA	VDD	VDD	VSS										TTLGND	DOUTC6	DOUTD9	COM_ DETD
7	VSSSUB	VSSA	NC	NC										TTLPWR	DOUTC7	DOUTD8	DOUTD1
8	RXCP	VSSA	VDDA	VSSSUB										TTLPWR	TTLGND	DOUTD0	DOUTD2
9	RXCN	NC	NC	VDD										DIGPWR	DOUTD4	DOUTD3	DOUTD5
10	TMS	VSS	TCK	TDI										DIGGND	DOUTD6	RBC1D	RBC0D
11	VSS	RXDP	NC	VSSA										DINA2	DINA1	DINA0	DOUTD7
12	VDD	RXDN	CLKSEL	RATE										DINA7	DINA6	DINA4	TBCA
13	VDDA	TMODE	VSSSUB	CAP1										DINB1	TBCB	DINA5	DINA3
14	VSSSUB	VSS	CAP2	LPENA	NC	NC	LPENB	LPEND	TCLKO	DIND4	TBCD	DINC5	DINC0	DINB6	DINB4	DINB0	DINA8
15	VDD	VSSA	RESET	PECL PWR	PECL PWR	NC	LPENC	TDO	DIGGND	DIND5	DIND0	DINC7	DINC2	TBCC	DINB7	DINB5	DINA9
16	VDDA	PWR	PECLGND	NC	PECL PWR	TXCN	PECL PWR	PECLGND	DIND9	DIND6	DIND2	DIND1	DINC6	DINC3	DINB9	DINB8	DINB2
17	TXAP	TXAN	TXBP	TXBN	TXCP	TXDP	TXDN	REFCLK	DIGPWR	DIND8	DIND7	DIND3	DINC9	DINC8	DINC4	DINC1	DINB3

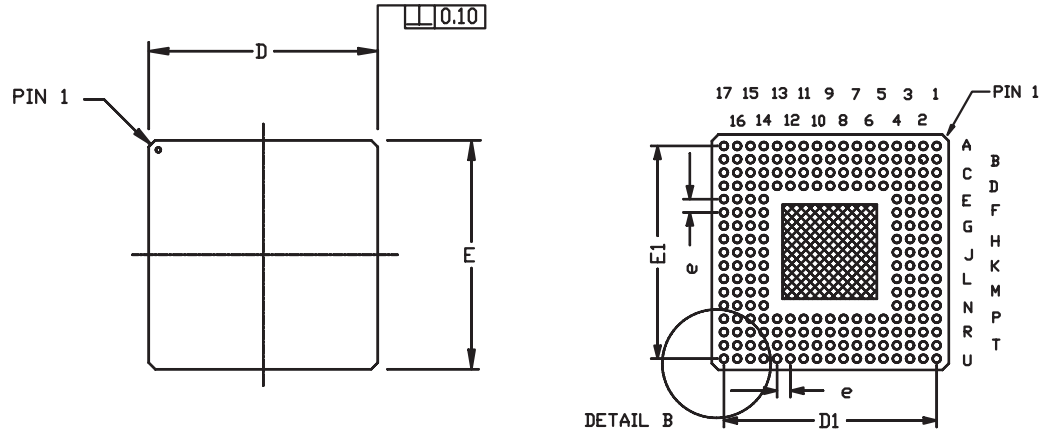
Note: NC used as test pins. Do Not Connect.

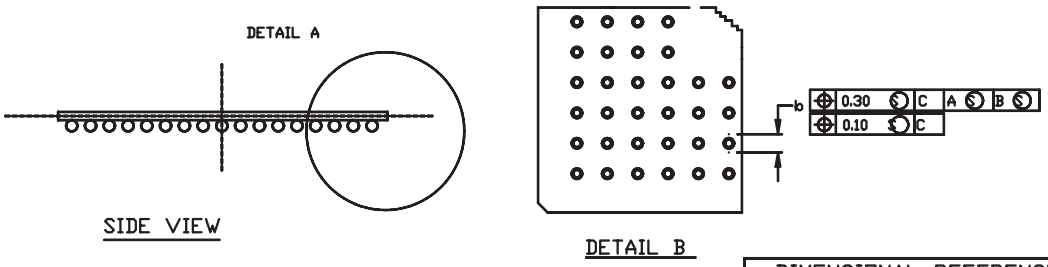
Figure 11. S2204 Pinout (Top View)

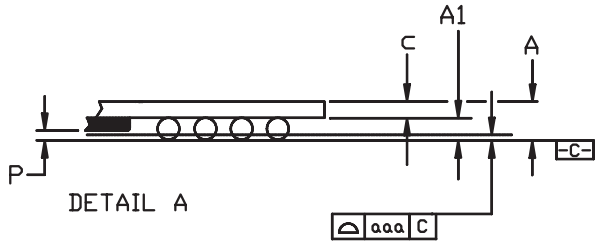
U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
RBC1B	RBC0B	DOUTB7	DOUTB6	DOUTB2	DOUTB0	COM_ DETB	RBC0A	DOUTA7	DOUTA4	DOUTA9	DOUTA1	TTLPWR	TTLGND	DIGGND	DIGPWR	VDDA	1
DOUTC1	DOUTC9	COM_ DETC	DOUTB8	DOUTB4	DOUTB3	DOUTB1	RBC1A	DOUTA5	DOUTA3	DOUTA0	COM_ DETA	TTLGND	DIGGND	CMODE	DIGPWR	RXAP	2
DOUTC4	DOUTC0	DIGGND	DOUTC8	TTLPWR	DOUTB5	TTLGND	DOUTB9	DOUTA6	DOUTA2	DOUTA8	TTLGND	DIGPWR	PWR	DIGGND	TRS	RXAN	3
RBC0C	DOUTC3	TTLGND	TTLGND	DIGGND	TTLGND	DIGPWR	TTLPWR	TTLGND	TTLPWR	TTLPWR	DIGGND	TEST MODE	TEST MODE1	VSSA	VDD	VSS	4
RBC1C	DOUTC5	DOUTC2	TTLPWR										VSSSUB	NC	RXBN	RXBP	5
COM_ DETD	DOUTD9	DOUTC6	TTLGND										VSS	VDD	VDD	VDDA	6
DOUTD1	DOUTD8	DOUTC7	TTLPWR										NC	NC	VSSA	VSSSUB	7
DOUTD2	DOUTD0	TTLGND	TTLPWR										VSSSUB	VDDA	VSSA	RXCP	8
DOUTD5	DOUTD3	DOUTD4	DIGPWR										VDD	NC	NC	RXCN	9
RBC0D	RBC1D	DOUTD6	DIGGND										TDI	TCK	VSS	TMS	10
DOUTD7	DINA0	DINA1	DINA2										VSSA	NC	RXDP	VSS	11
TBCA	DINA4	DINA6	DINA7										RATE	CLKSEL	RXDN	VDD	12
DINA3	DINA5	TBCB	DINB1										CAP1	VSSSUB	TMODE	VDDA	13
DINA8	DINB0	DINB4	DINB6	DINC0	DINC5	TBCD	DIND4	TCLKO	LPEND	LPENB	NC	NC	LPENA	CAP2	VSS	VSSSUB	14
DINA9	DINB5	DINB7	TBCC	DINC2	DINC7	DIND0	DIND5	DIGGND	TDO	LPENC	NC	PECL PWR	PECL PWR	RESET	VSSA	VDD	15
DINB2	DINB8	DINB9	DINC3	DINC6	DIND1	DIND2	DIND6	DIND9	PECLGND	PECL PWR	TXCN	PECL PWR	NC	PECLGND	PWR	VDDA	16
DINB3	DINC1	DINC4	DINC8	DINC9	DIND3	DIND7	DIND8	DIGPWR	REFCLK	TXDN	TXDP	TXCP	TXBN	TXBP	TXAN	TXAP	17

Note: NC used as test pins. Do Not Connect.

Figure 12. Compact 23mm x 23mm 208 TBGA Package







DIMENSIONAL REFERENCES		
DIM LTR	TOL / TBGA	208 TBGA
A	±.10	1.55
A1	±.05	0.65
D	±.20	23.00
D1	20.32 BSC.	
E	±.20	23.00
E1	20.32 BSC.	
b	±.10	0.75
c	±.05	0.90
M	17	
N	208	
aaa	MAX.	0.15
ccc	MAX.	0.15
e	1.27 TYP.	
P	MAX.	0.25

Thermal Management

Device	Θja (Still Air)	Θjc
S2204	17.7˚ C/W	3.5˚ C/W

Figure 13. Transmitter Timing (REFCLK Mode, TMODE = 0)

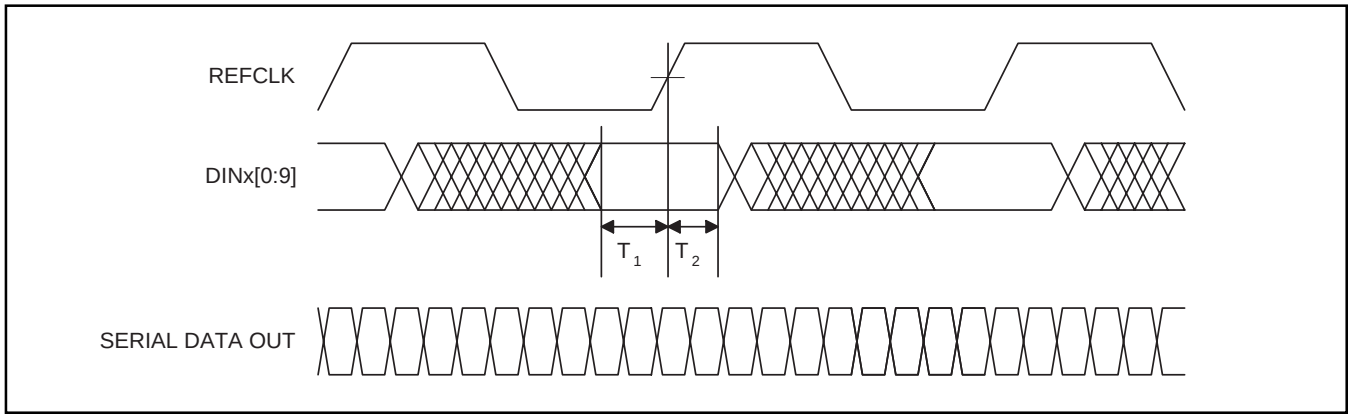


Table 15. S2204 Transmitter Timing (REFCLK Mode, TMODE = 0)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ REFCLK	0.5	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ REFCLK	1.5	-	ns	

1. All AC measurements are made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 14. Transmitter Timing (TBC Mode, TMODE = 1)

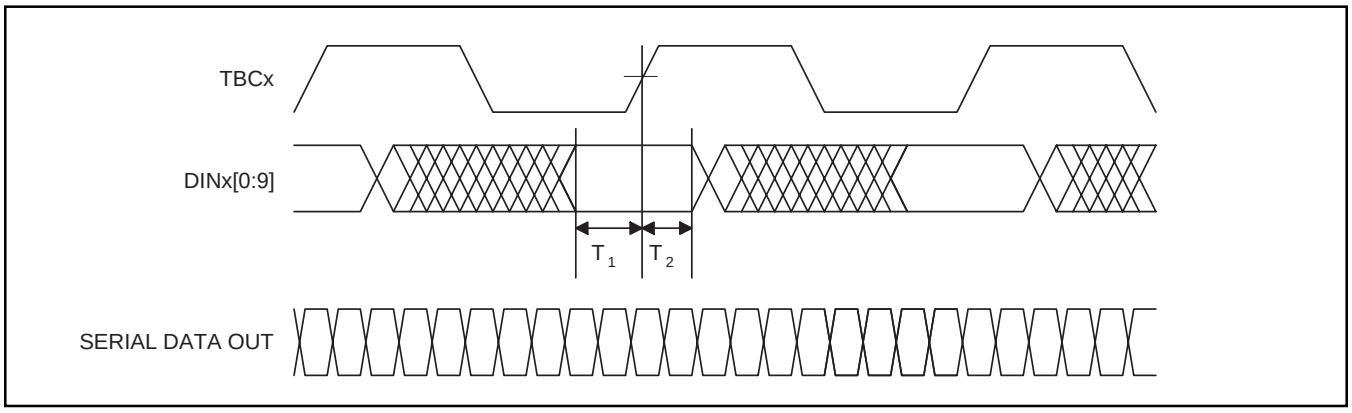


Table 16. S2204 Transmitter Timing (TBC Mode, TMODE = 1)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ TBC	1.0	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ TBC	0.5	-	ns	
	Phase drift between TBCx and REFCLK	-3	+3	ns	

1. All AC measurements are made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Table 17. S2204 Receiver Timing (Full and Half Clock Mode)

Parameters	Description	Min	Max	Units	Conditions
T_3	Data Setup w.r.t.↑ RBC1/0x	2.5		ns	at 1.25 Gbps [1,2] TMODE = 1
T_4	Data Hold w.r.t.↑ RBC1/0x	2.5		ns	TMODE = 1
T_5	Data Setup w.r.t.↑ RBC1/0x	2.5		ns	at 1.25 Gbps [1,2] TMODE = 1
T_6	Data Hold w.r.t.↑ RBC1/0x	2.5		ns	TMODE = 1
T_7	Time from RBC1x rise to RBC0x rise	7.5	8.5	ns	at 1.25 Gbps [1,2]
T_{R1}, T_{F1}	RBC1x Rise and Fall Times		2.4	ns	See note 2. See Figure 20.
T_{R0}, T_{F0}	RBC0x Rise and Fall Times		2.4	ns	See note 2. See Figure 20.
T_{DR}, T_{DF}	DOUTx Rise and Fall Times		2.4	ns	See note 2. See Figure 19.
Duty Cycle	RBC1/0x Duty Cycle	40	60	%	See note 1.

1. Measurements made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).
2. TTL/CMOS AC timing measurements are assumed to have an output load of 10pf.

Table 18. S2204 Receiver Timing (External Clock Mode)

Parameters	Description	Min	Max	Units	Conditions
T_8	TBCA to DOUTx Propagation Delay	3.0	8.0	ns	10 pf load capacitance at the end of a 3 inch 50 Ω transmission line.

1. Measurements made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 15. Receiver Timing (Full Clock Mode, CMODE = 1)

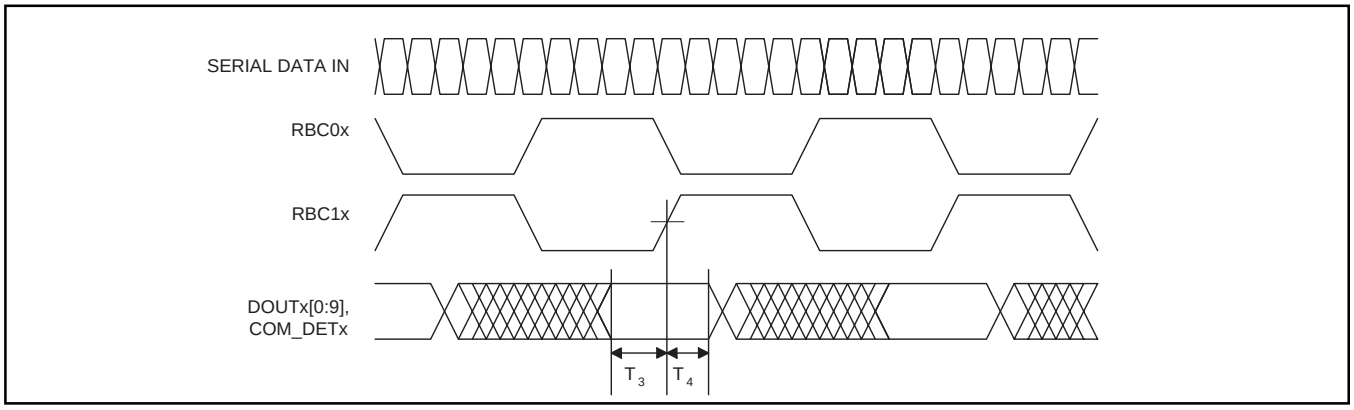


Figure 16. Receiver Timing (Half Clock Mode, CMODE = 0, TMODE = 1)

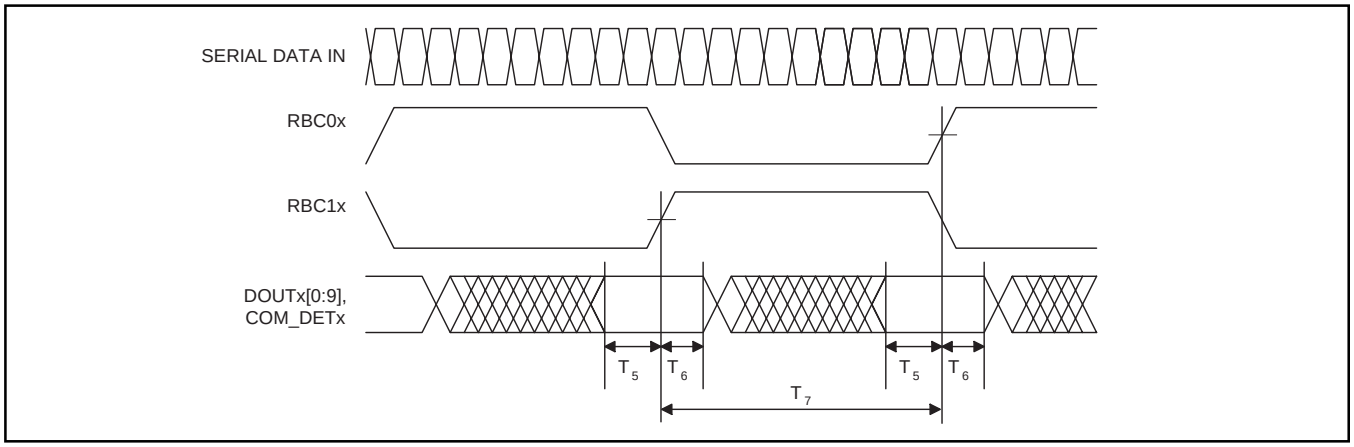


Figure 17. Receiver Timing (External Clock Mode)
(TBCA to DATA Propagation Delay, TMODE = 0)

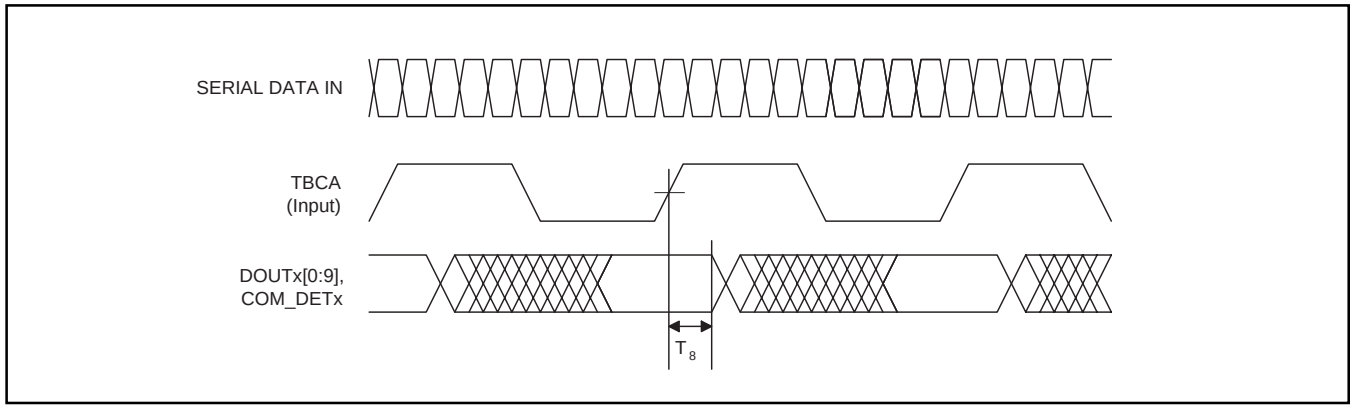


Figure 18. TCLKO Timing

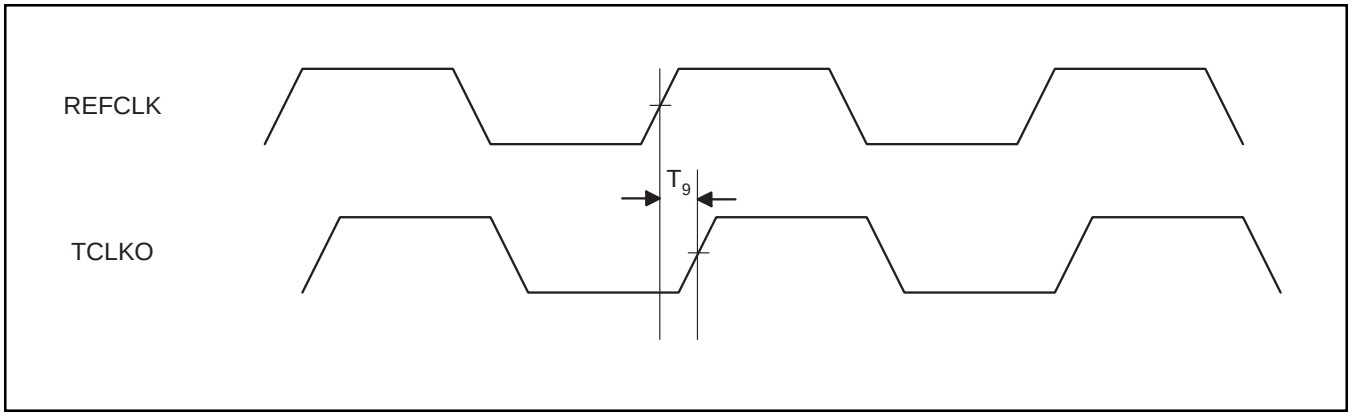


Table 19. S2204 Transmitter (TCLKO Timing)

Parameters	Description	Min	Max	Units	Conditions
T_9	↑ TCLKO w.r.t. ↑ REFCLK	1.0	6.5	ns	
TCLKO Duty Cycle		45%	55%	%	

Note: Measurements are made at 1.4V level of clocks.

Table 20. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on VDD with Respect to GND	-0.5		+5.0	V
Voltage on any TTL Input Pin	-0.5		3.47	V
Voltage on any PECL Input Pin	0		VDD	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			25	mA
ESD Sensitivity [1]	Over 500 V			

1. Human body model.

Table 21. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on any Power Pin with respect to GND/VSS	3.13	3.3	3.47	V
Voltage on TTL Input Pin	0		3.47	V
Voltage on any PECL Input Pin	VDD -2V		VDD	V

Table 22. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% - 80%.
—	Jitter		80	ps	Peak-to-Peak, to maintain ≥ 77% eye opening.

Table 23. Serial Data Timing, Transmit Outputs

Parameters	Description	Min	Typ	Max	Units	Comments
Total Jitter	Serial Data Output total jitter			192	ps	Peak-to-Peak.
T_{DJ}	Serial Data Output deterministic jitter			80	ps	Peak-to-Peak.
T_{SR}, T_{SF}	Serial Data Output rise and fall time			300	ps	20% - 80%.

Table 24. Serial Data Timing, Receive Inputs

Parameters	Description	Min	Typ	Max	Units	Comments
T_{LOCK} (Frequency)	Frequency Acquisition Lock Time (Loss of Lock) (1.25 Gbps)			175	µs	8B/10B idle pattern sample basis, from device start up.
T_{DJ}	Deterministic Input Jitter Tolerance	370			ps	As specified by IEEE 802.3z.
Input Jitter Tolerance	Serial Data Input total jitter tolerance	599			ps	Peak-to-Peak, as specified by IEEE 802.3z.
R_{SR}, R_{SF}	Serial Data Input rise and fall time			330	ps	20% - 80%.

Table 25. DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL)	2.4	2.8	VDD	V	VDD = min I_{OH} = -4mA
V_{OL}	Output Low Voltage (TTL)	GND	.025	0.5	V	VDD = min I_{OL} = 4mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4 V, VDD = Max
I_{IL}	Input Low Current (TTL)			600	µA	V_{IN} = .8 V, VDD = Max
IDD	Supply Current		760	980	mA	1010 Pattern.
P_D	Power Dissipation		2.5	3.4	W	1010 Pattern.
V_{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		2600	mV	See Figure 22.
ΔV_{OUT}	Differential Serial Output Voltage Swing	1400		2600	mV	See Figure 21.
C_{IN}	Input Capacitance			3	pf	

OUTPUT LOAD

The S2204 serial outputs do not require output pulldown resistors.

ACQUISITION TIME

With the input eye diagram shown in Figure 24, the S2204 will recover data with a ≤1E-9 BER within the time specified by T_{LOCK} in Table 24 after an instantaneous phase shift of the incoming data.

Figure 19. Serial Input/Output Rise and Fall Time

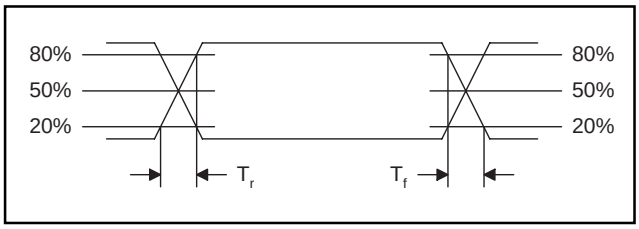


Figure 20. TTL Input/Output Rise and Fall Time

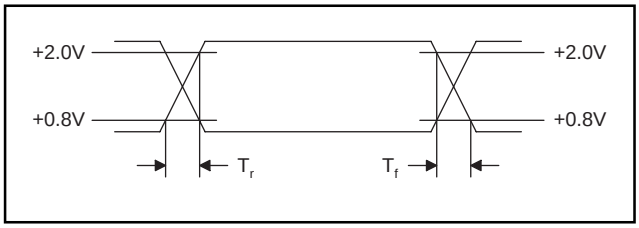


Figure 21. Serial Output Load

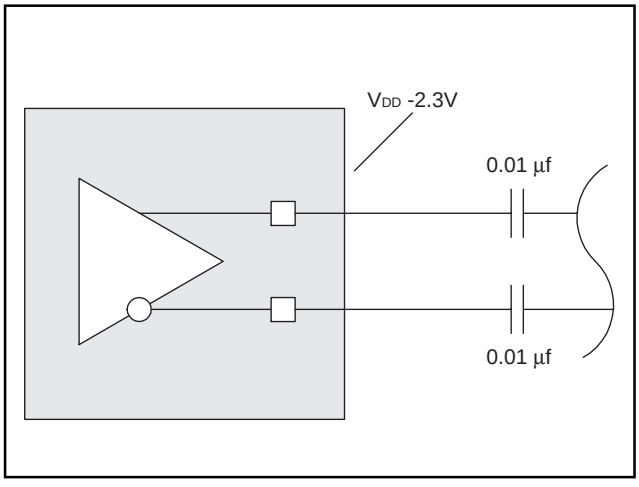


Figure 22. High Speed Differential Inputs

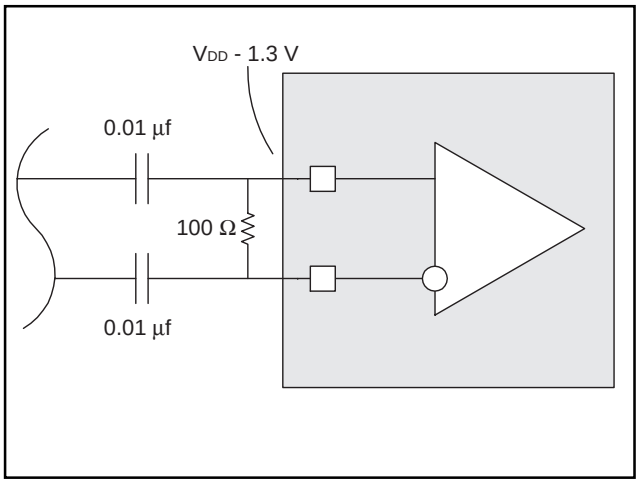


Figure 23. Receiver Input Eye Diagram Jitter Mask

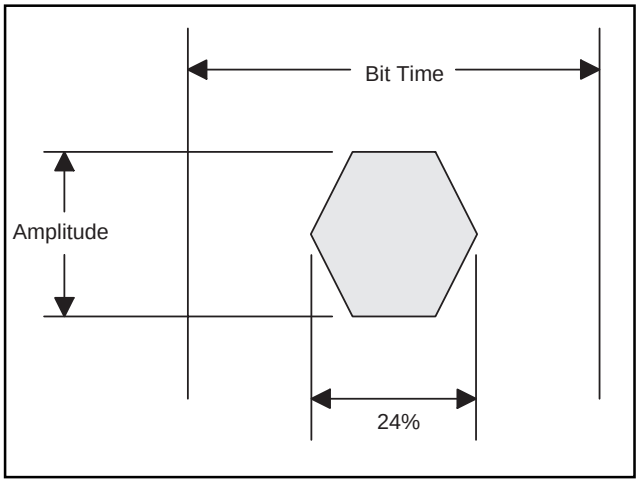


Figure 24. Acquisition Time Eye Diagram

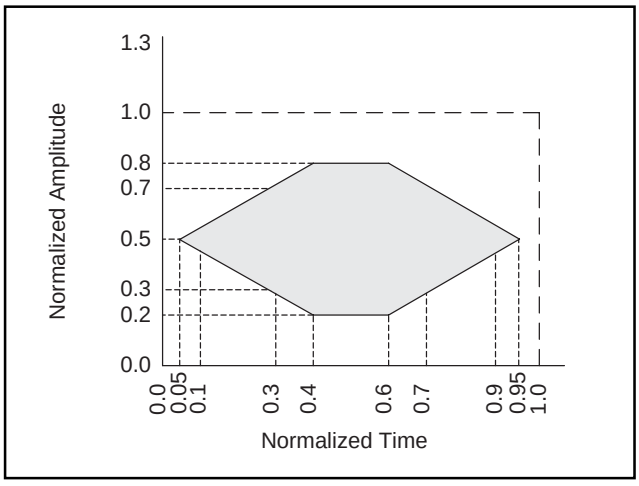
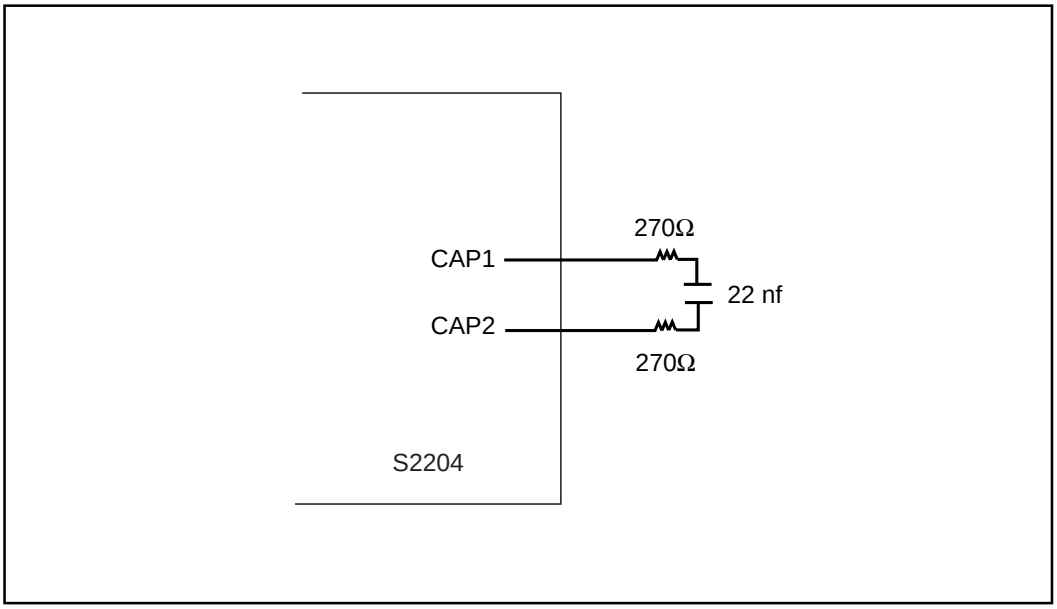
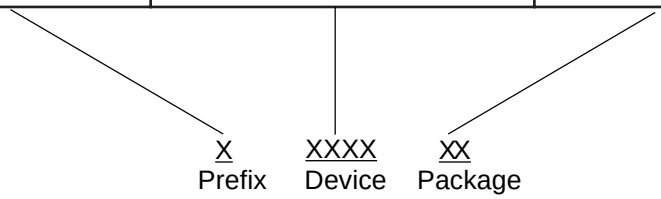


Figure 25. Loop Filter Capacitor Connections



Ordering Information

PREFIX	DEVICE	PACKAGE
S- Integrated Circuit	2204	TB – 208 TBGA



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