Precision Voltage Supervisory Circuit With Watchdog Timer and 4K I²C Memory

3 and 5 Volt Systems

FEATURES

- **Precision Dual Voltage Monitor**
  - **Automatic V_{CC} Supply Monitor**
    - **Dual reset outputs for complex microcontroller systems**
    - **Integrated memory write lockout function**
    - **No external components required**
- **Second voltage monitor output**
  - **Separate V_{LOW} output**
  - **Generates interrupt to MCU**
  - **Generates RESET for dual supply systems**
    - **Guaranteed output assertion to $V_{CC} \leq 1V$**
- **Watchdog Timer**
  - **Nominal 1.6 second Timeout**
- **Memory Internally Organized 512K X 8**
  - **Two Wire Serial Interface (I²C™)**
- **High Reliability**
  - **Endurance: 1,000,000 erase/write cycles**
  - **Data retention: 100 years**
- **8-Pin PDIP or SOIC Packages**

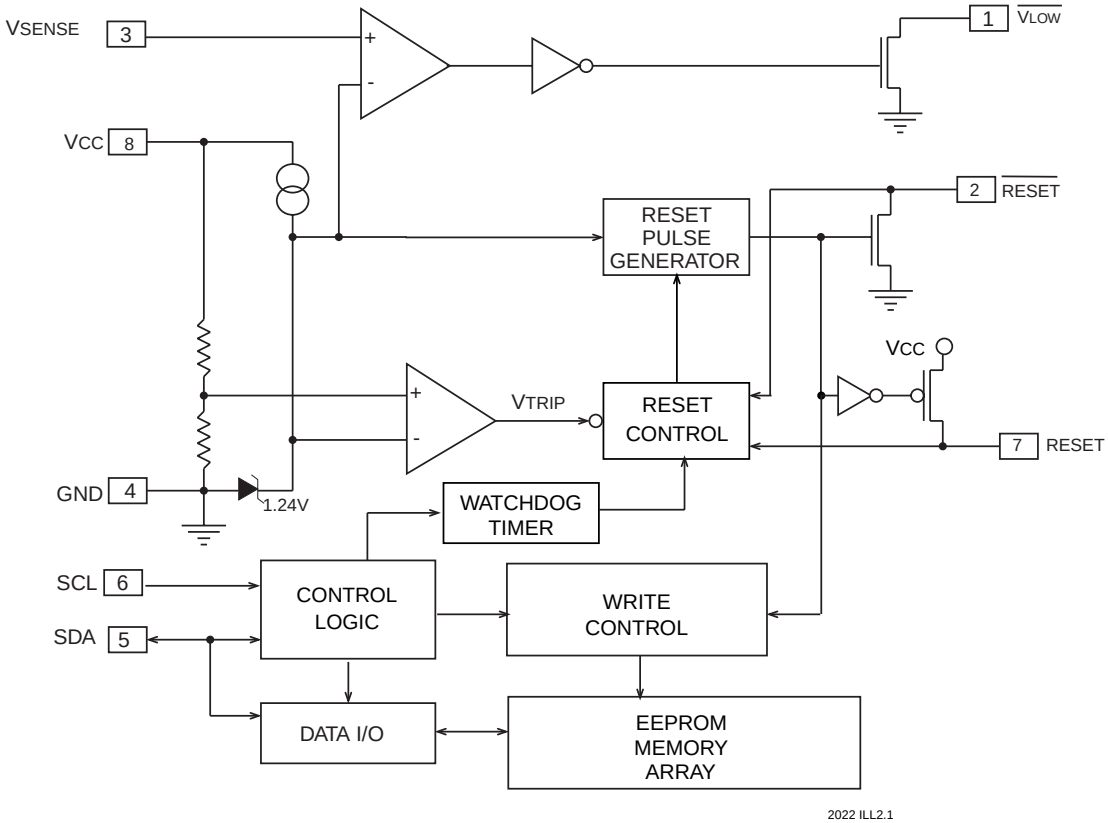
OVERVIEW

The S42WD42 is a precision power supervisory circuit. It automatically monitors the device's V_{CC} level (3V or 5V) and will generate a reset output on two complementary open drain outputs. In addition to the V_{CC} monitoring, the S42WD42 also provides a second voltage comparator input. This input has an independent open drain output that can be wire-OR'ed with the $\overline{\text{RESET}}$ I/O or it can be used as a system interrupt.

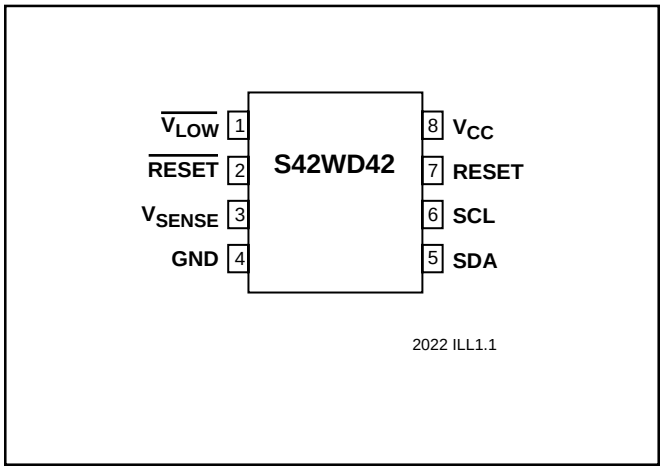
In addition to the reset circuitry, the S42WD42 also has a watchdog timer. The nominal timeout period is 1.6 seconds. If the watchdog is not cleared within 1.6 seconds it will generate a reset condition.

The S42WD42 also has an integrated 4K-bit nonvolatile memory. The memory conforms to the industry standard two-wire serial interface.

BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

Symbol	Pin	Description
$\overline{V_{LOW}}$	1	Open Drain Output Active When V_{SENSE} is < 1.24V
$\overline{RESET}$	2	Active Low $\overline{RESET}$ Input/Output
V_{SENSE}	3	Second Monitor Voltage Input. When less than 1.24V the $\overline{V_{LOW}}$ output will be driven
GND	4	Analog and Digital Ground
SDA	5	Serial Memory Input/Output data line
SCL	6	Serial Memory clock input
RESET	7	Active High RESET Input/Output
V_{CC}	8	Supply Voltage

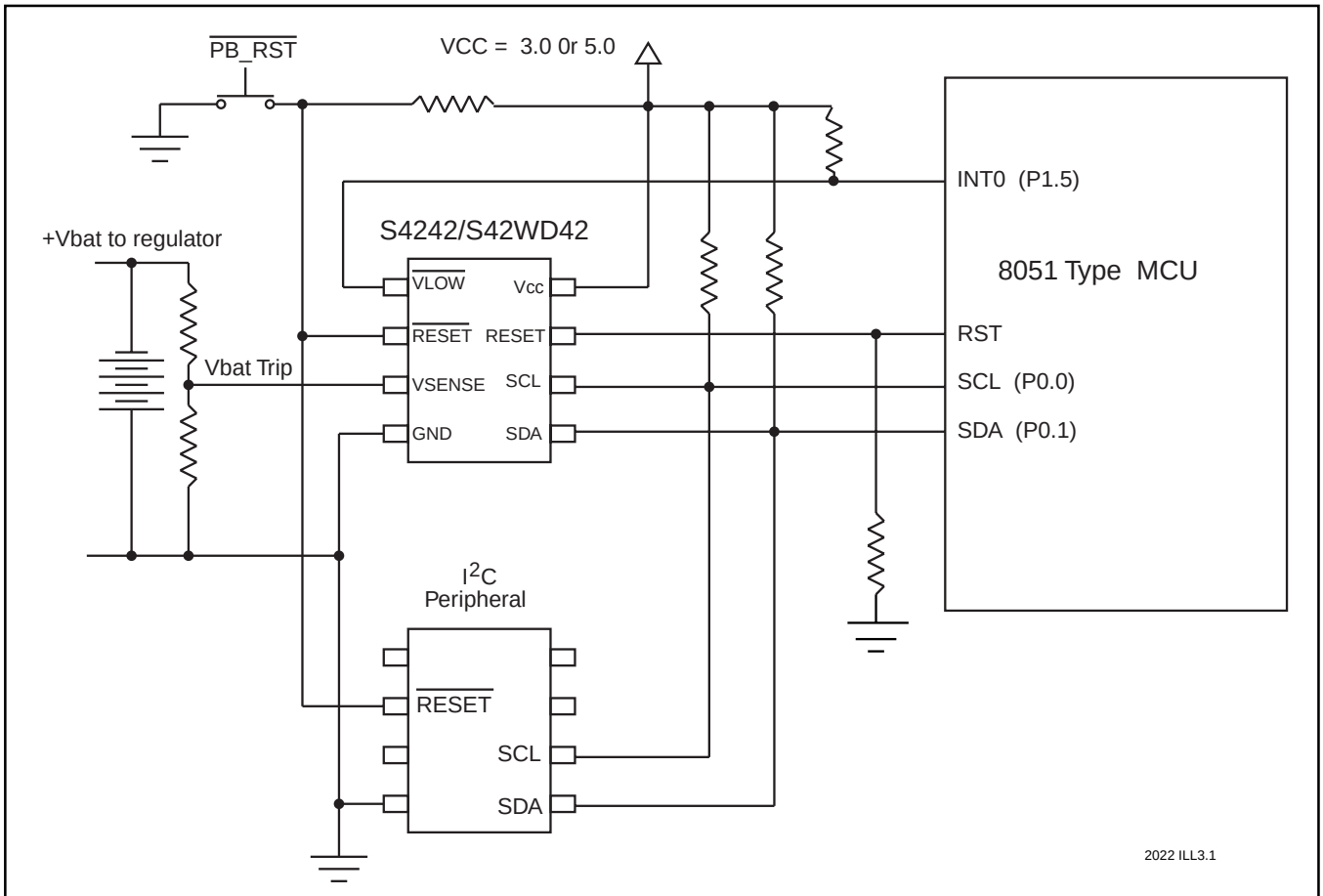


FIGURE 1. TYPICAL SYSTEM CONFIGURATION USING A PUSH BUTTON RESET AND BATTERY MONITOR CIRCUIT

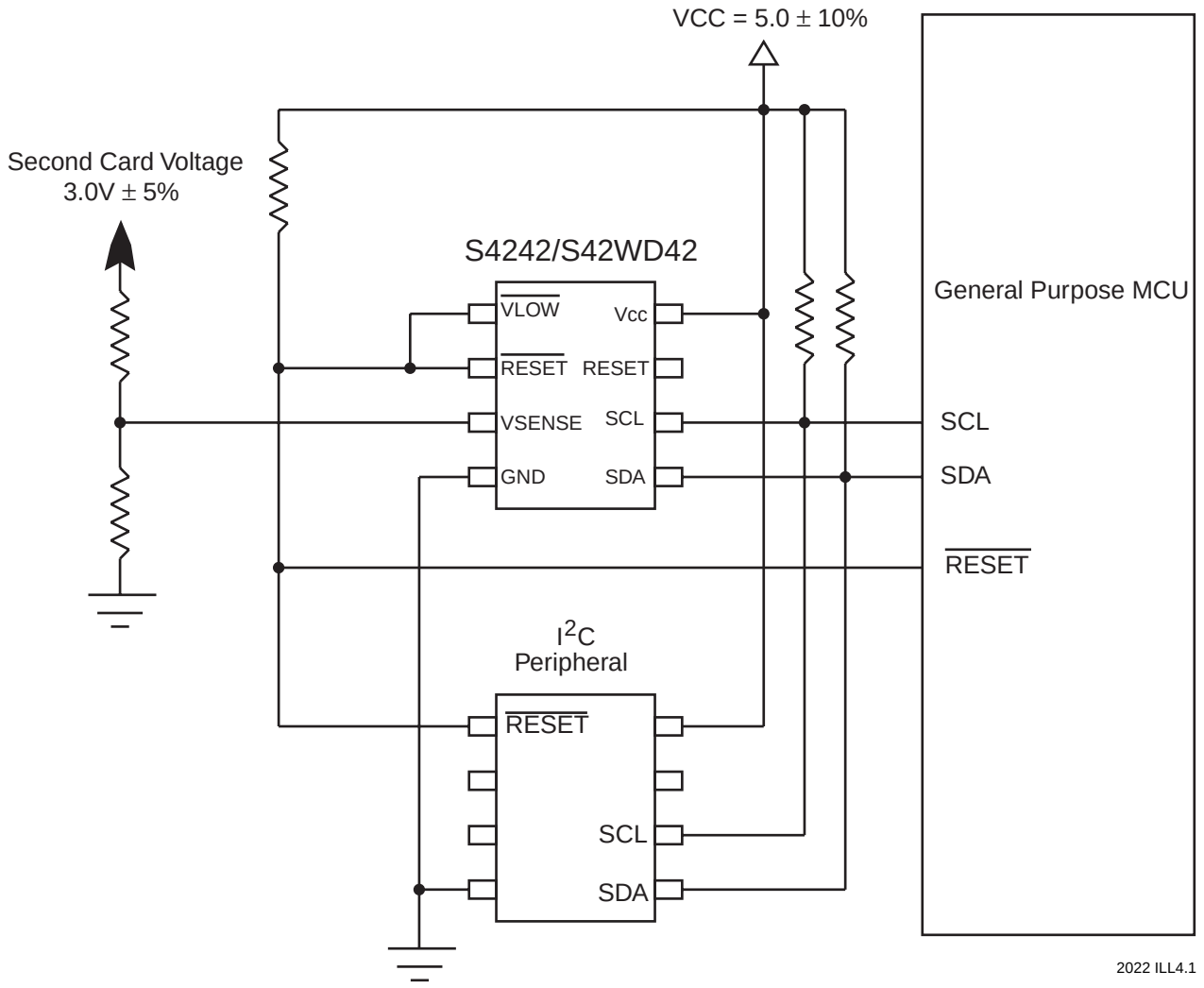


FIGURE 2. TYPICAL SYSTEM CONFIGURATION FOR DUAL RESET WITH V_{CC} MONITOR AND 3.3VOLT MONITOR

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -40°C to +85°C
Storage Temperature ..... -65°C to +125°C
Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3V to V_{CC}+0.3V
ESD Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	V_{CC} =5.5V		3	mA
			V_{CC} =3.3V		2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	V_{CC} =5.5V		50	µA
			V_{CC} =3.3V		25	µA
I_{LI}	Input Leakage	V_{IN} = 0 To V_{CC}			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 To V_{CC}			10	µA
V_{IL}	Input Low Voltage	SCL, SDA, $\overline{\text{RESET}}$ (pin 2)			0.3xV_{CC}	V
V_{IH}	Input High Voltage	SCL, SDA, RESET (pin7)			0.7xV_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA SDA			0.4	V

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AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

			2.7V to 4.5V		4.5V to 5.5V		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		µs
t_{HIGH}	Clock High Period		4.0		0.6		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		µs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

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CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
CIN	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

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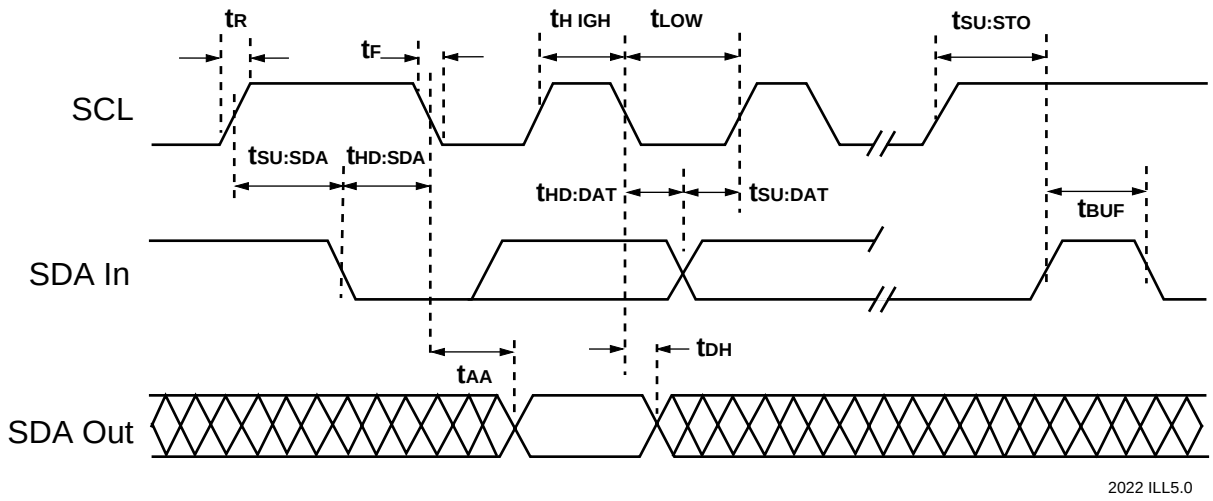

FIGURE 3. BUS TIMING

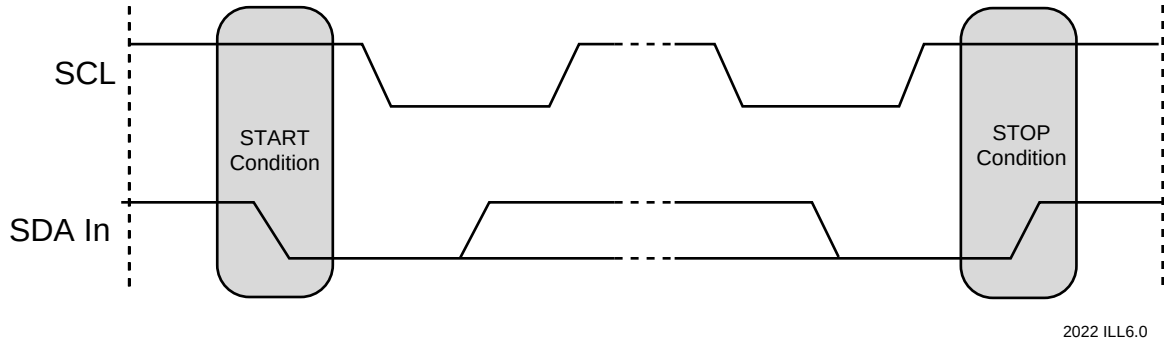

FIGURE 4. START AND STOP CONDITIONS

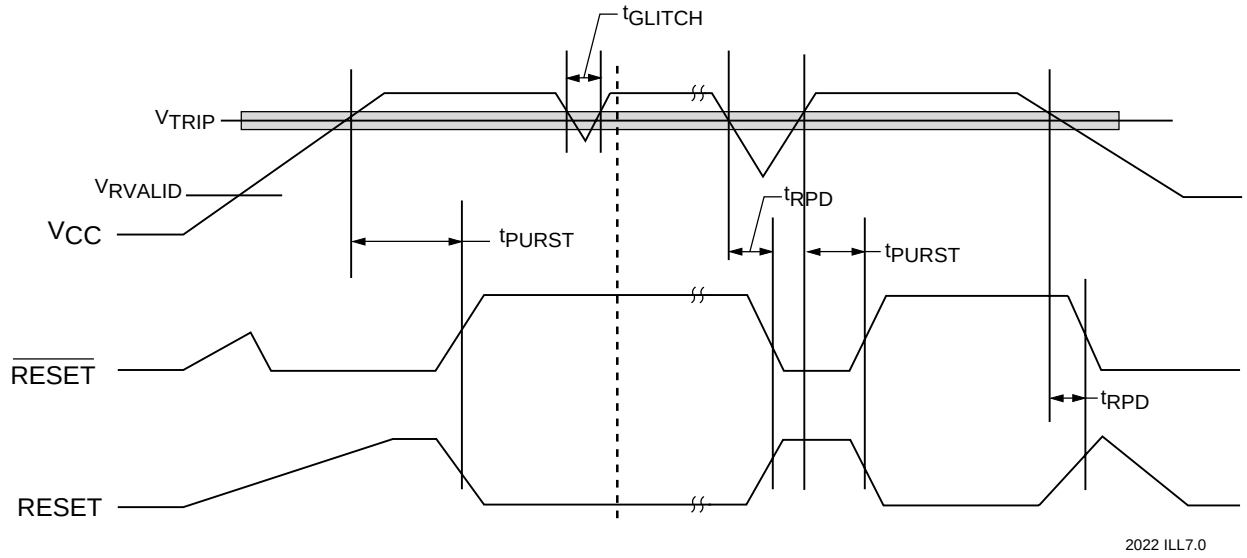

FIGURE 5. RESET OUTPUT TIMING

RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C

		S42WD42-2.7		S42WD42–A		S42WD42–B		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{TRIP}	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
t_{PURST}	Power-Up Reset Timeout	130	270	130	270	130	270	ms
t_{RPD}	V_{TRIP} to RESET Output Delay		5		5		5	µs
V_{RVALID}	$\overline{\text{RESET}}$ Output Valid	1		1		1		V
t_{GLITCH}	Glitch Reject Pulse Width		30		30		30	ns
V_{OLRS}	$\overline{\text{RESET}}$ Output Low Voltage I_{OL}= 1mA		0.4		0.4		0.4	V
V_{OHRS}	RESET Output High Voltage I_{OH} = 800 µA	V_{CC}-.75		V_{CC}-.75		V_{CC}-.75		V
$V_{SENSE}T$	Voltage Sense Trip Point	1.22	1.25	1.22	1.25	1.22	1.25	V
$V_{SENSE}H$	Voltage Sense Hysteresis		10		10		10	mV

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PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

$\overline{\text{RESET}}$ - $\overline{\text{RESET}}$ is an active low open-drain output. It should be tied high through a pull-up resistor connected to V_{CC}. $\overline{\text{RESET}}$ is an I/O, therefore it may also be used to condition a $\overline{\text{RESET}}$ signal generated by another device; it can also be used to debounce a pushbutton input.

RESET - RESET is an active high open drain (PFET) output. It should be tied low through a pull-down resistor connected to ground. RESET is an I/O, therefore it may also be used to condition a RESET signal generated by another device.

V_{SENSE} - The V_{SENSE} input is used as a second voltage sensing input. The pin is tied to a comparator that uses the precision internal 1.24V reference.

$\overline{V_{LOW}}$ - The $\overline{V_{LOW}}$ output is an open drain which is driven low whenever the V_{SENSE} input is less than 1.24V. For correct operation this output should be tied high through a pull-up resistor connected to V_{CC}.

ENDURANCE AND DATA RETENTION

The S42WD42 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

Reset Controller Description

The S42WD42 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output. For proper operation pin 7 should be tied low through a pull-down resistor while pin 2 should be tied high through a resistor connected to V_{CC}.

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP}. The RESET outputs will be valid so long as V_{CC} is > 1.0V. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP}.

The RESET pins are I/Os; therefore, the S42WD42 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition. Refer to the applications information section for more details on device operation as a reset conditioning circuit.

Voltage Sensor Description

The S42WD42 provides an additional voltage sensor which is internally compared to the internal 1.24 volt reference voltage. Whenever the V_{SENSE} input is below 1.24 volts, the $\overline{V_{LOW}}$ output will be driven low. An external resistor divider is used to set the desired system trip voltage.

This input can be used in two manners. The first example might be to sense unregulated DC or battery voltage in a battery powered application and to generate an interrupt in the case of either a low voltage from the battery or the failure of power in the system. The system power supply can then be designed to insure that the output capacitance is high enough to provide sufficient time to perform housekeeping tasks, such as the storing of the system status in the E^2PROM, prior to the assertion of the RESET signal. (Figure 1)

The second use for this input might be to sense a second power supply level, such as 3.3 volts in a dual voltage system. In this case, the $\overline{V_{LOW}}$ output could be connected to the $\overline{\text{RESET}}$ output to generate a reset condition whenever either supply is not valid. (Figure 2)

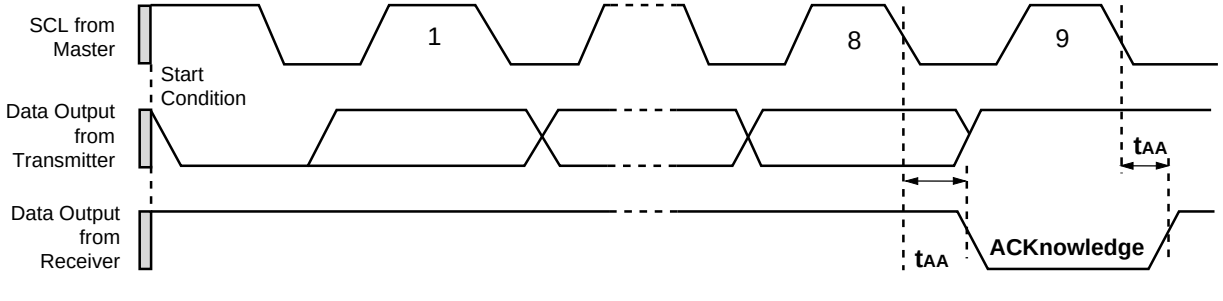


FIGURE 6. ACKNOWLEDGE RESPONSE FROM RECEIVER

CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition, refer to Figure 4.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the “START” condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the “STOP” condition (See Figure 4).

DEVICE OPERATION

The S42WD42 is a 16K-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a “transmitter” and any device which receives data as a “receiver.” The device controlling data transmission is called the “master” and the controlled device is called the “slave.” In all cases, the S42WD42 will be a “slave” device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 6).

The S42WD42 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S42WD42 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S42WD42 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S42WD42 will continue to transmit data. If an ACKnowledge is not detected, the S42WD42 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 7). For the S42WD42 this is fixed as 1010[B].

Word Address

The next two bits are don’t care. The next bit is an extension of the array’s address and is concatenated with the eight bits of address in the word address field, providing direct access to the 512 X 8 array.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to “1,” a read operation is selected; when set to “0,” a write operation is selected.

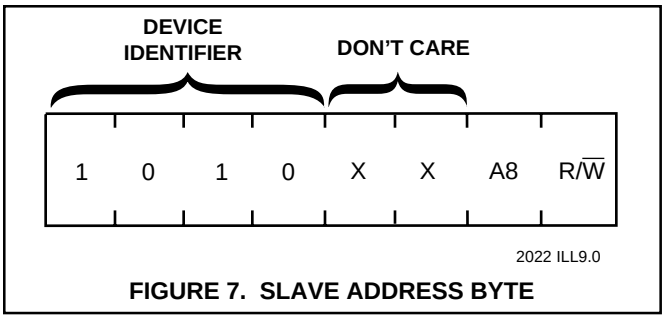


FIGURE 7. SLAVE ADDRESS BYTE

WRITE OPERATIONS

The S42WD42 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR}.

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 512 words in the array.

Upon receipt of the word address, the S42WD42 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S42WD42 begins the internal write cycle.

While the internal write cycle is in progress, the S42WD42 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S42WD42 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S42WD42 will respond with an ACKnowledge.

The S42WD42 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will “roll over,” and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

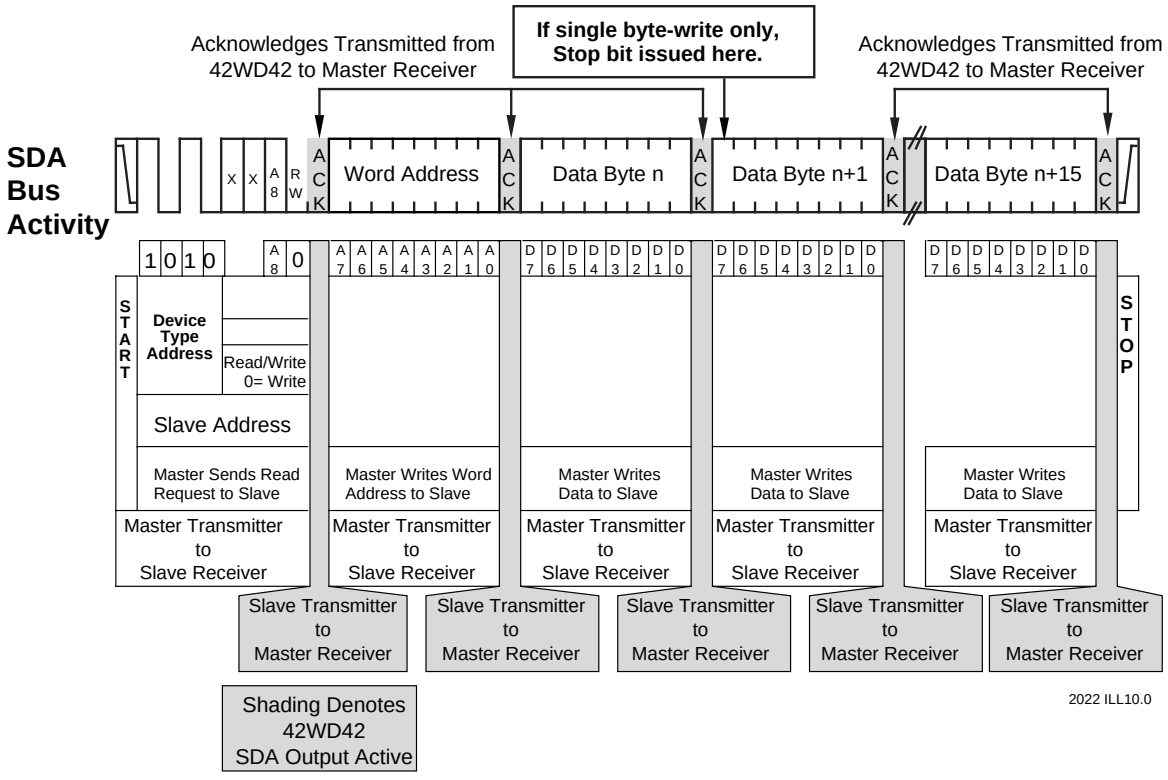


FIGURE 8. PAGE/BYTE WRITE MODE

Acknowledge Polling

When the S42WD42 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).

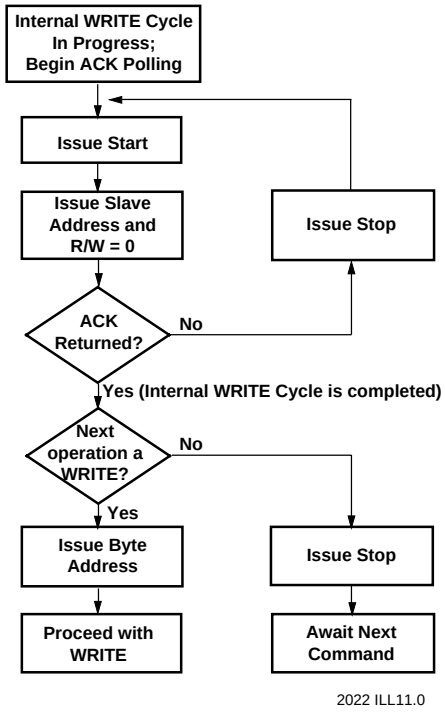


FIGURE 9. ACKNOWLEDGE POLLING

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S42WD42 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the S42WD42 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S42WD42 discontinues data transmission. See Figure 10 for the address acknowledge and data transfer sequence.

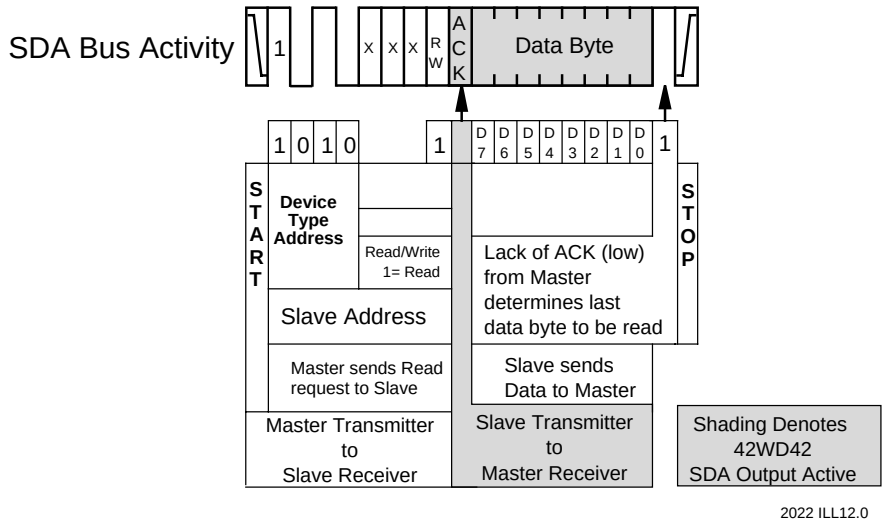


FIGURE 10. CURRENT ADDRESS BYTE READ MODE

Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S42WD42 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S42WD42 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S42WD42 discontinues data transmission and reverts to its standby power mode. See Figure 11 for the address, acknowledge and data transfer sequence.

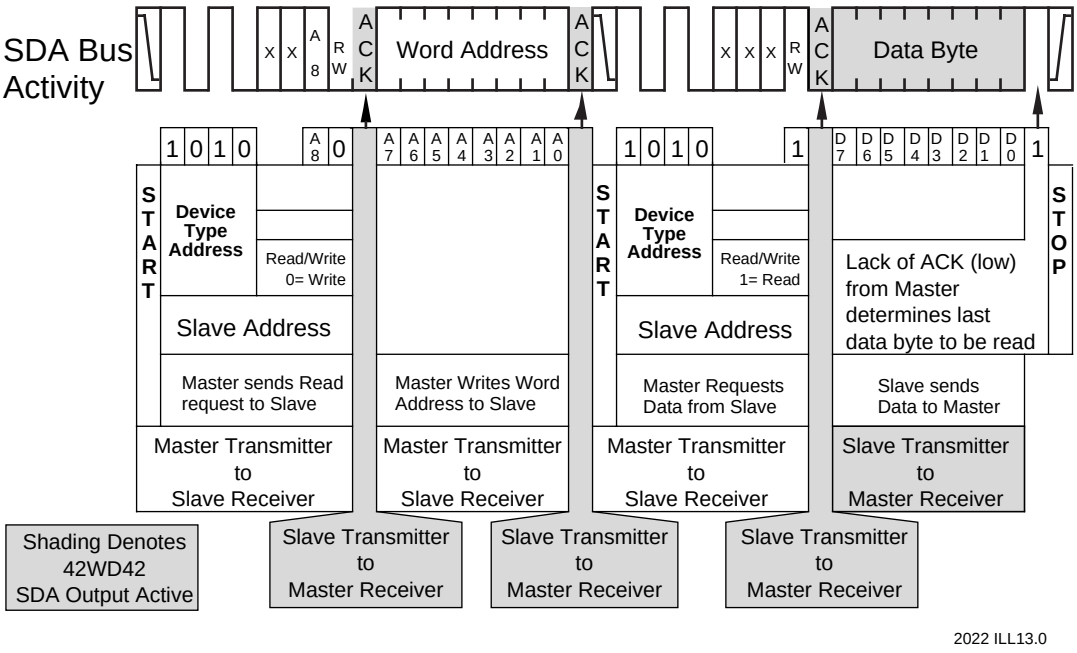


FIGURE 11. RANDOM ADDRESS BYTE READ MODE

Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S42WD42. The S42WD42 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 12 for the address, acknowledge and data transfer sequence.

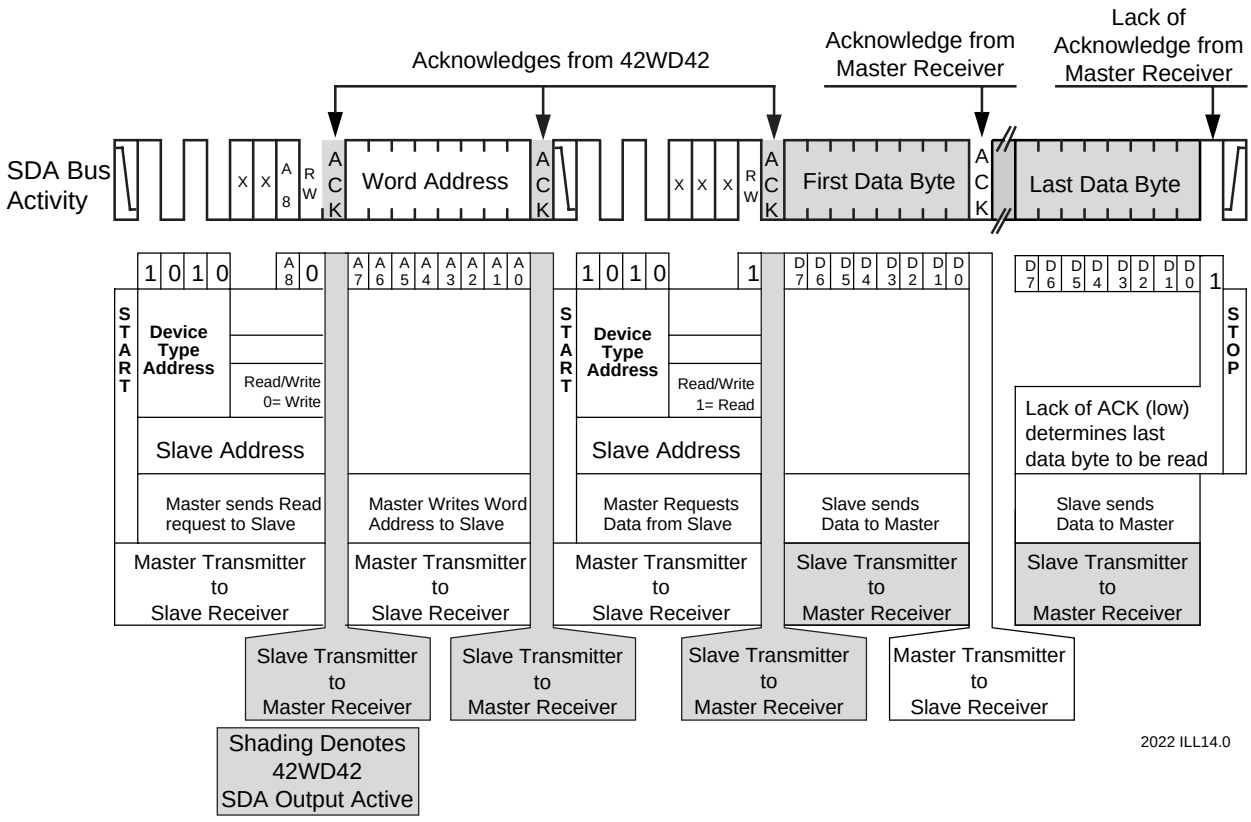


FIGURE 12. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

Watchdog Timer Operation

The S42WD42 has a watchdog timer with a nominal timeout period of 1.6 seconds. Whenever the watchdog times out it will generate a reset output on both $\overline{\text{RESET}}$ and RESET. The watchdog timer will reset to t_0 whenever the S42WD42 issues an ACKnowledge. Therefore, the host system will need to issue a start condition, followed by a valid address and command. It can be a normal command as in the sequence of reading or writing to the memory, or it can be a dummy command issued solely for the purpose of resetting the watchdog timer. Refer to Figure 15 for detailed sequence of operations.

The watchdog timer will be held in the reset state during power-on while V_{CC} is less than V_{TRIP}. Once V_{CC} exceeds V_{TRIP}, the watchdog will continue to be held in a reset state for the duration of t_{PURST}. After t_{PURST}, the timer will be released and begin counting.

If either reset input is asserted the watchdog timer will be reset and remain in the reset condition until either t_{PURST} has expired or the reset input is released, whichever is longer.

If the watchdog times out and no action is taken by the host, the S42WD42 will drive the reset outputs active for the duration of t_{PURST} at which point it will release the outputs and begin the watchdog timer again. Refer to Figure 16 for detailed sequence of operations.

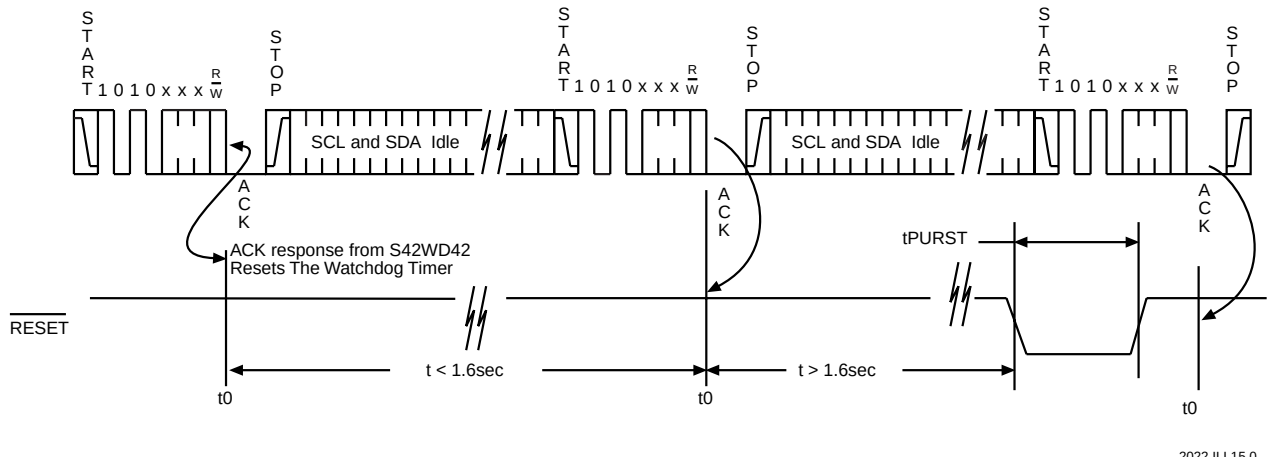


FIGURE 15. SEQUENCE ONE

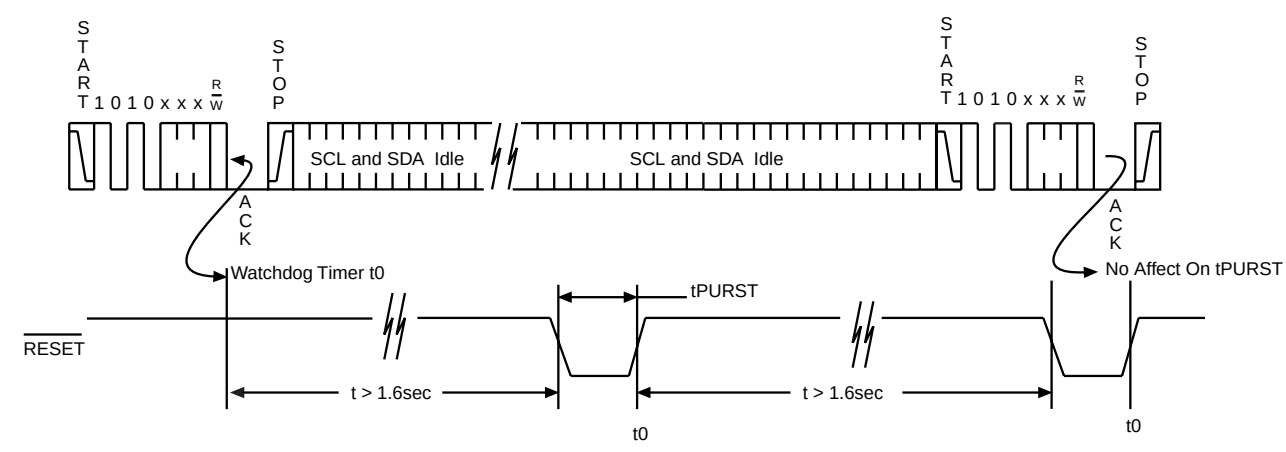
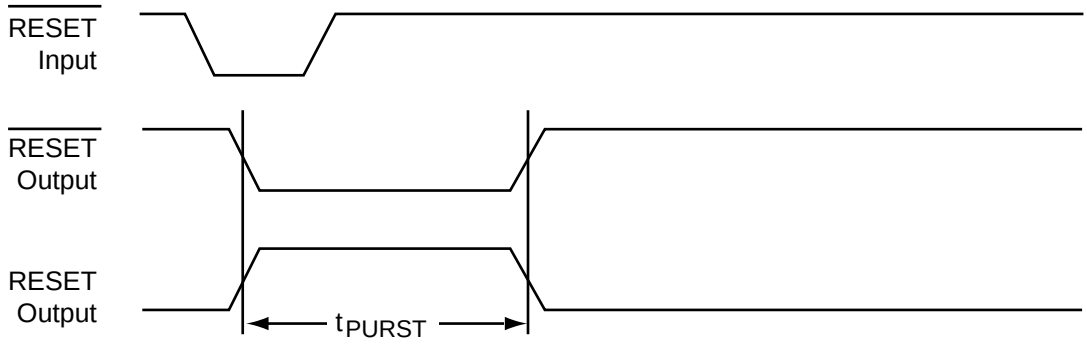


FIGURE 16. SEQUENCE TWO

Applications Info

Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S42WD42 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST}. The same reset output affect can be attained by using the active high reset input.



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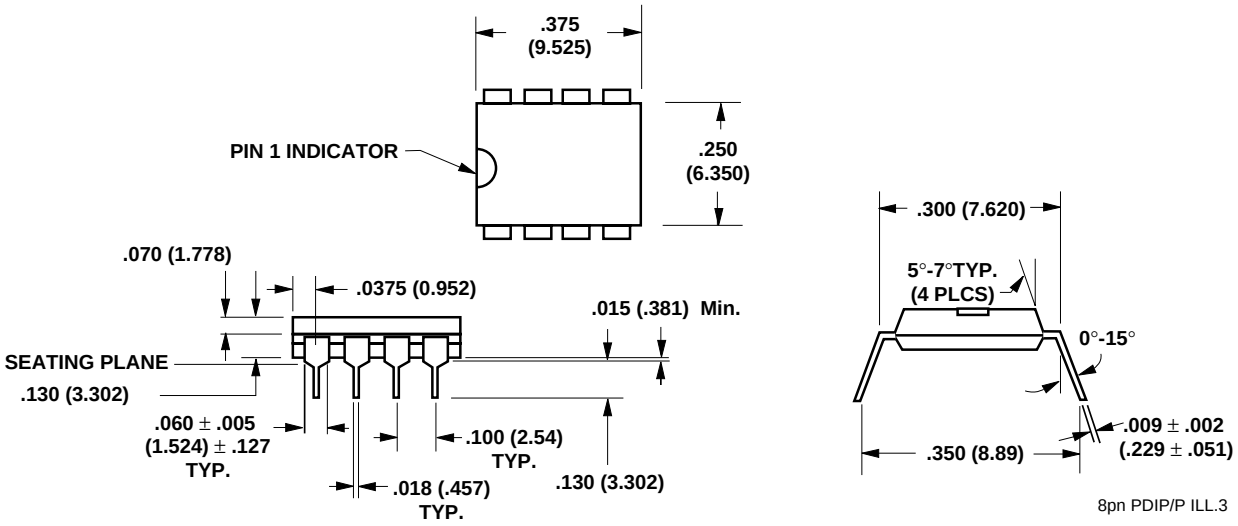
When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
$\overline{\text{RESET}}$ Output Voltage	V_{OL}	V_{CC} = 1.0V, I_{OL}=100µA			0.3	V
		V_{CC} = 1.2V, I_{OL}=100µA			0.3	V
		V_{CC} = 3.0V, I_{OL}=500µA			0.3	V
		V_{CC} = 3.6V, I_{OL}=500µA			0.3	V
		V_{CC} = 4.5V, I_{OL}=750µA			0.3	V
$\overline{\text{RESET}}$ Output Voltage	V_{OL}	V_{CC} = 1.0V, I_{OL}=100µA			0.4	V
		V_{CC} = 1.2V, I_{OL}=150µA			0.4	V
		V_{CC} = 3.0V, I_{OL}=750µA			0.4	V
		V_{CC} = 3.6V, I_{OL}=1mA			0.4	V
		V_{CC} = 4.5V, I_{OL}=1mA			0.4	V
RESET Output Voltage	V_{OH}	V_{CC} = 1.0V, I_{OH}=400µA	V_{CC}-0.75			V
		V_{CC} = 1.2V, I_{OH}=800µA	V_{CC}-0.75			V
		V_{CC} = 3.0V, I_{OH}=800µA	V_{CC}-0.5			V
		V_{CC} = 3.6V, I_{OH}=800µA	V_{CC}-0.5			V
		V_{CC} = 4.5V, I_{OH}=800µA	V_{CC}-0.5			V

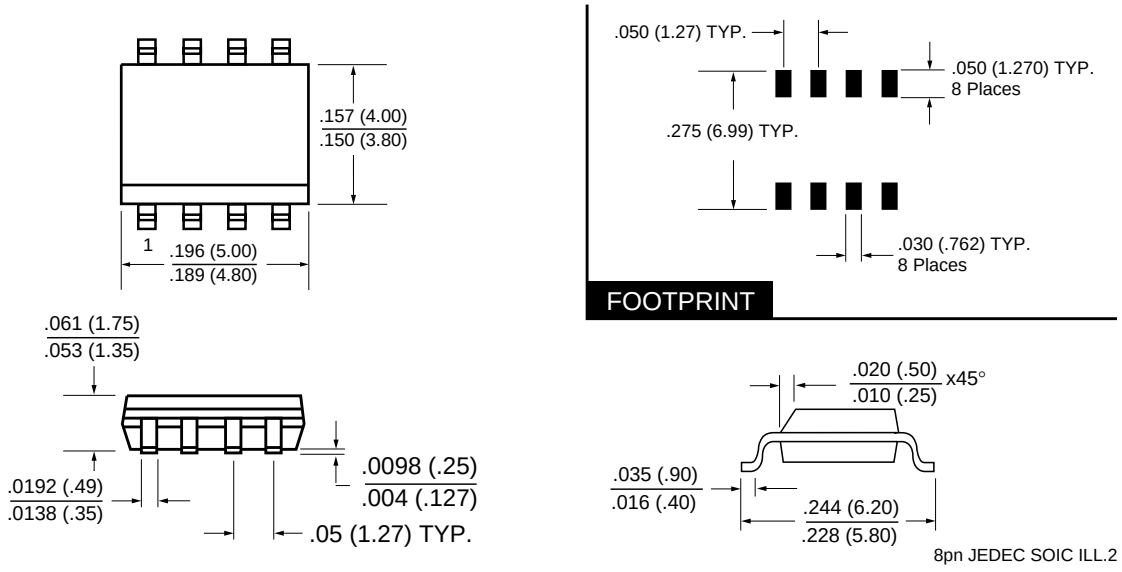
2022 PGM T6.0

8 Pin PDIP (Type P) Package



8pn PDIP/P ILL.3

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)



8pn JEDEC SOIC ILL.2

ORDERING INFORMATION