S3024

DEVICE SPECIFICATION

SONET/SDH/ATM Clock Recovery Unit

FEATURES

- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high-frequency PLL with internal loop filter for clock recovery
- Supports clock recovery for OC-12/STM-4 (622.08 Mbps) or OC-3/STM-1 (155.52 Mbps) NRZ data
- 19.44 MHz reference frequency
- Lock detect—monitors frequency
- 264 mW typical power dissipation
- Low-jitter LVPECL interface
- Maintains downstream clock in absence of data inputs
- 3.3 V supply
- Available in a 20-pin TSSOP package
- Active High LVPECL Signal Detect

GENERAL DESCRIPTION

The function of the S3024 clock recovery unit is to derive high-speed timing signals for SONET/SDH-based equipment. The S3024 is implemented using AMCC's proven Phase Lock Loop (PLL) technology.

The S3024 receives either an OC-12/STM-4 or OC-3/STM-1 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential LVPECL bit clock and retimed data. Figure 1 shows a typical network application.

The S3024 utilizes an on-chip PLL, which consists of a phase detector, a loop filter, and a Voltage Controlled Oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO, whose frequency is varied by this voltage. A block diagram is shown in Figure 2.

Figure 1. System Block Diagram

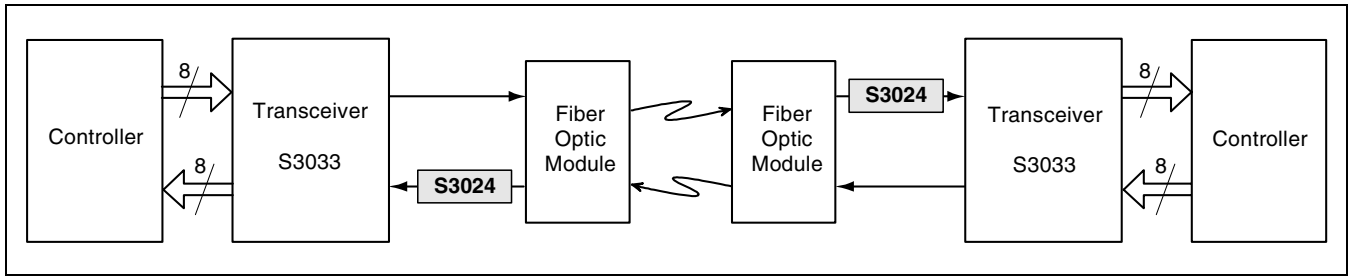
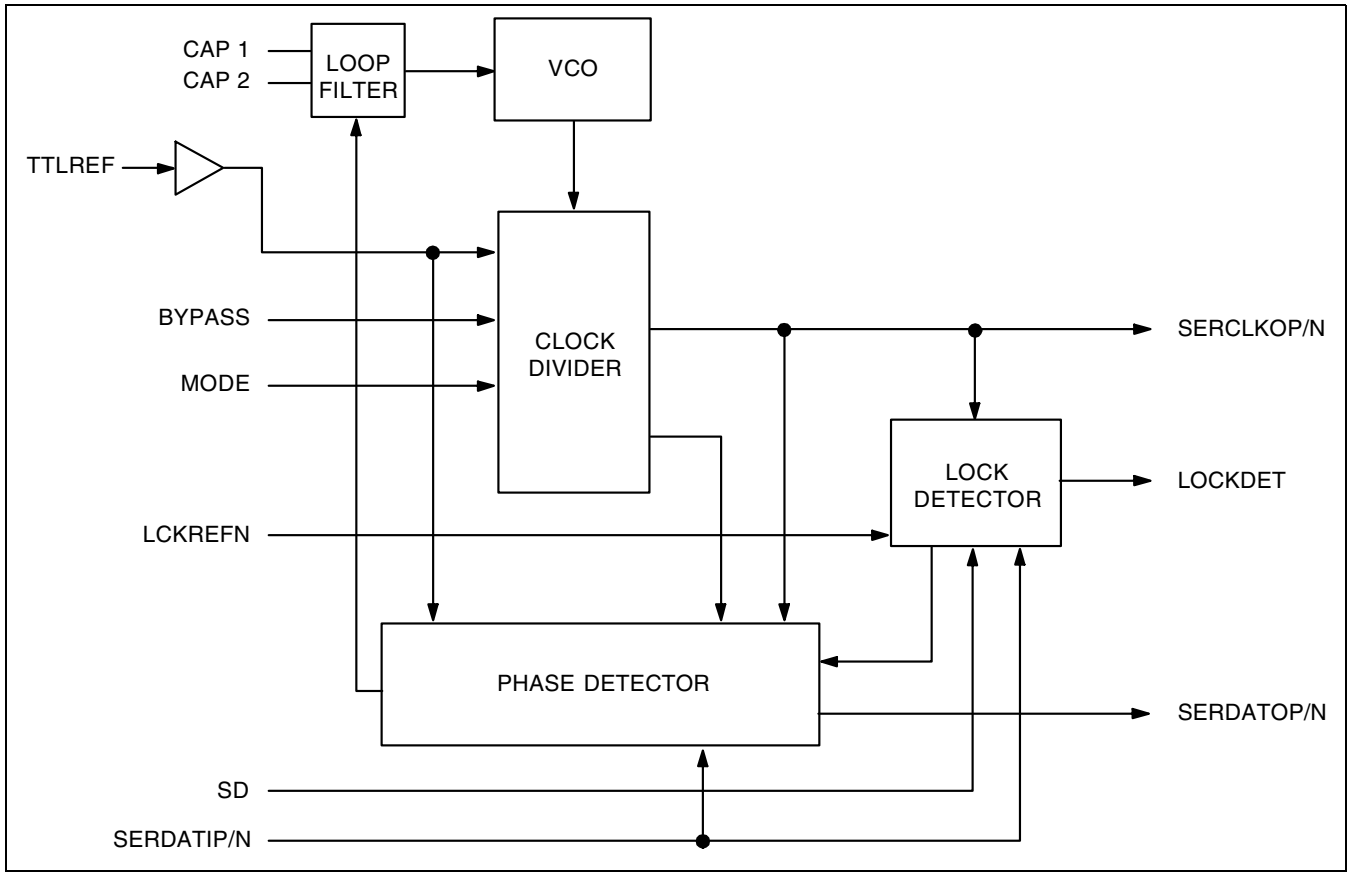


Figure 2. Functional Block Diagram



OVERVIEW

The S3024 supports clock recovery for the OC-12/STM-4 or OC-3/STM-1 data rates. Differential serial data is input to the chip at the specified rate, and clock recovery is performed on the incoming data stream. A reference clock is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3024.

JITTER CHARACTERISTICS

Performance

The S3024 PLL complies with the jitter specifications proposed for SONET/SDH equipment as defined by the T1X1.6/91-022 document when used with differential inputs and outputs as shown in Figure 3.

Jitter Transfer

The jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 5. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 4 be applied for each of the OC-N/STS-N rates.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 4. The measurement condition is the input jitter amplitude, which causes an equivalent of 1 dB power penalty.

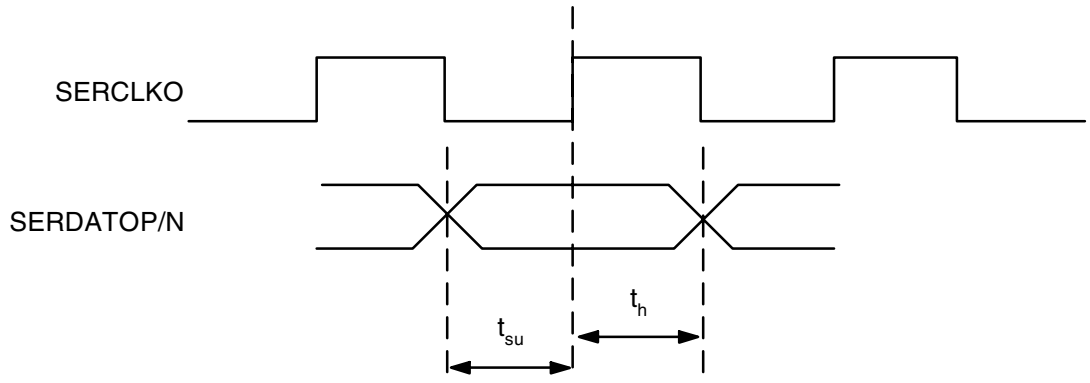
Serial Data Output Set-up and Hold Time

The output set-up and hold times are represented by the waveforms shown in Figure 3.

Jitter Generation

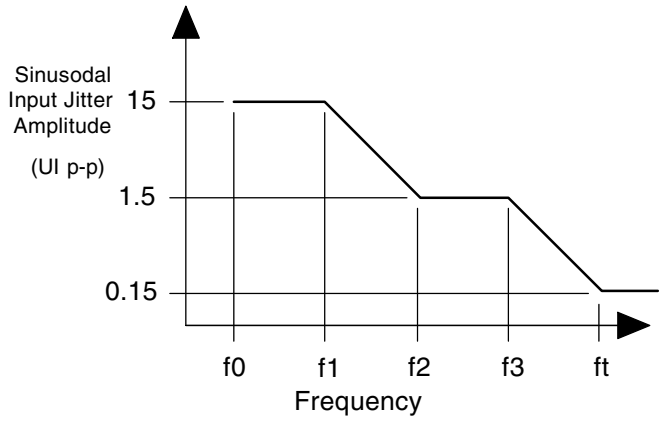
The jitter generation of the serial clock and serial data outputs shall not exceed the value specified in Table 6 when a serial data input with less than 14 ps (OC-12) or 56 ps (OC-3) rms jitter is presented to the serial data inputs.

Figure 3. Clock Output to Data Transition Delay



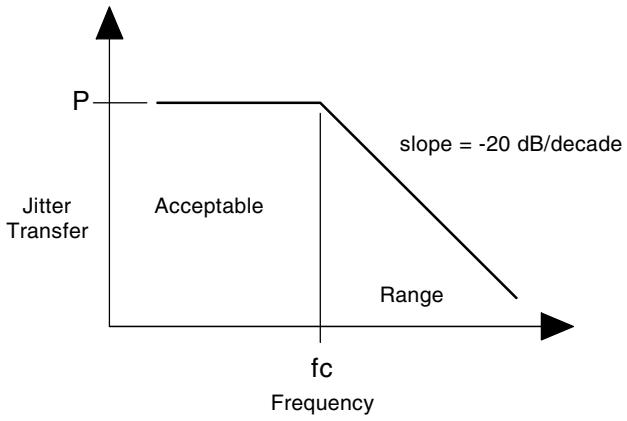
	Output Frequency	
	622.08 MHz	155.52 MHz
SERDATOP/N Setup Time	500 ps	2.5 ns
SERDATOP/N Hold Time	500 ps	2.5 ns

Figure 4. Input Jitter Tolerance Specification



OC/STS Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
12	10	30	300	25	250
3	10	30	300	6.5	65

Figure 5. Jitter Transfer Specification



OC/STS Level	fc (kHz)	P (dB)
12[1,2]	500	0.1
3[1,2]	130	0.1

1. Bellcore Specifications: TR-NWT-000253, Issue 2, December, 1991.
2. CCITT Recommendations: G.958.

Table 1. S3024 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
SERDATIP SERDATIN	Diff. LVPECL	I	2 3	Serial Data In. A clock is recovered from transitions on these inputs.
BYPASS	LVTTL	I	16	Bypass enable, active High. Used during production test to bypass the VCO in the PLL. Tie to ground for normal operation.
SD	LVPECL	I	15	Signal Detect, active High. A single-ended 10 K PECL input to be driven by the external optical receiver module to indicate presence of received optical power. When SD is inactive, the PLL will be forced to lock to the TTLREF input, and the SERDATOP/N output will be held in the logic Low state. When SD is active, data on the SERDATIP/N pins will be processed normally.
TTLREF	LVTTL	I	7	TTL Reference clock input used to establish the initial operating frequency of the clock recovery PLL. It is also used as a standby clock in the absence of data or when LOCKDET is inactive.
CAP1 CAP2	–	I	18 17	External Loop Filter Pins. The loop filter capacitor and resistors are connected to these pins. The capacitor value should be 1.0 µF ±10% tolerance, X7R dielectric. 50 V is recommended. The resistor values are 82 Ω ±5%. See Figure 8.
LCKREFN	LVTTL	I	8	Lock to Reference, active Low. When active, the serial clock output will be forced to lock to the TTLREF local reference input and the SERDATOP/N output will be held at the logic low state. See Table 2.
MODE	LVTTL	I	6	Rate select used to select the bit rate of the device. Set High to select 622.08 Mbps. Set Low to select 155.52 Mbps.
SERDATOP SERDATON	Diff. LVPECL	O	14 13	Serial Data Out signal that is the delayed version of the incoming data stream (SERDATI). Updated on the falling edge of Serial Clock Out (SERCLKOP).
SERCLKOP SERCLKON	Diff. LVPECL	O	12 11	Serial Clock Out signal that is phase aligned with Serial Data Out (SERDATOP/N). (See Figure 3.)
LOCKDET	LVPECL	O	5	Lock Detect, active High. When active, this output indicates that the PLL is locked to the serial data inputs, and valid clock and data are present at the serial outputs. When inactive, it indicates that the PLL is locked to the local reference clock. The lock detect will go inactive under the following conditions: 1. If SD is inactive. 2. If the VCO drifts away from the local reference clock by more than 1000 ppm. 3. If LCKREFN is active. Lock detect will return to the active state if the serial clock is within 250 ppm of the reference clock frequency.
DGND	GND	–	9	Digital Ground (0 V)
DVCC	3.3 V	–	10	Digital Power Supply (+3.3 V)
AGND	GND	–	4, 19	Analog Ground (0 V)
AVCC	3.3 V	–	1, 20	Analog Power Supply (+3.3 V)

Figure 6. S3024 Pinout

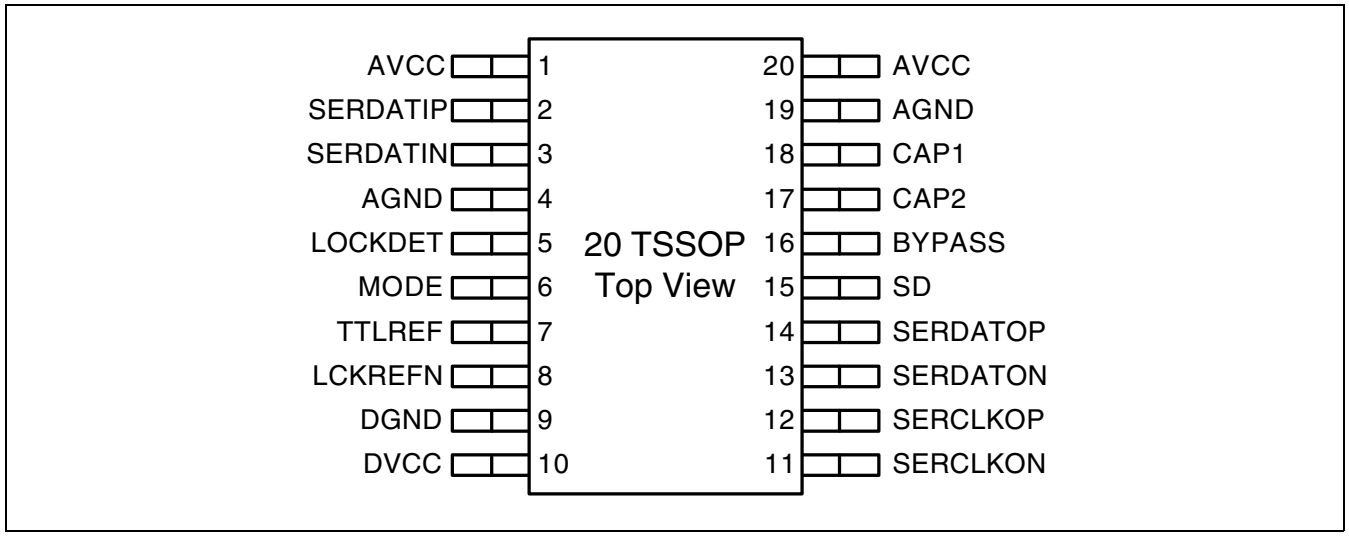
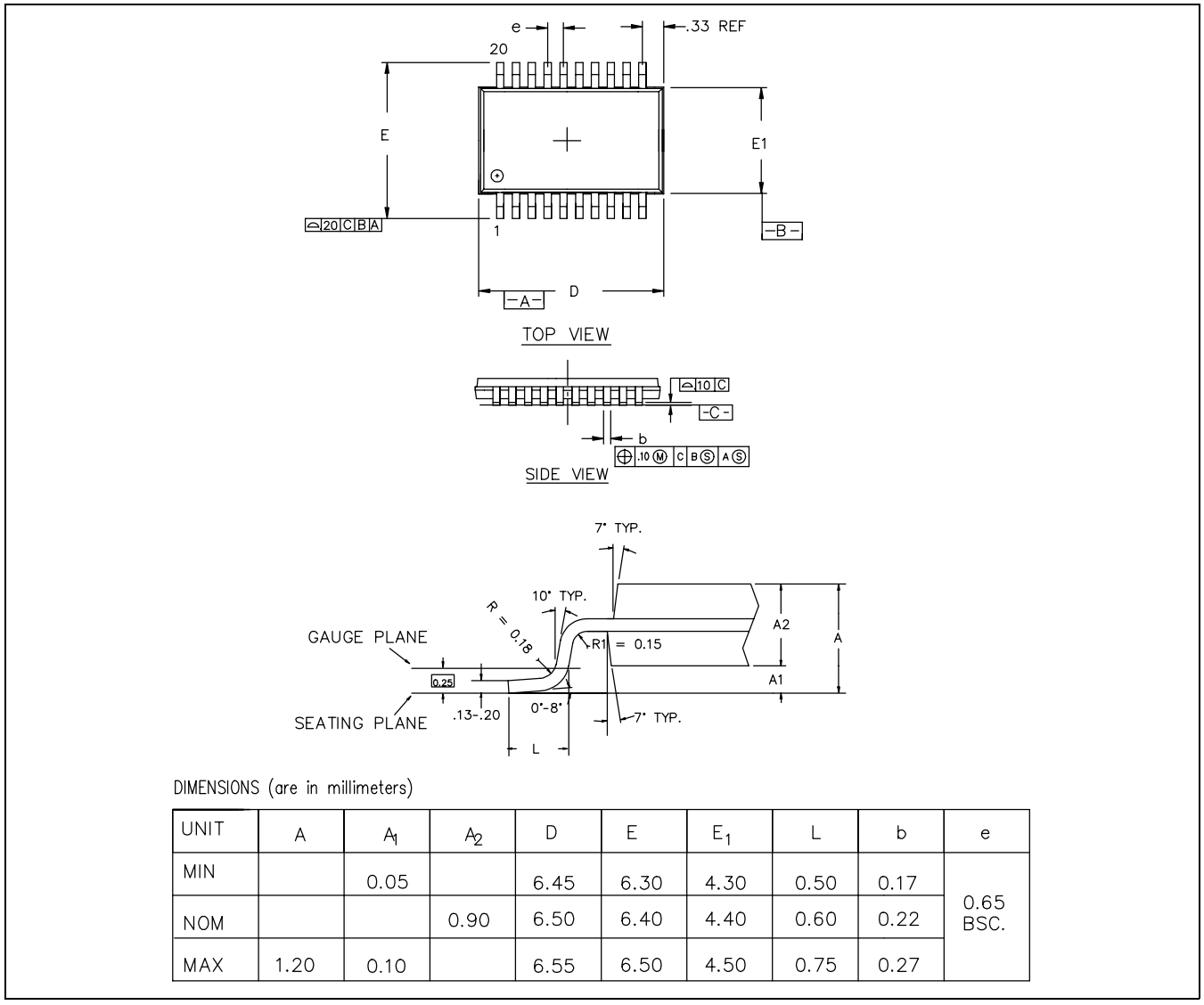


Figure 7. S3024A TSSOP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	E	E_1	L	b	e
MIN		0.05		6.45	6.30	4.30	0.50	0.17	0.65 BSC.
NOM			0.90	6.50	6.40	4.40	0.60	0.22	
MAX	1.20	0.10		6.55	6.50	4.50	0.75	0.27	

Table 2. Clock and Data Output Control

SD	LCKREFN	LOCK DETECT	SERCLKOP/N	SERDATP/N
X	0	0	Active	0
0	X	0	Active	0
1	1	1	Active	Active

Table 3. Thermal Management

Max Power	Θja (Still Air)
347 mW	77°C/W

Table 4. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Storage Temperature	-65		+150	°C
Voltage on V_{CC} with Respect to GND	-0.5		+7.0	V
Voltage on any LVTTL Input Pin	-0.5		V_{CC}	V
Voltage on any LVPECL Input Pin	V_{CC} –2.0		V_{CC}	V
LVTTL Output Sink Current			20	mA
LVTTL Output Source Current			10	mA
High Speed LVPECL Output Source Current			50	mA

ESD Ratings
The S3024 is rated to the following ESD voltages based on the human body model:
1. All pins are rated at or above 1500 V except pin 17, pin 18, and pin 20.

Table 5. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature under Bias (Industrial)	-40		+85	°C
Ambient Temperature under Bias (Commercial)	0		+70	°C
Voltage on V_{CC} with Respect to GND	3.135	3.3	3.465	V
Voltage on any LVTTL Input Pin	0.0		V_{CC}	V
Voltage on any LVPECL Input Pin	V_{CC} –2		V_{CC}	V
PECL Output Source Current (50 Ω to V_{CC} –2 V)		14	25	mA
I_{CC} Supply Current		80	100	mA

Table 6. Performance Specification

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	
Reference Clock Frequency Tolerance Clock Recovery[1]	-250		+250	ppm	
OC-12/STS-12 Capture Range		±500		ppm	With respect to fixed reference frequency.
Clock Output Duty Cycle	45		55	% of UI	Minimum transition density of 20%.
Acquisition Lock Time[1] OC-12/STS-12			16	µsec	With device already powered up and valid REFCLK.
PECL Output Rise and Fall Times			600	ps	10% to 90%, 50 Ω to -2 V equivalent load, 5 pF cap.
SERCLKOP/N Jitter Generation		0.005	0.01	UI	With less than 14 ps (OC-12) rms jitter or 56 ps (OC-3) rms jitter on SERDATIP/N data inputs.
OC-12/STS-12 Jitter Tolerance[1]	0.5			UI	Sinusoidal input jitter. Amplitude on SERDATIP/N data inputs from 12 kHz to 5 MHz.

1. Guaranteed but not tested.

Table 7. LVTTL Input/Output DC Characteristics[1] (T_A = -40°C to +85°C, V_{CC} = 3.3 V ±5%)

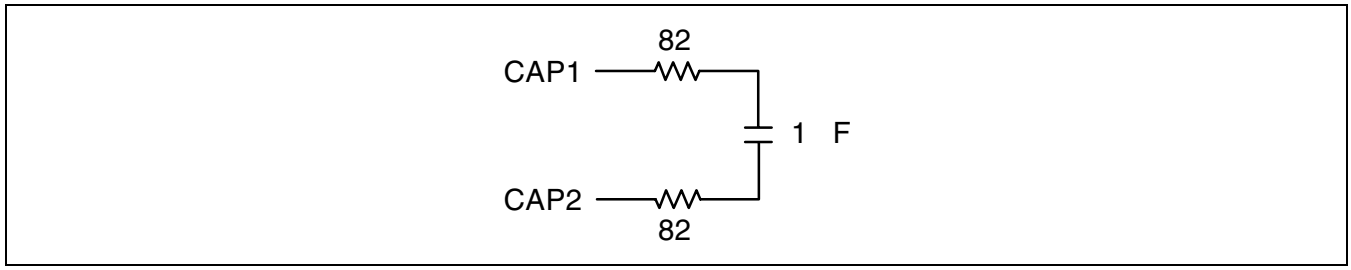
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}[1]	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for all inputs
V_{IH}[1]	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for all inputs
I_{IL}	Input LOW Current	-400			µA	V_{CC} = MAX, V_{IN} = 0.5 V
I_{IH}	Input HIGH Current			50	µA	V_{CC} = MAX, V_{IN} = 2.7 V
I_I	Input HIGH Current at Max V_{IN}			1	mA	V_{CC} = MAX, V_{IN} = V_{CC}
V_{IK}	Input Clamp Diode Voltage	-1.2			V	V_{CC} = MIN, I_{IN} = -18.0 mA

1. These input levels provide a zero-noise immunity and should only be tested in a static, noise-free environment.

Table 8. LVPECL Input/Output DC Characteristics (T_A = -40°C to +85°C, V_{CC} = 3.3 V)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}	Input Low Voltage	V_{CC} –2.000		V_{CC} –1.441	V	Guaranteed Input Low Voltage for single-ended inputs
V_{IH}	Input High Voltage	V_{CC} –1.225		V_{CC} –0.570	V	Guaranteed Input High Voltage for single-ended inputs
V_{IL}	Input Low Voltage	V_{CC} –2.000		V_{CC} –0.700	V	Guaranteed Input Low Voltage for differential inputs
V_{IH}	Input High Voltage	V_{CC} –1.750		V_{CC} –0.450	V	Guaranteed Input High Voltage for differential inputs
V_{ID}	Input Differential Voltage	0.250	0.500	1.400	V	Differential Input Voltage
I_{IH}	Input High Current	-0.500		100	µA	V_{ID} = 500 mV
I_{IL}	Input Low Current	-0.60		20.000	µA	V_{ID} = 500 mV
V_{OL}	Output Low Voltage	V_{CC} –2.000		V_{CC} –1.57	V	50 Ω Termination to V_{CC} –2 V
V_{OH}	Output High Voltage	V_{CC} –1.35		V_{CC} –0.670	V	50 Ω Termination to V_{CC} –2 V
V_{OD}	Output Differential Voltage	0.390		1.330	V	Differential Output Voltage

Figure 8. Loop Filter Connection



Ordering Information

Prefix	Device	Package
S - Integrated Circuit	3024	A – 20 TSSOP

X	XXXX	X
Prefix	Device	Package

Applied Micro Circuits Corporation
6290 Sequence Dr., San Diego, CA 92121
Phone: (858) 450-9333 — (800) 755-2622 — Fax: (858) 450-9885
http://www.amcc.com

D92/R142