DUAL GIGABIT ETHERNET TRANSCEIVER S2068

FEATURES

- Functionally compliant with IEEE 802.3z Gigabit Ethernet Applications
- 1250 MHz (Gigabit Ethernet) operating rate
  – Half rate operation
- Dual Transmitter incorporating phase-locked loop (PLL) clock synthesis from low speed reference
- Dual Receiver PLL provides clock and data recovery
- Internally series terminated TTL outputs
- Low-jitter serial PECL interface
- Local Loopback
- Interfaces with coax, twinax, or fiber optics
- Single +3.3V supply, 1.37W power dissipation
- Compact 21mm x 21mm 156 TBGA package

APPLICATIONS

High-speed data communications

- Ethernet Backbones
- Multi-port Gigabit Ethernet Cards
- Switched networks
- Data broadcast environments

GENERAL DESCRIPTION

The S2068 dual transmitter and receiver chip is designed to provide two channels of high-speed serial data transmission over fiber optic or copper interfaces conforming to the requirements of the IEEE 802.3z Gigabit Ethernet specification. The chip runs at 1250.0 Mbps serial data rate with an associated 10-bit parallel data word. The chip provides two separate receive PLLs which can be operated asynchronously at slightly different frequencies.

Each bi-directional channel provides parallel to serial and serial-to-parallel conversion, clock generation and recovery, and framing. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip dual receive PLL is used for clock recovery and data re-timing on the two independent data inputs. The transmitter and receiver each support differential PECL-compatible I/O for copper or fiber optic component interfaces and provide excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a 3.3V power supply and dissipates 1.37 watts.

Figure 1 shows the use of the S2062 and S2068 in a Gigabit Ethernet application. Figure 2 summarizes the input/output signals of the device. Figures 3 and 4 show the transmit and receive block diagrams, respectively.

Figure 1. Typical Dual Gigabit Ethernet Application

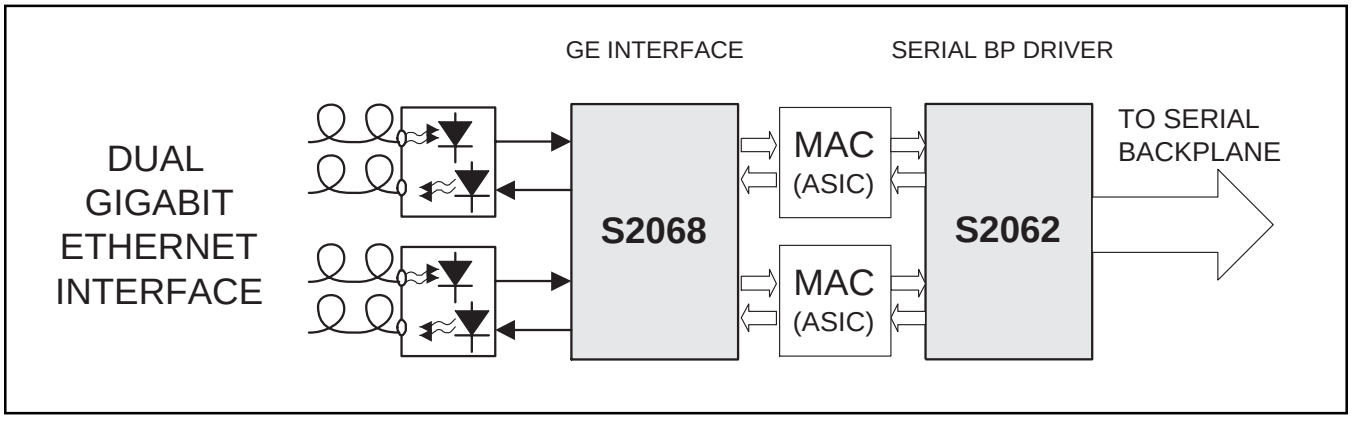


Figure 2. S2068 Input/Output Diagram

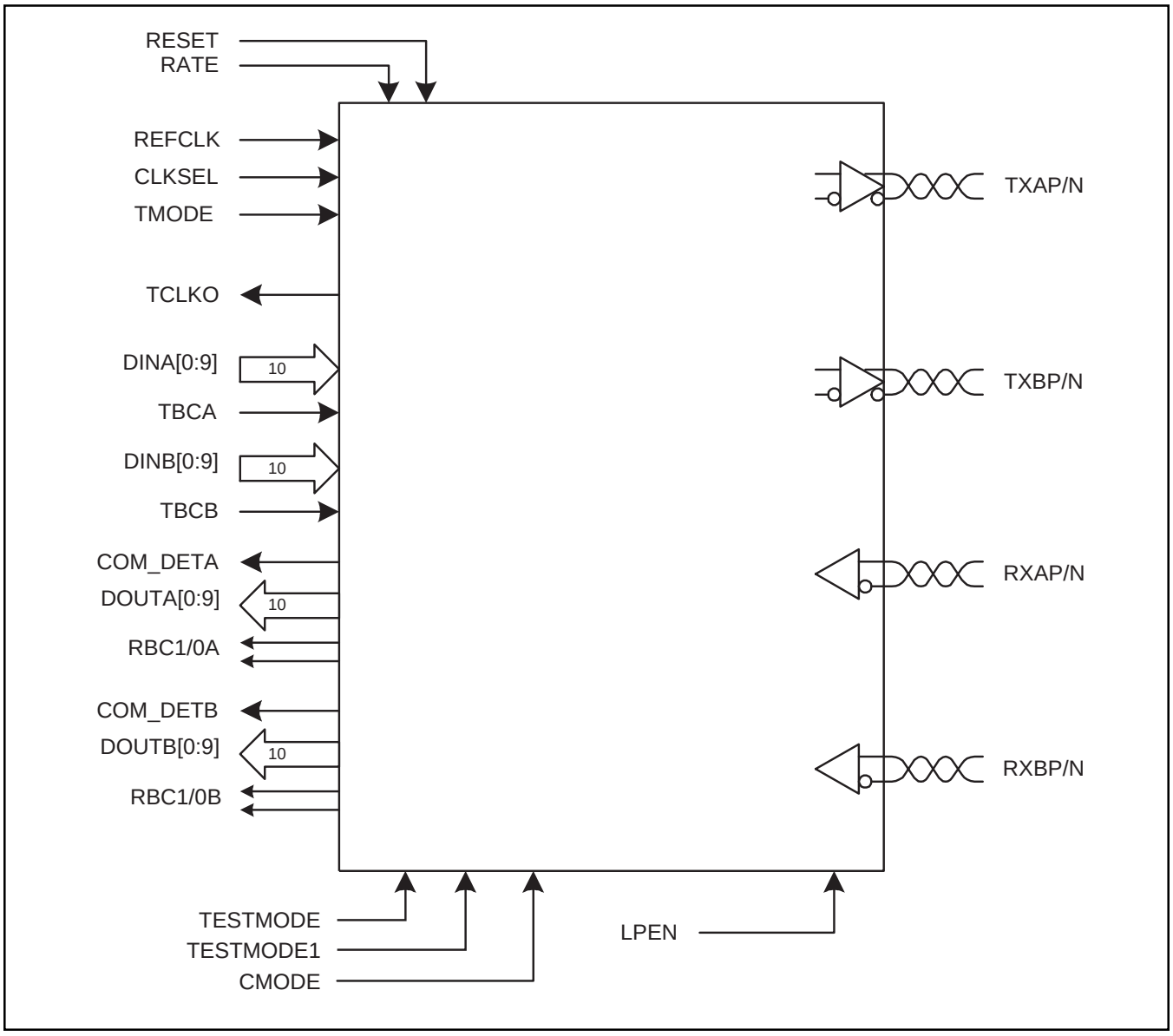


Figure 3. Transmitter Block Diagram

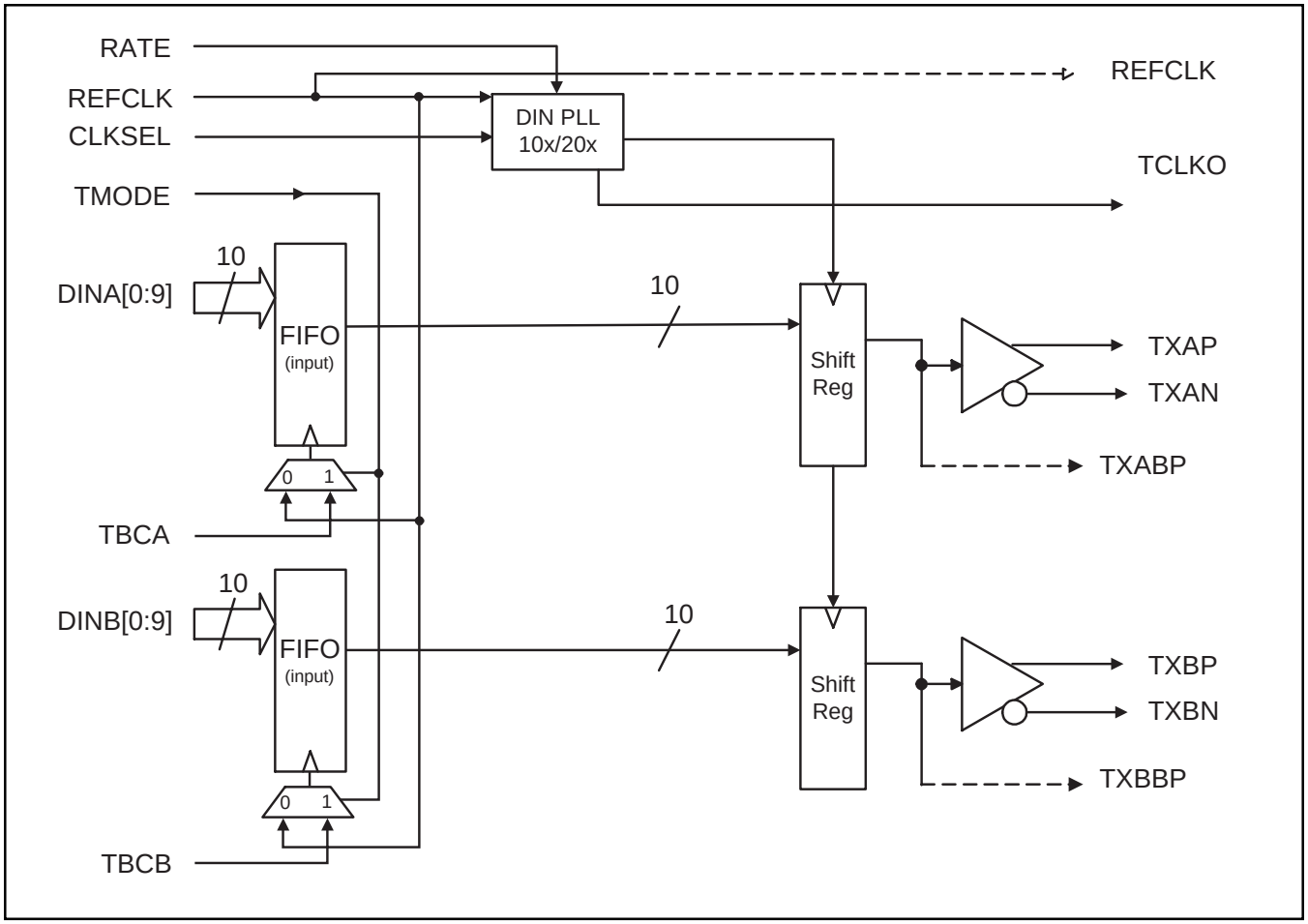
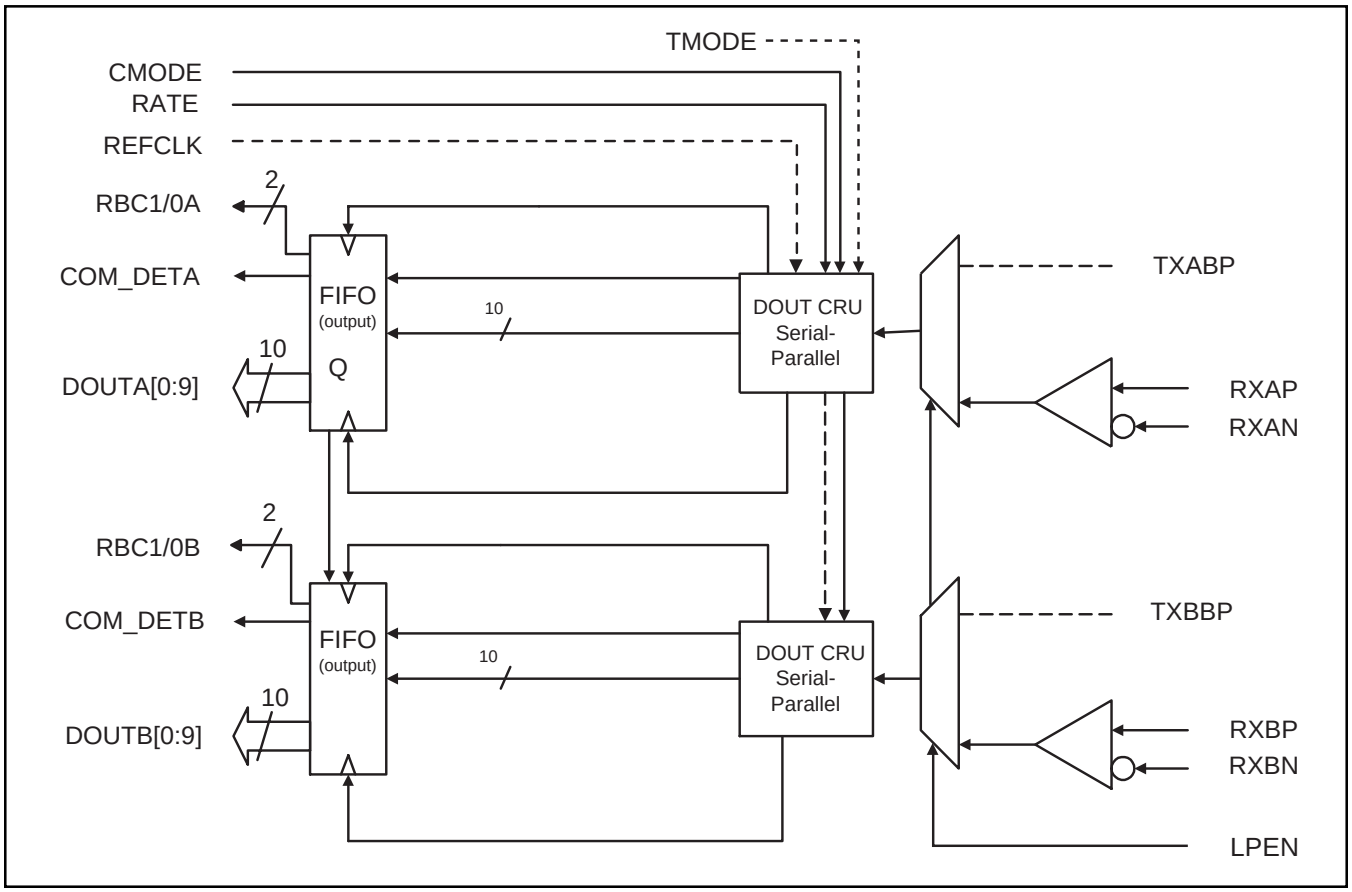


Figure 4. Receiver Block Diagram



TRANSMITTER DESCRIPTION

The transmitter section of the S2068 contains a single PLL which is used to generate the serial rate transmit clock for all transmitters. Transmitter functionalities shown schematically in Figure 3. Two channels are provided with a variety of options regarding input clocking and loopback. The transmitters operate at 1.250 GHz, 10 or 20 times the reference clock frequency.

Data Input

The S2068 has been designed to simplify the parallel interface data transfer and provides flexibility in the clocking of parallel data. Prior implementations of this function have either forced the user to synchronize transmit data to the reference clock or to provide the output clock as a reference to the PLL, resulting in increased jitter at the serial interface. The S2068 incorporates a unique FIFO structure which enables the user to provide a “clean” reference source for the PLL and to accept a separate external clock which is used exclusively to reliably clock data into the device.

Table 1. Operating Rates

RATE	CLKSEL	REFCLK Frequency	Serial Output Rate	TCLK0 Frequency
0	0	SDR/10	1250 Mbps	SDR/10
0	1	SDR/20	1250 Mbps	SDR/10
1	0	SDR/10	625 Mbps	SDR/10
1	1	SDR/20	625 Mbps	SDR/10

Note: SDR = Serial Data Rate.

Table 2. Input Modes

TMODE	Operation
0	REFCLK Mode. REFCLK used to clock data into FIFOs for all channels.
1	TBC Mode. TBCx used to clock data into FIFOs for all channels.

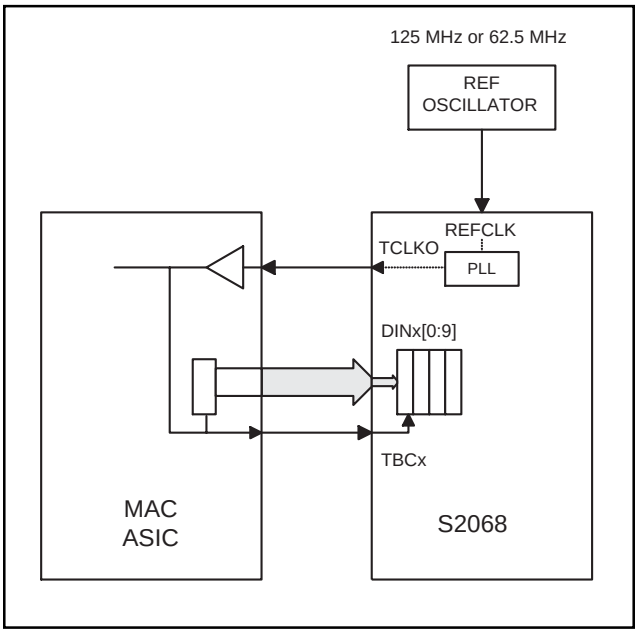
Note that internal synchronization of FIFOs is performed upon de-assertion of RESET.

The S2068 also provides a system clock output, TCLKO, which is derived from the internal VCO. The frequency of this output is constant at the parallel word rate, 1/10 the serial data rate, regardless of whether the reference is provided at 1/10 or 1/20 the serial data rate. This clock can be used by upstream circuitry as a system clock. See Table 1.

Data to be input to the S2068 should be coded to ensure transition density and DC balance. Data is input to each channel of the S2068 as a 10 bit wide word. An input FIFO and a clock input, TBCx, are provided for each channel of the S2068. This device can operate in two different modes. The S2068 can be configured to use either the TBCx (TBC MODE) input or the REFCLK input (REFCLK MODE). Table 2 provides a summary of the input modes for the S2068.

Operation in the TBC MODE makes it easier for users to meet the relatively narrow setup and hold time window required by the 125 Mbit/sec 10 bit interface. The TBC signal is used to clock the data into an internal holding register and the S2068 synchronizes its internal data flow to ensure stable operation. REFCLK, not TBCx, is used as the reference for the transmit PLL. This ensures minimum jitter on the high speed serial data stream.

Figure 5. DIN Clocking with TBC



The TBC must be frequency locked to REFCLK, but may have an arbitrary but fixed phase relationship. Adjustment of internal timing of the S2068 is performed during reset. Once synchronized, the S2068 can tolerate up to ±3ns of phase drift between TBC and REFCLK.

Figure 5 demonstrates the flexibility afforded by the S2068. A low jitter reference is provided directly to the S2068 at either 1/10 or 1/20 the serial data rate. This insures minimum jitter in the synthesized clock used for serial data transmission. A system clock output at the parallel word rate, TCLKO, is derived from the PLL and provided to the upstream circuit as a system clock. This clock can be buffered as required without concern about added delay. There is no phase requirement placed upon TCLKO and the TBCx clock, which is provided back to the S2068, other than that they remain within ± 3ns of the phase relationship established at reset.

The S2068 also supports the traditional REFCLK clocking found in many Gigabit Ethernet applications and is illustrated in Figure 6.

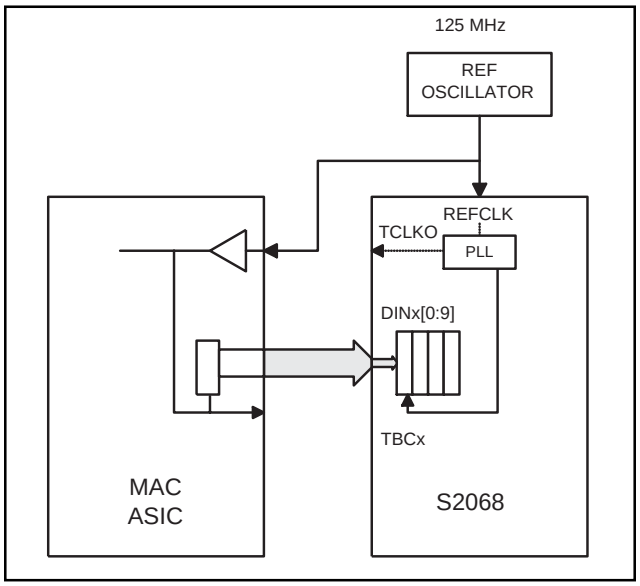
Half Rate Operation

The S2068 supports full and half rate operation for all modes of operation. When RATE is LOW, the S2068 serial data rate equals the VCO frequency. When RATE is HIGH, the VCO is divided by two before being provided to the chip. Thus, the S2068 can support Gigabit Ethernet and serial backplane functions at full and half the VCO rate.

Table 3. Data to 8B/10B Alphabetic Representation

	Data Byte									
DIN[0:9] or DOUT[0:9]	0	1	2	3	4	5	6	7	8	9
8B/10B alph. repr.	a	b	c	d	e	i	f	g	h	j

Figure 6. GE DIN Clocking with REFCLK



Parallel to Serial Conversion

The 10-bit parallel data handled by the S2068 device should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded, 8 bits at a time, into a 10-bit transmission character and must be compliant with IEEE 802.3z Gigabit Ethernet.

The 8B/10B transmission code includes serial encoding and decoding rules, special characters, and error control. Information is encoded, 8 bits at a time, into a 10 bit transmission character. The characters defined by this code ensure that short run lengths and enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple errors that might occur during the transmission and reception of data[1].

Table 3 identifies the mapping of the 8B/10B characters to the data inputs of the S2068. The S2068 will serialize the parallel data for each channel and will transmit bit “a” or DIN[0] first.

Frequency Synthesizer (PLL)

The S2068 synthesizes a serial transmit clock from the reference signal provided. The S2068 will obtain phase and frequency lock within 2500 bit times after the start of receiving reference clock inputs. Reliable locking of the transmit PLL is assured, but a lock-detect output is NOT provided.

Reference Clock Input

The reference clock input must be supplied with a low-jitter clock source. All reference clocks in a system must be within 200 ppm of each other to insure that the clock recovery units can lock to the serial data.

1. A.X. Widner and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC9391, May 1982.

The frequency of the reference clock must be either 1/10 the serial data rate, CLKSEL = 0, or 1/20 the serial data rate, CLKSEL = 1. Note that in both cases, the frequency of the parallel word rate output, TCLKO, is constant at 1/10 the serial data rate.

Serial Data Outputs

The S2068 provides LVPECL level serial outputs. Each high speed output should be provided with a resistor to VSS (Gnd) near the device. A value of 4.5KΩ provides optimal performance with minimum impact on power dissipation. The resistance may be as low as 450 Ω, but will dissipate additional power with no substantive performance improvement.

Transmit FIFO Initialization

The transmit FIFO must be initialized after stable delivery of data and TBC to the parallel interface, and before entering the normal operational state of the circuit. FIFO initialization is performed upon the deassertion of the RESET signal. The TCLKO output will operate normally even when RESET is asserted and is available for use as an upstream clock source.

RECEIVER DESCRIPTION

Each receiver channel is designed to implement the IEEE 802.3z Gigabit Ethernet receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 4.

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. After acquiring bit synchronization, the S2068 searches the serial bit stream for the occurrence of a K28.5 character on which to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the word-aligned data on its parallel outputs.

Data Input

A differential input receiver is provided for each channel of the S2068. Each channel has a loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function for the two channels is controlled by the loopback enable signal, LPEN.

The high speed serial inputs to the S2068 are internally biased to VDD-1.3V. This facilities AC-coupling of the differential inputs and termination with a single differential termination.

Clock Recovery Function

Clock recovery is provided for each channel of the S2068. The receiver PLL has been optimized for the needs of Gigabit Ethernet systems. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the serial data inputs.

The run-length requirements insure that the S2068 will respond appropriately and quickly to a loss of signal. The run-length checker looks for a minimum of 120 consecutive ones or zeros. The checking is done in parallel, thus 12 parallel words are examined.

An off-frequency detection circuit in the S2068 monitors the receiver VCO frequency to insure that the input signal is at a valid data rate. The data stream must be within 200 ppm of the appropriate rate for reliable locking of the CRU to the data stream.

If both the off-frequency test and the run-length test are satisfied, the CRU will attempt to lock to the incoming data. Note that if the run length test is satisfied due to noise on the inputs, and no signal is present, the receiver VCO will maintain frequency accuracy to within 100 ppm of the target rate as determined by the REFCLK.

In any transfer of PLL control from the serial data to the reference clock, the RBC1/0x outputs remain phase continuous and glitch free, assuring the integrity of downstream clocking.

If at any time, the frequency or run length checks are violated, the state machine forces the VCO to lock to the reference clock. This is required to guarantee that the VCO maintains the correct frequency in the absence of data.

Reference Clock Input

The reference clock must be provided from a low jitter clock source. The frequency of the received data stream (divided by 10 or 20) must be within 200 ppm of the reference clock to insure reliable locking of the receiver PLL. A single reference clock is provided to both the transmitter and the receiver of the S2068.

Serial-to-Parallel Conversion

Once bit synchronization has been attained by the S2068 CRU, the S2068 must synchronize to the 10 bit word boundary. Word synchronization in the S2068 is accomplished by detecting and aligning to the 8B/10B K28.5 codeword. The S2068 will detect and byte-align to either polarity of the K28.5. Each channel of the S2068 will detect and align to a K28.5 anywhere in the data stream. The presence of a K28.5 is indicated for each channel by the assertion of the COM_DETx (Comma Detect) signal.

Data Output

Data is output on the DOUTx[0:9] outputs. The COM_DETx signal is used to indicate the reception of a valid K28.5 character and is driven concurrent with the K28.5 character on the DOUTx[0:9] outputs.

The S2068 TTL outputs are optimized to drive 65Ω line impedences. Internal source matching provides good performance on unterminated lines of reasonable length.

Parallel Output Clock Rate

Two output clock modes are supported. When CMODE is HIGH, a complementary TTL clock at the data rate is provided on the RBC1/0x outputs. Data should be clocked on the rising edge of RBC1x. When CMODE is LOW, the S2068 outputs a complementary TTL clock at 1/2 the data rate in compliance with the the Gigabit Ethernet Physical Media Attachment (PMA) specification. Data should be latched on the rising edge of RBC1x and the rising edge of RBC0x.

If consecutive K28.5 characters are received, the S2068 RBC1/0x clock operates without glitches or loss of cycles.

Table 4. Output Clock Modes

Mode	CMODE	RBC1/0x Freq.
Half Clock Mode	0	62.5 MHz
Full Clock Mode	1	125 MHz

Table 5. Transmitter Input Signals Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DINA9 DINA8 DINA7 DINA6 DINA5 DINA4 DINA3 DINA2 DINA1 DINA0	TTL	I	T15 R13 P12 T14 R12 P11 T13 R11 T12 P10	Transmit Data for Channel A. Parallel data on this bus is clocked in on the rising edge of TBCA or REFCLK.
TBCA	TTL	I	R10	Transmit Byte Clock A. When TMODE is High, this signal is used to clock Data on DINA[0:9] into the S2068. When TMODE is Low, TBCA is ignored.
DINB9 DINB8 DINB7 DINB6 DINB5 DINB4 DINB3 DINB2 DINB1 DINB0	TTL	I	L15 L14 M16 M15 M14 N16 N15 N14 P16 P15	Transmit Data for Channel B. Parallel data on this bus is clocked in on the rising edge of TBCB or REFCLK.
TBCB	TTL	I	R16	Transmit Byte Clock B. When TMODE is High, this signal is used to clock Data on DINB[0:9] into the S2068. When TMODE is Low, TBCB is ignored.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 6. Transmitter Output Signals Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
TXAP TXAN	Diff. LVPECL	O	D16 E15	High speed serial outputs for Channel A.
TXBP TXBN	Diff. LVPECL	O	G15 G16	High speed serial outputs for Channel B.
TCLKO	TTL	O	K14	TTL Output Clock at the parallel data rate. This clock is provided for use by up-stream circuitry.

Table 7. Receiver Output Signals Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DOUTA9 DOUTA8 DOUTA7 DOUTA6 DOUTA5 DOUTA4 DOUTA3 DOUTA2 DOUTA1 DOUTA0	TTL	O	J2 G2 L2 L1 K2 K1 J3 J1 H3 H2	Channel A Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1A in full clock mode and valid on the rising edge of both RBC1A and RBC0A in half clock mode.
COM_DETA	TTL	O	G1	Channel A Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTA[0:9].
RBC1A RBC0A	TTL	O	M1 L3	Receive Byte Clocks. Parallel receive data, DOUTA[0:9] and COM_DETA are valid on the rising edge of RBC1A when in full clock mode and valid on the rising edge of both RBC1A and RBC0A in half clock mode.
DOUTB9 DOUTB8 DOUTB7 DOUTB6 DOUTB5 DOUTB4 DOUTB3 DOUTB2 DOUTB1 DOUTB0	TTL	O	P4 R1 P8 T5 R6 P6 R5 T3 P5 R3	Channel B Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1B in full clock mode and valid on the rising edge of both RBC1B and RBC0B in half clock mode.
COM_DETB	TTL	O	P2	Channel B Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTB[0:9].
RBC1B RBC0B	TTL	O	R7 P7	Receive Byte Clocks. Parallel receive data, DOUTB[0:9] and COM_DETB are valid on the rising edge of RBC1B when in full clock mode and valid on the rising edge of both RBC1B and RBC0B in half clock mode.

Table 8. Receiver Input Signals Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RXAP RXAN	Diff. LVPECL	I	B5 A4	Differential LVPECL compatible inputs for channel A. RXAP is the positive input, RXAN is the negative. Internally biased to VDD -1.3V for AC coupled applications.
RXBP RXBN	Diff. LVPECL	I	B10 A11	Differential LVPECL compatible inputs for channel B. RXBP is the positive input, RXBN is the negative. Internally biased to VDD -1.3V for AC coupled applications.

Table 9. Receiver Control Signals Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
LPEN	TTL	I	C14	Loopback Enable. When Low, input source for each channel is the high speed serial output. When High, the serial output for each channel is looped back to its input.
CMODE	TTL	I	C2	Clock Mode Control. When Low, the parallel output clocks (RBC1/0x) rate equals 1/2 the data rate. When High, the parallel output clocks (RBC1/0x) rate is equal to the data rate.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 10. Mode Control Signal Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
TESTMODE	TTL	I	D3	Test Mode Control. Keep Low for normal operation.
TESTMODE1	TTL	I	L16	Test Mode Control. Keep Low for normal operation.
TMODE	TTL	I	A13	Transmit Mode Control. When TMODE is Low, REFCLK is used to clock data on DINx[0:9] into the S2068. When TMODE is High, TBCx is used to clock data into the S2068.
CLKSEL	TTL	I	B11	REFCLK Select Input. This signal configures the PLL for the appropriate REFCLK frequency. When CLKSEL=0, the REFCLK frequency should equal the parallel word rate. When CLKSEL=1, the REFCLK frequency should be 1/2 the parallel data rate.
REFCLK	TTL	I	J15	Reference Clock is used for the transmit VCO and frequency check for the clock recovered from the receiver serial data.
RESET	TTL	I	B15	When Low, the S2068 is held in reset. The receiver PLL is forced to lock to the REFCLK. The FIFOs are initialized on the rising edge of RESET. When High, the S2068 operates normally.
RATE	TTL	I	C11	When Low, the S2068 operates with the serial output rate equal to the VCO frequency. When High, the S2068 operates with the VCO internally divided by 2 for all functions.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 11. Power and Ground Signals Assignment and Descriptions

Pin Name	Qty.	Pin #	Description
VDDA	3	B8 B13 C5	Analog Power (VDD) low noise.
VSSA	3	A8 B4 C13	Analog Ground (VSS).
VDD	3	A10 B12 C6	Power for high speed circuitry (VDD).
VSS VSSSUB	8	A3 A5 A7 A12 A14 C8 C10 C12	Ground for high speed circuitry (VSS).
PECLPWR	2	G14 J16	PECL Power (VDD).
PECLGND	3	C16 D15 F16	PECL Ground (VSS).
DIGPWR	5	B2 C1 D2 K16 N1	Core circuitry Power (VDD).
DIGGND	8	C3 D1 E2 E3 J14 K15 P1 T1	Core circuitry Ground (VSS).
TTLPWR	9	F1 G3 H1 M2 N3 P9 R4 R8 T7	Power for TTL I/O (VDD).
TTLGND	11	E1 F2 F3 K3 M3 N2 P3 T2 T4 T8 T11	Ground for TTL I/O (VSS).
PWR	4	A2 A16 B1 B9	Power.
GND	9	A6 A9 B3 B6 C9 E16 F15 H15 H16	Ground.
CAP1 CAP2	2	A15 B14	Pins for external loop filter capacitor.
NC	20	A1 B7 B16 C4 C7 C15 D14 E14 F14 H14 P13 P14 R2 R9 R14 R15 T6 T9 T10 T16	Not connected. Used as Test Pins. Do Not Connect.

Figure 7. S2068 Pinout (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
1	NC	PWR	DIGPWR	DIGGND	TTLGND	TTLPWR	COM_ DETA	TTLPWR	DOUTA2	DOUTA4	DOUTA6	RBC1A	DIGPWR	DIGGND	DOUTB8	DIGGND
2	PWR	DIGPWR	CMODE	DIGPWR	DIGGND	TTLGND	DOUTA8	DOUTA0	DOUTA9	DOUTA5	DOUTA7	TTLPWR	TTLGND	COM_ DETB	NC	TTLGND
3	VSSSUB	GND	DIGGND	TEST MODE	DIGGND	TTLGND	TTLPWR	DOUTA1	DOUTA3	TTLGND	RBC0A	TTLGND	TTLPWR	TTLGND	DOUTB0	DOUTB2
4	RXAN	VSSA	NC											DOUTB9	TTLPWR	TTLGND
5	VSS	RXAP	VDDA											DOUTB1	DOUTB3	DOUTB6
6	GND	GND	VDD											DOUTB4	DOUTB5	NC
7	VSSSUB	NC	NC											RBC0B	RBC1B	TTLPWR
8	VSSA	VDDA	VSSSUB											DOUTB7	TTLPWR	TTLGND
9	GND	PWR	GND											TTLPWR	NC	NC
10	VDD	RXBP	VSS											DINA0	TBCA	NC
11	RXBN	CLKSEL	RATE											DINA4	DINA2	TTLGND
12	VSSSUB	VDD	VSSSUB											DINA7	DINA5	DINA1
13	TMODE	VDDA	VSSA											NC	DINA8	DINA3
14	VSS	CAP2	LPEN	NC	NC	NC	PECL PWR	NC	DIGGND	TCLKO	DINB8	DINB5	DINB2	NC	NC	DINA6
15	CAP1	RESET	NC	PECL GND	TXAN	GND	TXBP	GND	REFCLK	DIGGND	DINB9	DINB6	DINB3	DINB0	NC	DINA9
16	PWR	NC	PECLGND	TXAP	GND	PECL GND	TXBN	GND	PECL PWR	DIGPWR	TEST MODE1	DINB7	DINB4	DINB1	TBCB	NC

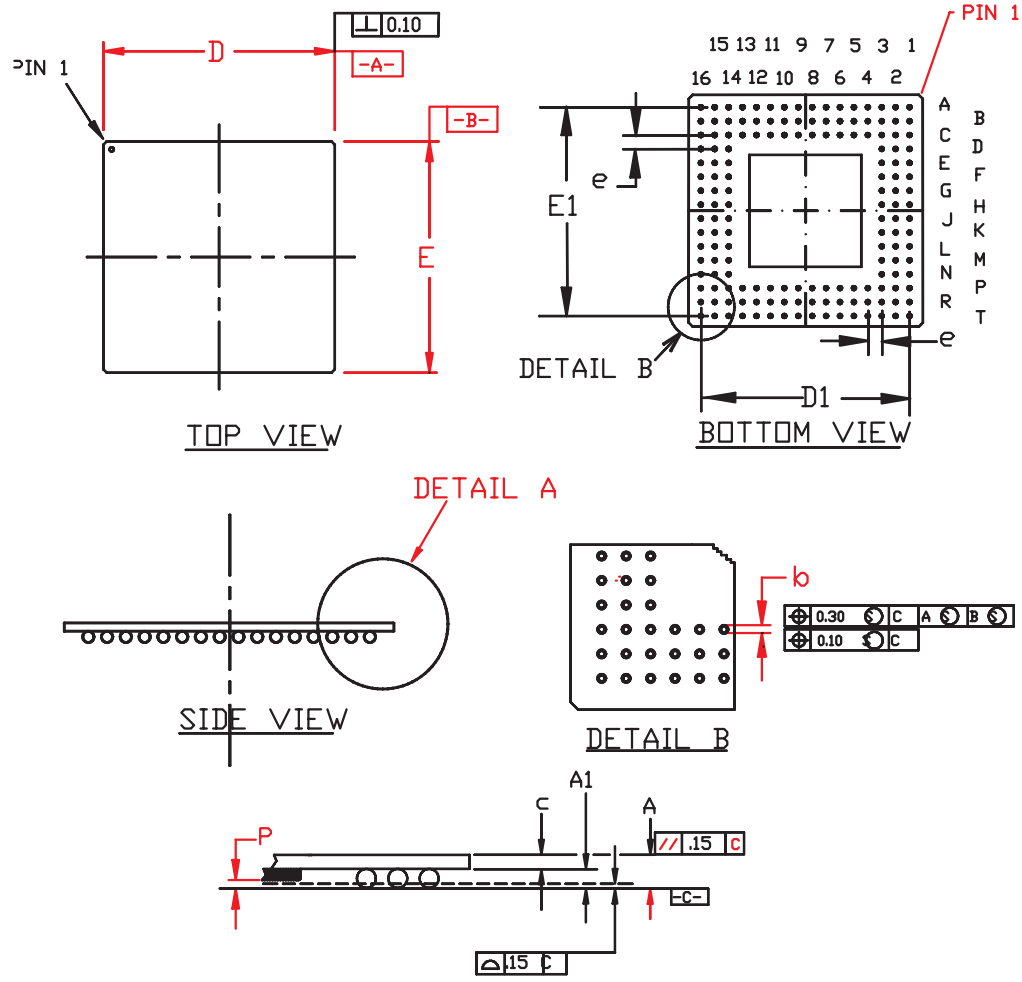
Note: NC used as Test Pins. Do Not Connect.

Figure 8. S2068 Pinout (Top View)

T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
DIGGND	DOUTB8	DIGGND	DIGPWR	RBC1A	DOUTA6	DOUTA4	DOUTA2	TTLPWR	COM_ DETA	TTLPWR	TTLGND	DIGGND	DIGPWR	PWR	NC	1
TTLGND	NC	COM_ DETB	TTLGND	TTLPWR	DOUTA7	DOUTA5	DOUTA9	DOUTA0	DOUTA8	TTLGND	DIGGND	DIGPWR	CMODE	DIGPWR	PWR	2
DOUTB2	DOUTB0	TTLGND	TTLPWR	TTLGND	RBC0A	TTLGND	DOUTA3	DOUTA1	TTLPWR	TTLGND	DIGGND	TEST MODE	DIGGND	GND	VSSSUB	3
TTLGND	TTLPWR	DOUTB9											NC	VSSA	RXAN	4
DOUTB6	DOUTB3	DOUTB1											VDDA	RXAP	VSS	5
NC	DOUTB5	DOUTB4											VDD	GND	GND	6
TTLPWR	RBC1B	RBC0B											NC	NC	VSSSUB	7
TTLGND	TTLPWR	DOUTB7											VSSSUB	VDDA	VSSA	8
NC	NC	TTLPWR											GND	PWR	GND	9
NC	TBCA	DINA0											VSS	RXBP	VDD	10
TTLGND	DINA2	DINA4											RATE	CLKSEL	RXBN	11
DINA1	DINA5	DINA7											VSSSUB	VDD	VSSSUB	12
DINA3	DINA8	NC											VSSA	VDDA	TMODE	13
DINA6	NC	NC	DINB2	DINB5	DINB8	TCLKO	DIGGND	NC	PECL PWR	NC	NC	NC	LPEN	CAP2	VSS	14
DINA9	NC	DINB0	DINB3	DINB6	DINB9	DIGGND	REFCLK	GND	TXBP	GND	TXAN	PECL GND	NC	RESET	CAP1	15
NC	TBCB	DINB1	DINB4	DINB7	TEST MODE1	DIGPWR	PECL PWR	GND	TXBN	PECL GND	GND	TXAP	PECLGND	NC	PWR	16

Note: NC used as Test Pins. Do Not Connect.

Figure 9. 156 TBGA Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	D	D_1	E	E_1	P	b	c	e
MIN	1.45	0.60	20.80	19.05 BSC.	20.80	19.05 BSC.		0.65	0.85	1.27 BSC.
NOM	1.55	0.65	21.00		21.00			0.75	0.90	
MAX	1.65	0.70	21.20		21.20		0.25	0.85	0.95	

Thermal Management

Device	Θja	Θjc
S2068	19.8˚C/W	3.5˚C/W

Figure 10. Transmitter Timing (REFCLK Mode, TMODE = 0)

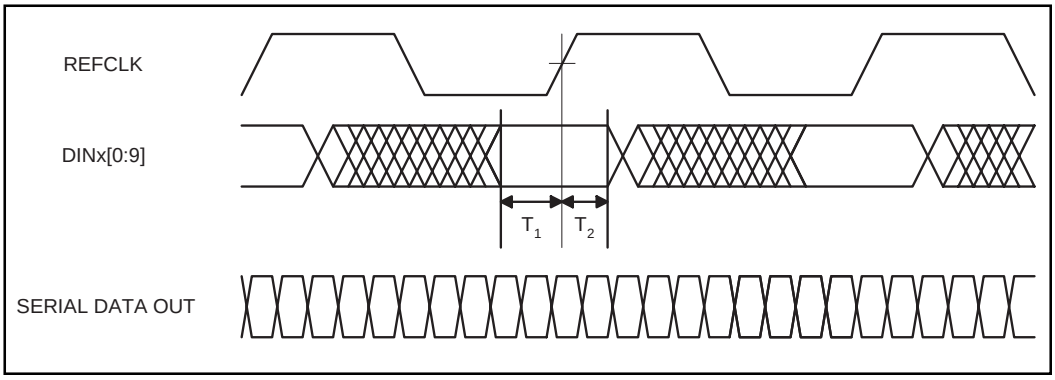


Table 12. S2068 Transmitter Timing (REFCLK Mode, TMODE = 0)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ REFCLK	0.5		ns	See Note 1.
T_2	Data Hold w.r.t. ↑ REFCLK	1.3		ns	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 11. Transmitter Timing (TBC Mode, TMODE = 1)

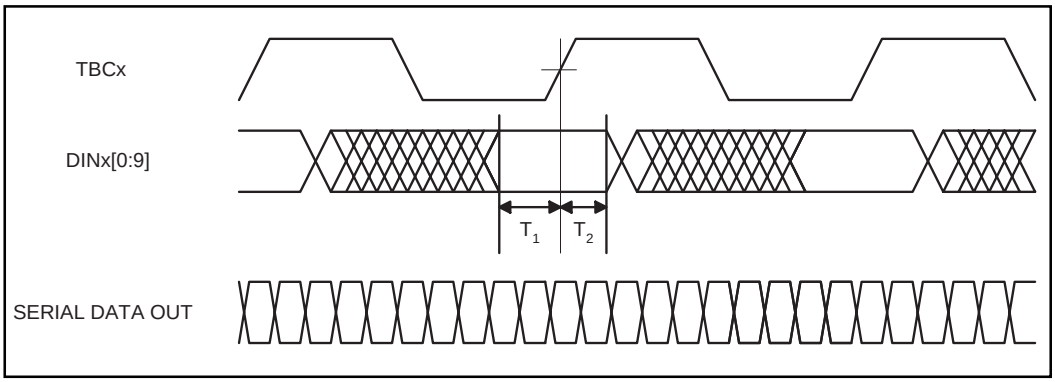


Table 13. S2068 Transmitter Timing (TBC Mode, TMODE = 1)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↓ TBC	1.0		ns	See Note 1.
T_2	Data Hold w.r.t. ↑ TBC	0.5		ns	
	Phase drift between TBCx and REFCLK	–3	+3	ns	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Table 14. Transmitter Timing

Parameters	Description	Min	Max	Units	Conditions
T_{SDR}, T_{SDF}	Serial Data Rise and Fall		300	ps	20% - 80%, tested on sample basis. 4.5 kΩ to ground.
T_J	Serial Data Output total jitter (p-p)		192	ps	Peak-to-peak, measured on sample basis. Measured with ±K28.5 or 2^7-1 pattern at 1.25 GHz.
T_{DJ}	Serial Data Output deterministic jitter (p-p)		80	ps	Peak-to-peak, tested on a sample basis. Measured with ±K28.5 pattern at 1.25 GHz.

Figure 12. TCLKO Timing

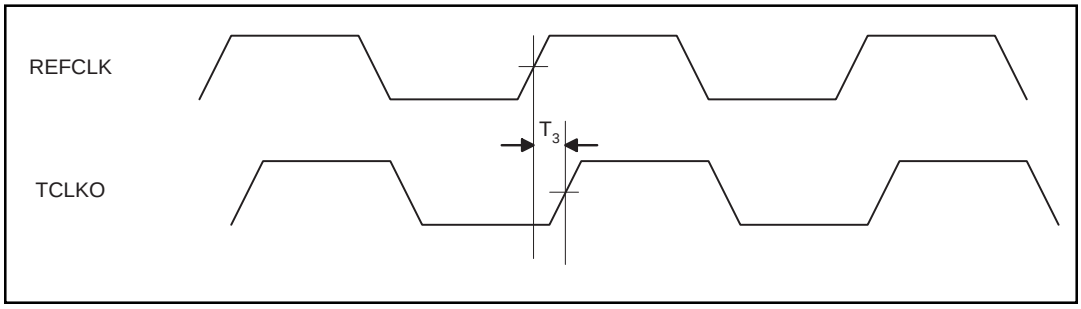


Table 15. S2068 Transmitter (TCLKO Timing)

Parameters	Description	Min	Max	Units	Conditions
T_3	↑TCLKO w.r.t.↑REFCLK	2	7.5	ns	
TCLKO Duty Cycle		40%	60%	%	

Note: Measurements are made at 1.4V level of clocks.

Figure 13. Receiver Timing (Full Clock Mode, CMODE = 1)

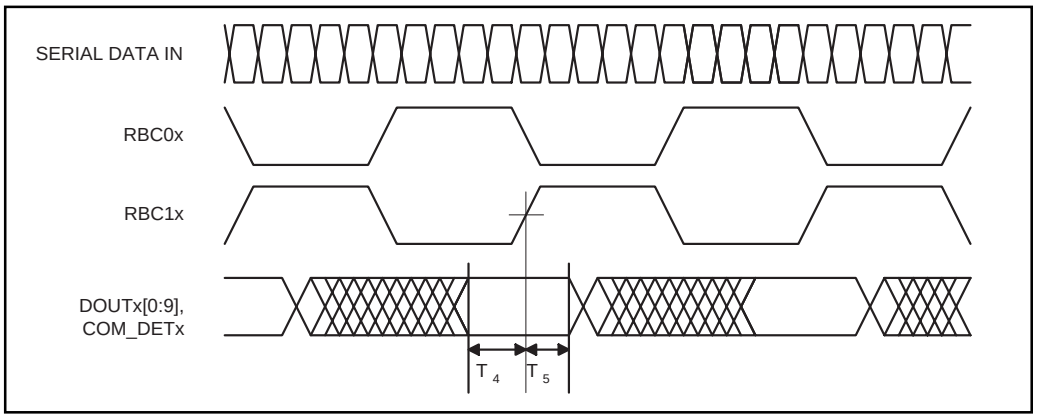


Table 16. S2068 Receiver Timing (Full Clock Mode, CMODE = 1)

Parameters	Description	Min	Max	Units	Conditions
T_4	Data Setup w.r.t. ↑ RBC1x	2.75		ns	See Note 1.
T_5	Data Hold w.r.t. ↑ RBC1x	2.0		ns	
RBC1/0x Duty Cycle		40	60	%	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 14. Receiver Timing (Half Clock Mode, CMODE = 0)

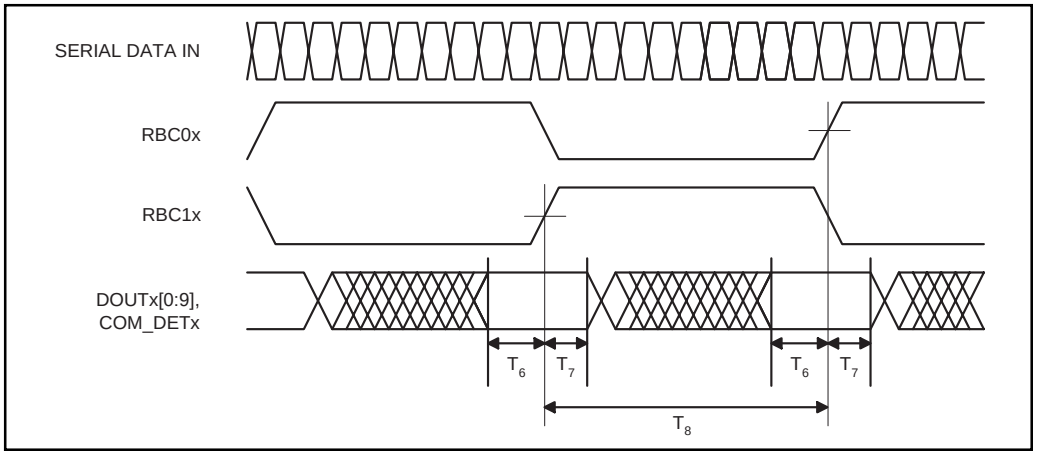


Table 17. S2068 Receiver Timing (Half Clock Mode, CMODE = 0)

Parameters	Description	Min	Max	Units	Conditions
T_6	Data Setup w.r.t. ↑ RBC1/0x	2.5		ns	See Note 1.
T_7	Data Hold w.r.t. ↑ RBC1/0x	2.0		ns	
T_8	Time from RBC1x Rise to RBC0x Rise	7.8	8.82	ns	
RBC1/0x Duty Cycle		40	60	%	

1. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Table 18. S2068 Receiver Timing

Parameters	Description	Min	Max	Units	Conditions
T_{RCR}, T_{RCF}	RBC1, RBC0 Rise and Fall Time		3.0	ns	Measured +.8V to +2.0V. See Figure 17.
T_{DR}, T_{DF}	Data Output Rise and Fall Time		3.0	ns	Measured +.8V to +2.0V. See Figure 16.
T_{LOCK} (Frequency)	Frequency Acquisition Lock Time (Loss of Lock) (1.25 Gbps)		175	µs	After power up.
T_J	Total Input Jitter Tolerance	599		ps	As specified in IEEE 802.3z.
T_{DJ}	Deterministic Input Jitter Tolerance	370		ps	As specified in IEEE 802.3z.

OTHER OPERATING MODES

Loopback Mode

When loopback mode is enabled, the serial data from the transmitter is provided to the serial input of the receiver. Loopback mode can be simultaneously enabled for both channels using the loopback-enable input, LPEN.

The loopback mode provides the ability to perform system diagnostics and off-line testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium.

Note that the high speed outputs are disabled during loopback operation.

Test Modes

The RESET pin is used to initialize the transmit FIFOs and must be asserted (LOW) prior to entering the normal operational state (see section Transmit FIFO Initialization).

Operating Frequency Rate

The S2068 is designed to operate at the Gigabit Ethernet rate of 1.250 GHz.

Figure 15. S2068 Diagnostic Loopback Operation

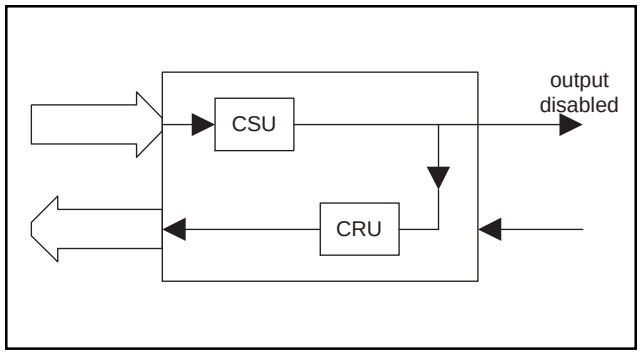


Table 19. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	–55		125	˚C
Junction Temperature Under Bias	–55		150	˚C
Storage Temperature	–65		150	˚C
Voltage on VDD with Respect to GND	–0.5		+7.0	V
Voltage on any TTL Input Pin	–0.5		3.47	V
Voltage on any PECL Input Pin	0		VDD	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			30	mA
Static Discharge Voltage, TTL I/O		2000		V
Static Discharge Voltage, PECL I/O		1500		V

Table 20. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on any Power Pin with respect to GND/VSS	3.13	3.3	3.47	V
Voltage on any TTL Input Pin	0		3.47	V
Voltage on any PECL Input Pin	VDD -2V		VDD	V

Table 21. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	–100	+100	ppm	
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% – 80%.
—	Jitter		80	ps	Peak-to-Peak, 77% data eye.

Table 22. DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL)	2.4	2.8	VDD	V	VDD = min I_{OH} = –4mA
V_{OL}	Output Low Voltage (TTL)	GND	.025	0.5	V	VDD = min I_{OL} = 4mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4V, VDD = Max
I_{IL}	Input Low Current (TTL)			600	µA	V_{IN} = 0.8V, VDD = Max
IDD	Supply Current		415	533	mA	1010 Pattern.
P_D	Power Dissipation		1.37	1.84	W	1010 Pattern.
V_{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		2200	mV	See Figure 19.
ΔV_{OUT}	Differential Serial Output Voltage Swing	1500	1900	2200	mV	AC coupled with 4.5 kΩ pulldown and 100 Ω differential termination. See Figure 18.
C_{IN}	Input Capacitance			3	pf	

OUTPUT LOAD

The S2068 serial outputs require a resistive load to set the output current. The recommended resistor value is 4.5 kΩ to ground. This value can be varied to adjust drive current, signal voltage swing, and power usage on the board.

ACQUISITION TIME

With the input eye diagram shown in Figure 21, the S2068 will recover data with a ≤1E-9 BER within the time specified by T_{LOCK} in Table 18 after an instantaneous phase shift of the incoming data.

Figure 19. High Speed Differential Inputs

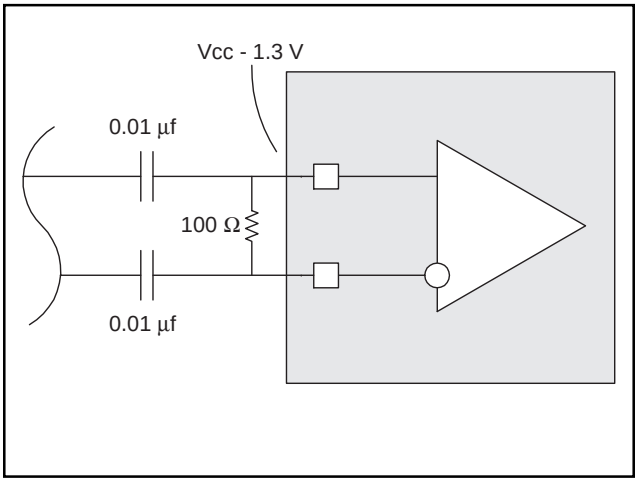


Figure 16. Serial Input/Output Rise and Fall Time

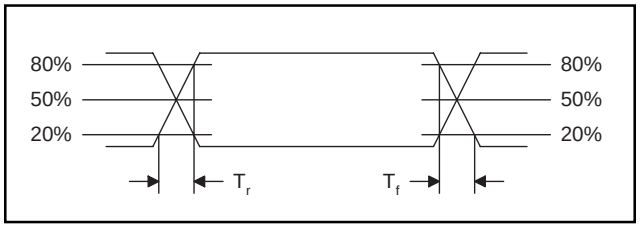


Figure 17. TTL Input/Output Rise and Fall Time

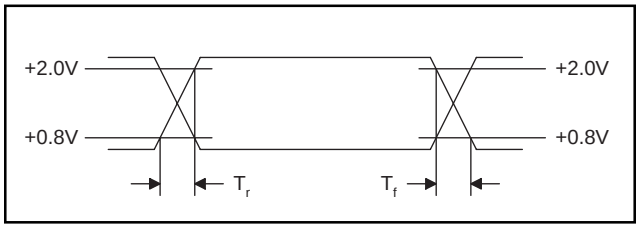


Figure 18. Serial Output Load

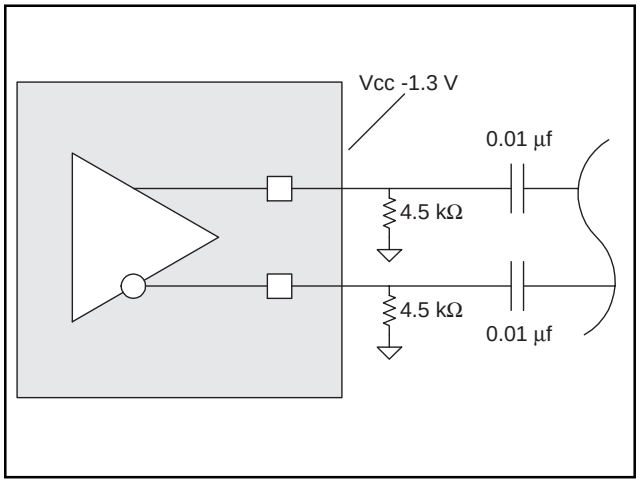


Figure 20. Receiver Input Eye Diagram Jitter Mask

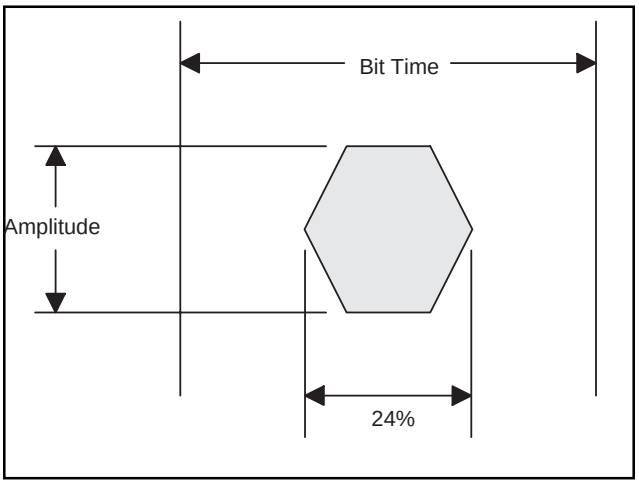


Figure 21. Acquisition Time Eye Diagram

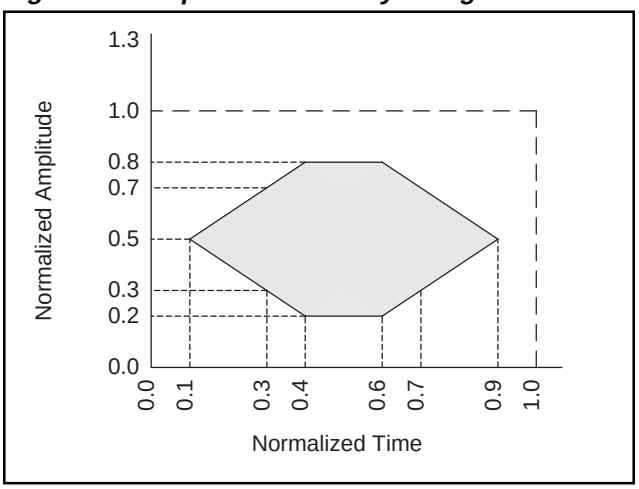
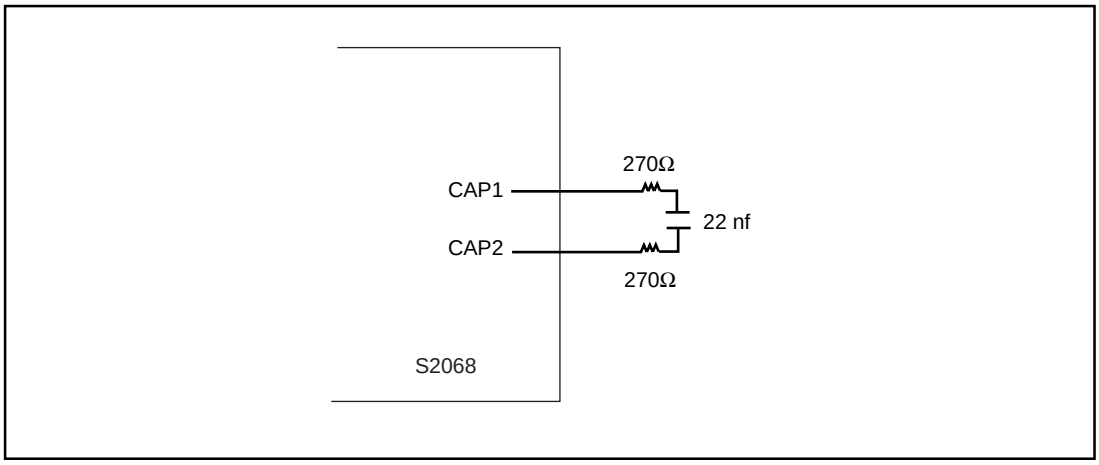
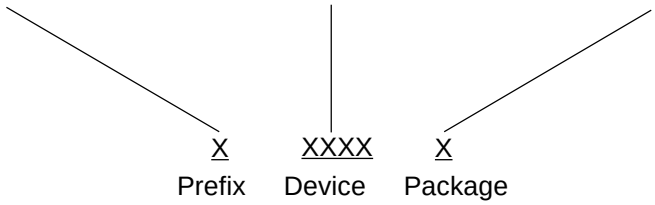


Figure 22. Loop Filter Capacitor Connections



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	2068	TB – 156 TBGA



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