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DESCRIPTION

The SLV series of transient voltage suppressors are designed to protect low voltage, state-of-the-art CMOS semiconductors from transients caused by electrostatic discharge (ESD), lightning and other induced voltage surges.

The devices are constructed using Semtech's proprietary EPD process technology. The EPD process provides low standoff voltages with significant reductions in leakage currents and capacitance over silicon avalanche diode processes. The SLVU2.8 features an integrated low capacitance compensation diode that allows the device to be configured to protect one unidirectional line or, when paired with a second SLVU2.8, two high-speed line pairs.

The SLV series is specifically designed to protect low voltage components such as Ethernet transceivers, microprocessors, ASICs, video, and high speed RAM. The low clamping voltage of the SLVU2.8 minimizes the stress on the protected IC. In high-speed applications, the low capacitance and low leakage current are critical for preserving signal integrity.

The SLV series TVS diodes will meet the surge requirements of IEC 1000-4-2, Level 4, "Human Body Model" for air and contact discharge.

ORDERING INFORMATION

Part Number	Qty per Reel	Reel Size
SLVU2.8.TC	3,000	7”
SLVU2.8.TG	10,000	13”

FEATURES

- 400 watts peak pulse power (tp = 8/20µs)
- Transient protection for data lines to
  IEC 1000-4-2 (ESD) 15kV (air), 8kV (contact)
  IEC 1000-4-4 (EFT) 40A (tp = 5/50ns)
  IEC 1000-4-5 (Lightning) 12A (tp = 1.2/50µs)
- One device protects one unidirectional line
- Two devices provide low capacitance protection for high-speed interfaces
- Low operating voltage (2.8V) ideal for latch-up protection
- Low capacitance
- Low clamping voltage
- Solid-state EPD process technology

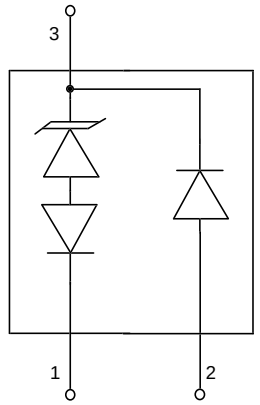
MECHANICAL CHARACTERISTICS

- JEDEC SOT-23 package
- Molding compound flammability rating: UL 94V-0
- Marking : U2.8
- Packaging : Tape and Reel per EIA 481

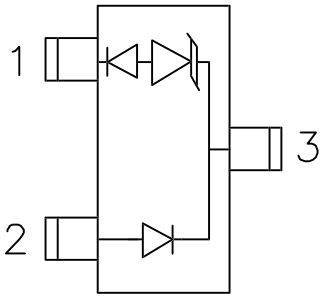
APPLICATIONS

- 10/100 Ethernet
- WAN/LAN Equipment
- Low Voltage ASICs
- Notebook, Laptop, Palmtop Computers
- Desktop PC & Servers
- Video

CIRCUIT DIAGRAM



SCHEMATIC & PIN CONFIGURATION



SOT-23 (Top View)

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20µs)	P_{pk}	400	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	24	A
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS, T_A = 25°C (Unless Otherwise Specified)

SLVU2.8						
Parameter	**Symbol**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Reverse Stand-Off Voltage	V_{RWM}	Pin 3 to 1 or Pin 2 to 1			2.8	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2µA Pin 3 to 1	3.0			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA Pin 3 to 1	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 2.8V, T=25°C Pin 3 to 1 or Pin 2 to 1			1	µA
Clamping Voltage	V_C	I_{PP} = 2A, tp = 8/20µs Pin 3 to 1			3.9	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs Pin 3 to 1			7	V
Clamping Voltage	V_C	I_{PP} = 24A, tp = 8/20µs Pin 3 to 1			12.5	V
Clamping Voltage	V_C	I_{PP} = 2A, tp = 8/20µs Pin 2 to 1			5.5	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs Pin 2 to 1			8.5	V
Clamping Voltage	V_C	I_{PP} = 24A, tp = 8/20µs Pin 2 to 1			15	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz Pin 3 to 1 & 2 (1 & 2 are tied together)		70	100	pF
Junction Capacitance	C_j	V_R = 0V, f = 1MHz Pin 2 to 1 (Pin 3 N.C.)		5	10	pF
Steering Diode Characteristics						
Reverse Breakdown Voltage	V_{BR}	I_t = 10µA Pin 3 to 2	40			V
Reverse Leakage Current	I_{RD}	V_{RWM} = 2.8V, T=25°C Pin 3 to 2			1	µA
Forward Voltage	V_F	I_F = 1A, tp = 120µs Pin 2 to 3			2	V

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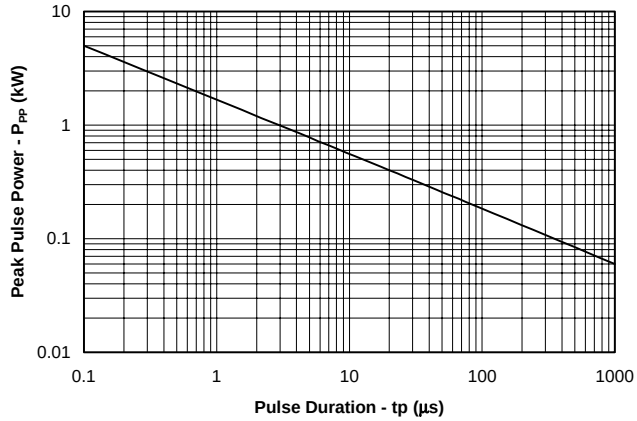
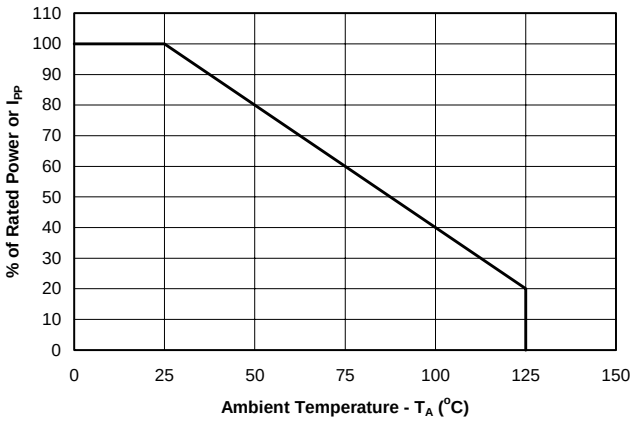
TYPICAL CHARACTERISTICS

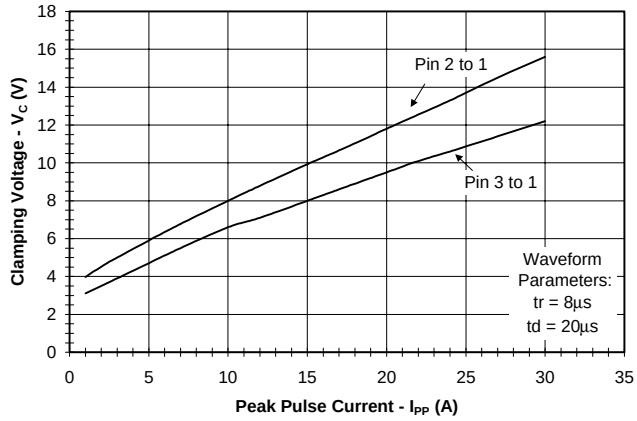
Non-Repetitive Peak Pulse Power vs. Pulse Time



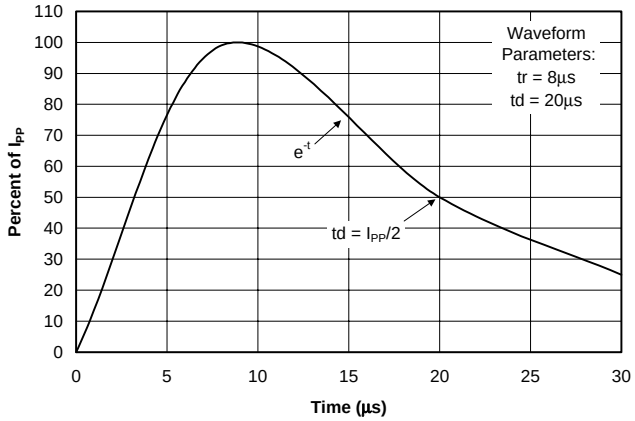
Pulse Derating Curve



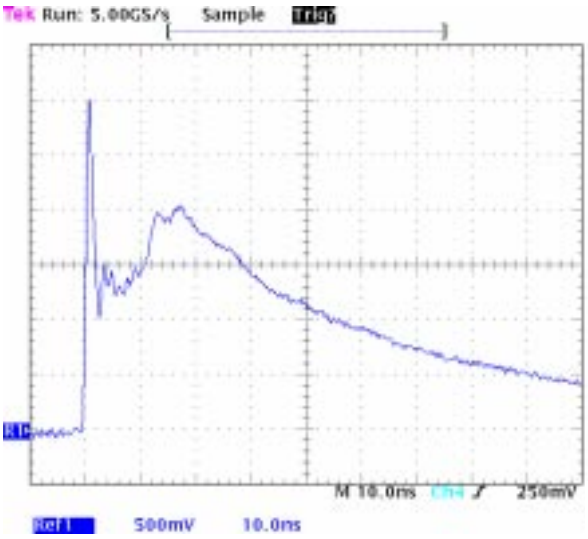
Clamping Voltage vs. Peak Pulse Current



Pulse Waveform



ESD Pulse Waveform (Per IEC 1000-4-2)



IEC 1000-4-2 Discharge Parameters

Level	First Peak Current (A)	Peak Current at 30ns (A)	Peak Current at 60ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

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APPLICATIONS INFORMATION

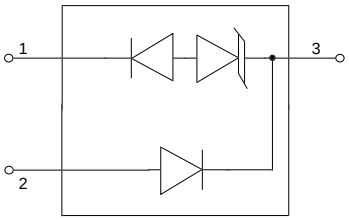
Device Connection Options

Electronic equipment is susceptible to transient disturbances from a variety of sources including: ESD to an open connector or interface, direct or nearby lightning strikes to cables and wires, and charged cables "hot plugged" into I/O ports. The SLVU2.8 is designed to protect sensitive components from damage and latch-up which may result from such transient events. The SLVU2.8 can be configured to protect either one unidirectional line or two (one line pair) high-speed data lines. The options for connecting the devices are as follows:

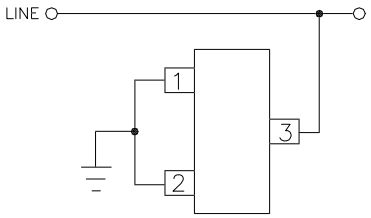
1. **Protection of one unidirectional I/O line:** Protection of one data line is achieved by connecting pin 3 to the protected line, and pins 1 and 2 to ground. This connection option will allow the device to operate on lines with positive polarity signal transitions (during normal operation). In this configuration, the device adds a maximum loading capacitance of 100pF. During positive duration transients, the internal TVS diode will be reversed biased and will act in the avalanche mode, conducting the transient current from pin 3 to 1. The transient will be clamped at or below the rated clamping voltage of the device. For negative duration transients, the internal steering diode is forward biased, conducting the transient current from pin 2 to 3. The transient is clamped below the rated forward voltage drop of the diode. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

2. **Low capacitance protection of one differential line pair:** Protection of a high-speed differential line pair is achieved by connecting two devices in anti-parallel. Pin 1 of the first device is connected to line 1 and pin 2 is connected to line 2. Pin 2 of the second device is connected to line 1 and pin 1 is connected to line 2 as shown. Pin 3 must be left open on both devices. During negative duration transients, the first device will conduct from pin 2 to 1. The steering diode conducts in the forward direction while the TVS will avalanche and conduct in the reverse direction. During positive transients, the second device will conduct in the same manner. In this configuration, the total loading capacitance is the sum of the capacitance (between pins 1 and 2) of each device (typically <10pF) making this configuration suitable for high-speed interfaces such as 10/100 Ethernet (See application note SI98-02).

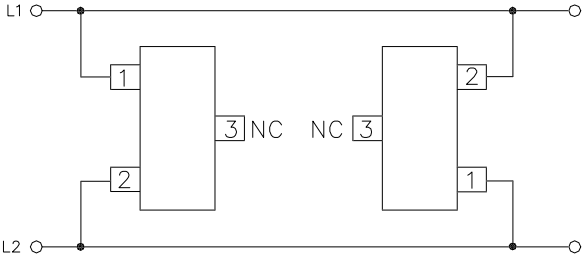
SLVU2.8 Circuit Diagram



Protection of One Unidirectional I/O Line



Low Capacitance Protection of One Differential Line Pair



Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of fast rise-time transients such as ESD. The following guidelines are recommended:

- Place the SLVU2.8 near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the SLVU2.8 and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

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APPLICATIONS INFORMATION (CON'T)

EPD TVS Characteristics

The SLVU2.8 is constructed using Semtech's proprietary EPD technology. The structure of the EPD TVS is vastly different from the traditional pn-junction devices. At voltages below 5V, high leakage current and junction capacitance render conventional avalanche technology impractical for most applications. However, by utilizing the EPD technology, the SLVU2.8 can effectively operate at 2.8V while maintaining excellent electrical characteristics.

The EPD TVS employs a complex nppn structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. The EPD mechanism is achieved by engineering the center region of the device such that the reverse biased junction does not avalanche, but will "punch-through" to a conducting state. This structure results in a device with superior dc electrical parameters at low voltages while maintaining the capability to absorb high transient currents.

The IV characteristic curve of the EPD device is shown in Figure 1. The device represents a high impedance to the circuit up to the working voltage (V_{RWM}). During a transient event, the device will begin to conduct as it is biased in the reverse direction. When the punch-through voltage (V_{PT}) is exceeded, the device enters a low impedance state, diverting the transient current away from the protected circuit. When the device is conducting current, it will exhibit a slight "snap-back" or negative resistance characteristic due to its structure. This must be considered when connecting the device to a power supply rail. To return to a non-conducting state, the current through the device must fall below the snap-back current (approximately < 50mA).

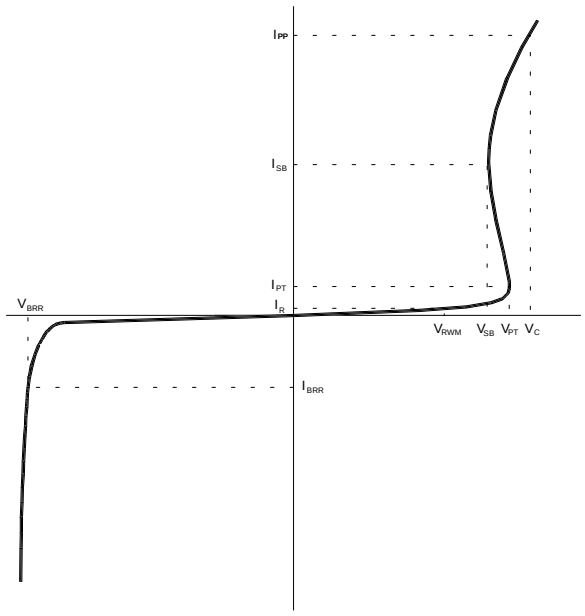

Figure 1 - EPD TVS IV Characteristic Curve

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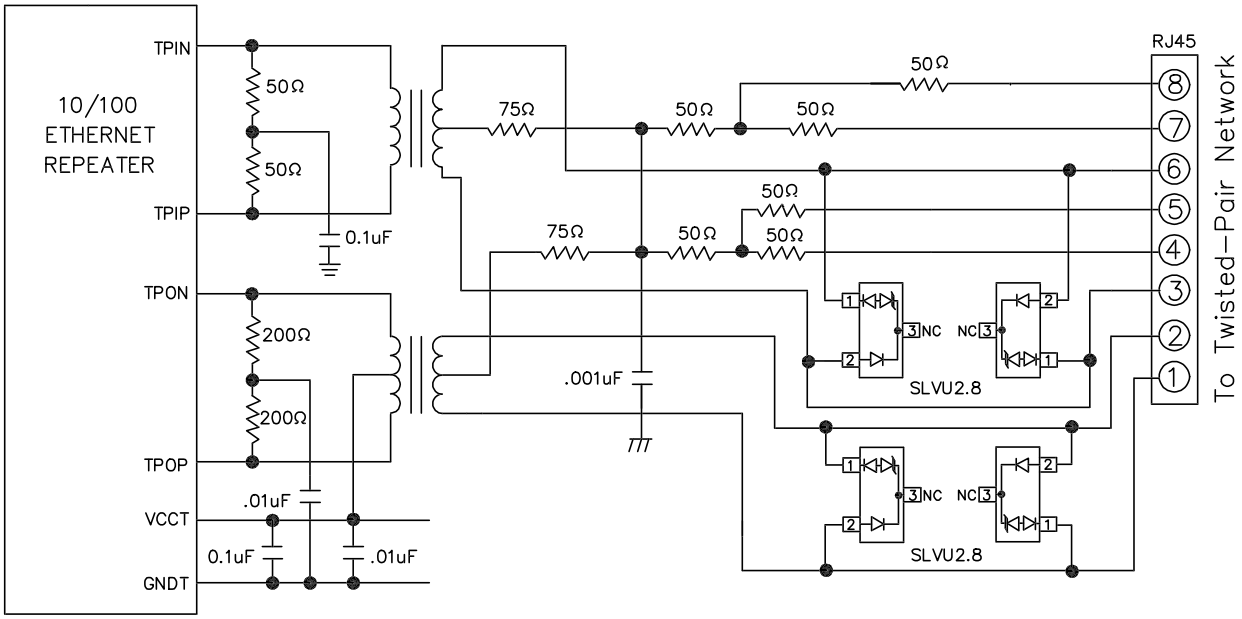
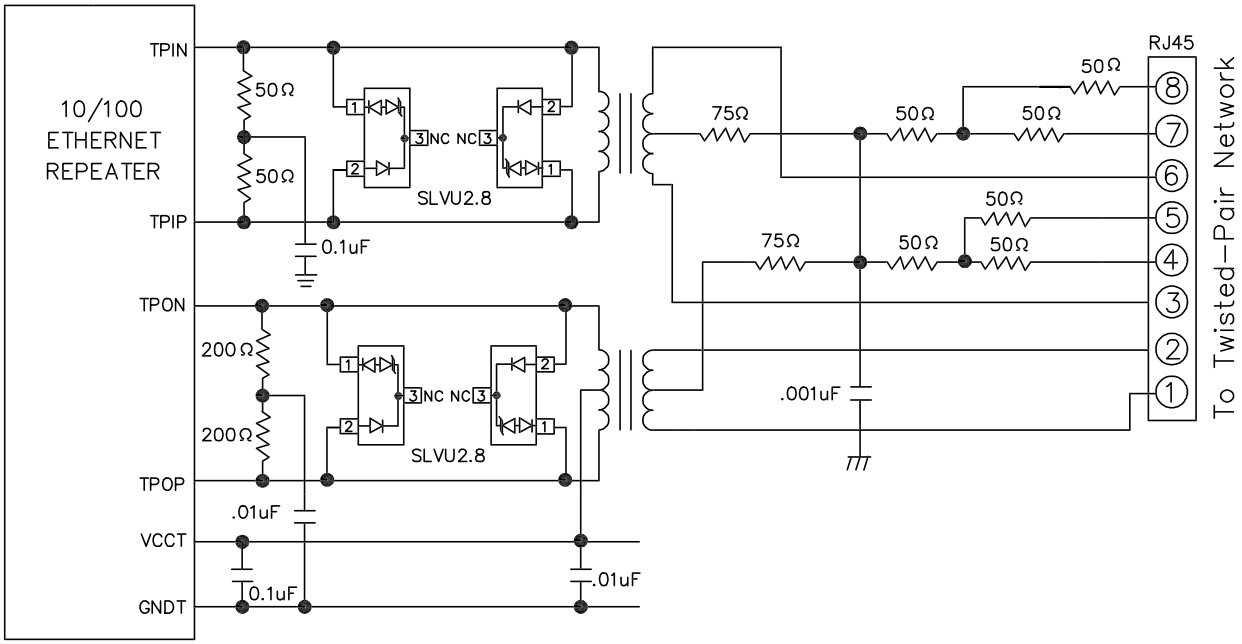
TYPICAL APPLICATIONS



10/100 Ethernet ESD Protection Circuit
(Reference Semtech Application Note SI98-02 for Additional Information)



10/100 Ethernet Lightning Protection to Bellcore GR-1089 (Intra-Building)
(Reference Semtech Application Note SI98-02 for Additional Information)

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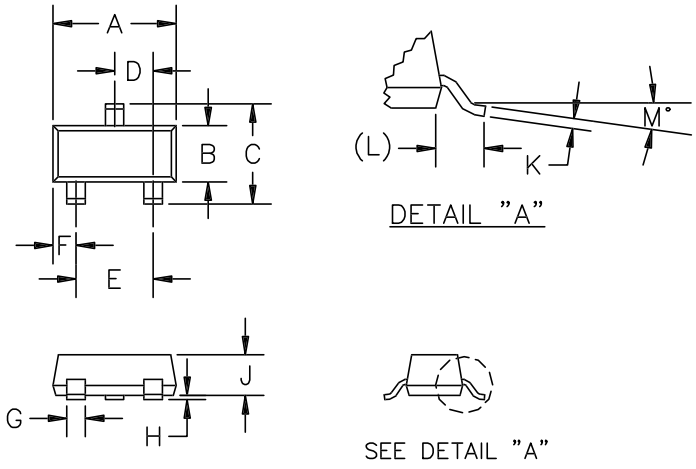
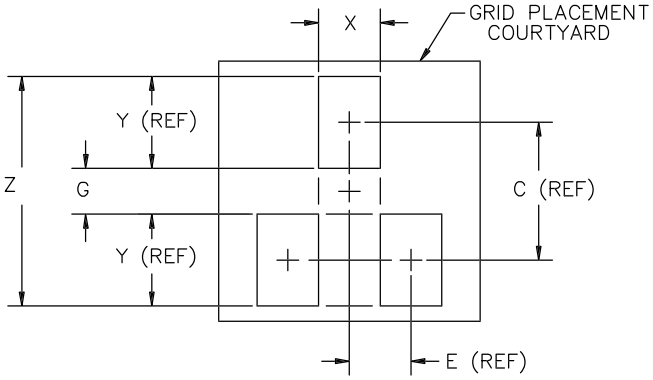
OUTLINE DRAWING SOT-23



DIMENSIONS [1]					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.110	.119	2.8	3.04	–
B	.047	.055	1.20	1.40	–
C	.083	.104	2.10	2.64	–
D	.035	.040	0.88	1.02	–
E	.070	.081	1.78	2.05	–
F	.017	.024	.44	.60	–
G	.014	.020	.37	.51	–
H	.0005	.004	.013	0.10	–
J	.034	.040	.87	1.02	–
K	.003	.007	.085	.180	–
L	–	.022	–	0.55	REF
M	0	8°	0	8°	–

LAND PATTERN SOT-23



DIMENSIONS					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.09	–	2.20	–
E	–	.04	–	.95	–
G	.03	.04	.80	1.00	–
X	.03	.04	.80	1.00	–
Y	–	.06	–	1.40	–
Z	.14	.15	3.40	3.60	–

Note 1 : Grid placement courtyard is 8 x 8 elements (4mm x 4mm) in accordance with the international grid detailed in IEC Publication 97.