



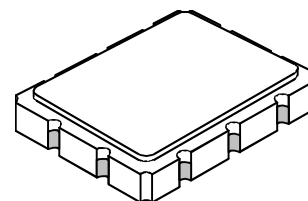
- **Designed for Interactive Video Applications**
- **Wide Bandwidth and Excellent GD Variation**
- **9.1 x 7.1 mm Surface-mount Case**
- **Single Ended Input and Output**

Absolute Maximum Ratings

Rating	Value	Units
Maximum Incident Power in Passband	+10	dBm
Max. DC voltage between any 2 terminals	30	VDC
Storage Temperature Range	-40 to +85	°C
Max. Soldering Profile	265°C for 10 s	

SF1126A

127 MHz SAW Filter



SM9171-10

Electrical Characteristics

Characteristic	Sym	Notes	Min	Typ	Max	Units
Nominal Center Frequency	f_c	1	127.000			MHz
Passband Insertion Loss at f_c 1.3 db Passband Group Delay Variation over $f_c \pm 12.0$ MHz Phase Linearity over $f_c \pm 12.0$ MHz	IL	1, 2		14	15.0	dB
	$BW_{1.3}$		± 15.0			MHz
	GDV			11	30	nS _{p-p}
					10	° _{p-p}
Rejection < 107.0 MHz > 147.25 MHz Ultimate		1, 2, 3	40			dB
			40			
				40		
Operating Temperature Range	T_A	1	+25		+30	°C
Frequency Temperature Coefficient	FTC			-94		ppm/°C

Impedance Matching to 50Ω Unbalanced	External L-C
Case Style	SM9171-10 9.1 x 7.1 mm Nominal Footprint
Lid Symbolization (YY = year, WW = week)	RFM SF1126A YYWW

Notes:

1. Unless noted otherwise, all specifications apply over the operating temperature range with filter soldered to the specified demonstration board with impedance matching to 50 Ω and measured with 50 Ω network analyzer.
2. Unless noted otherwise, all frequency specifications are referenced to the nominal center frequency, f_c .
3. Rejection is measured as attenuation below the minimum IL point in the passband. Rejection in final user application is dependent on PCB layout and external impedance matching design. See Application Note No. 42 for details.
4. Part to part absolute delay measurement records the absolute delay mean across 1 dB passband.
5. "LRIP" or "L" after the part number indicates "low rate initial production" and "ENG" or "E" indicates "engineering prototypes."
6. The design, manufacturing process, and specifications of this filter are subject to change.
7. Either Port 1 or Port 2 may be used for either input or output in the design. However, impedances and impedance matching may vary between Port 1 and Port 2, so that the filter must always be installed in one direction per the circuit design.
8. US and international patents may apply.
9. Electrostatic Sensitive Device. Observe precautions for handling.

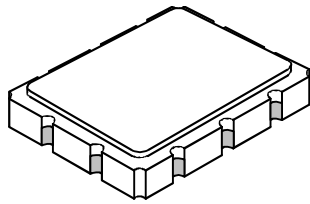


Electrical Connections

Connection	Terminals
Port 1 Hot (Input)	1
Port 1 Gnd Return	10
Port 2 Hot (Output)	6
Port 2 Gnd Return	5
Case Ground	All others

SM9171-10 Case

10-Terminal Ceramic Surface-Mount Case
9.1 x 7.1 mm Nominal Footprint

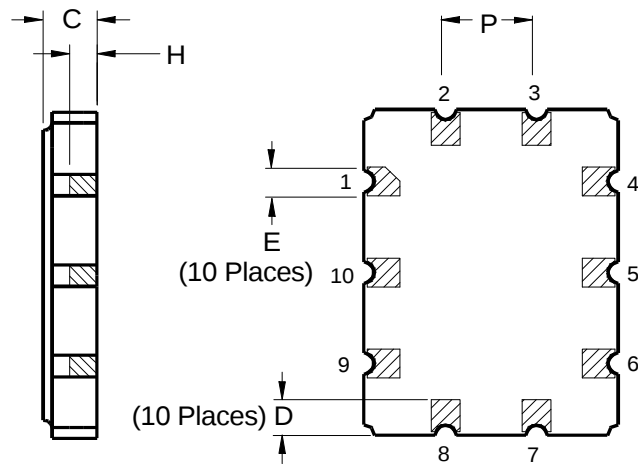
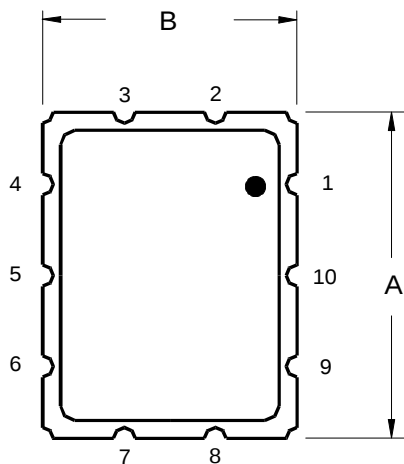


Case Dimensions

Dimension	mm			Inches		
	Min	Nom	Max	Min	Nom	Max
A	8.86	9.09	9.40	0.349	0.358	0.370
B	6.88	7.11	7.40	0.271	0.280	0.291
C		1.91	2.00		0.075	0.079
D		0.99			0.039	
E		0.79			0.031	
H		1.0			0.039	
P		2.54			0.100	

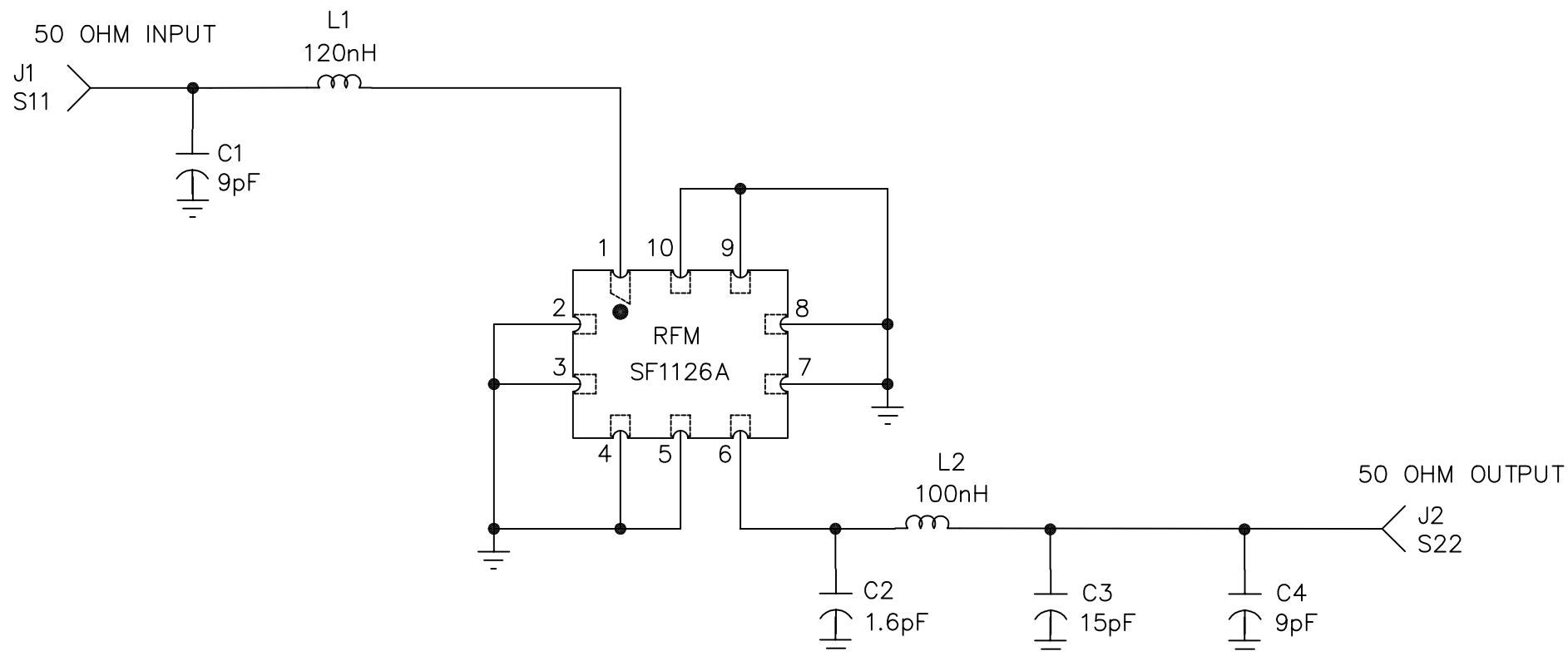
Electrical Connections

Connection		Terminals
Port 1	Output or Return	1
	Return or Output	10
Port 2	Input or Return	6
	Return or Input	5
Ground		All others
Single Ended Operation		Return is ground
Differential Operation		Return is hot



NOTES:

REV	ECN NO.	DESCRIPTION	APP/DATE
A	8180	INITIAL RELEASE	08oct99



SCHEMATIC

D.U.T. VIEWED FROM TOP

DRAWN BY/DATE: J.F.Christopherson 08oct99

TITLE: ASSEMBLY DIAGRAM, SF1126A-DEMO

RF Monolithics, Inc.
DALLAS, TEXAS 75244

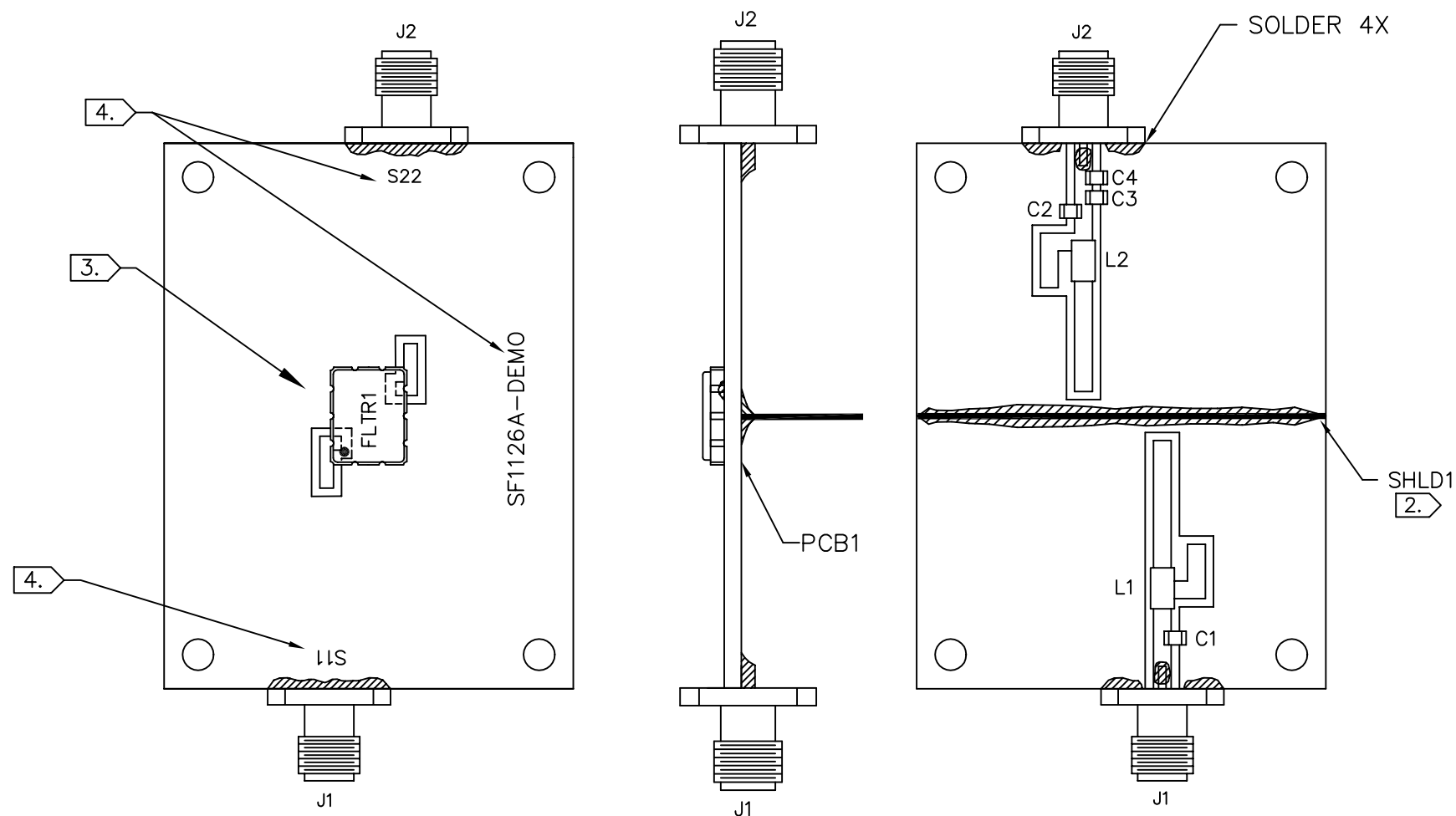
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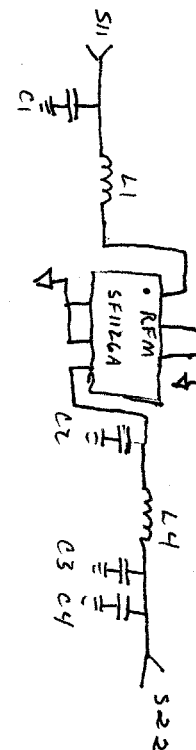
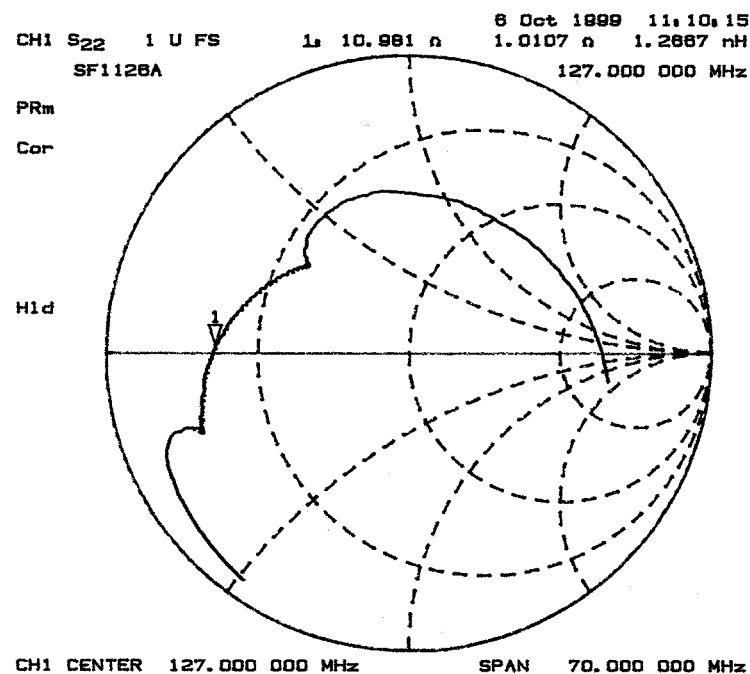
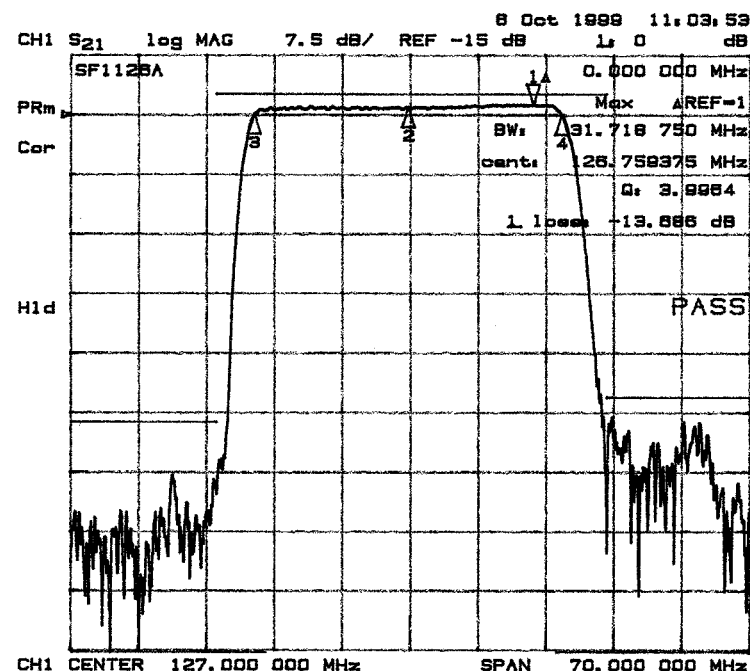
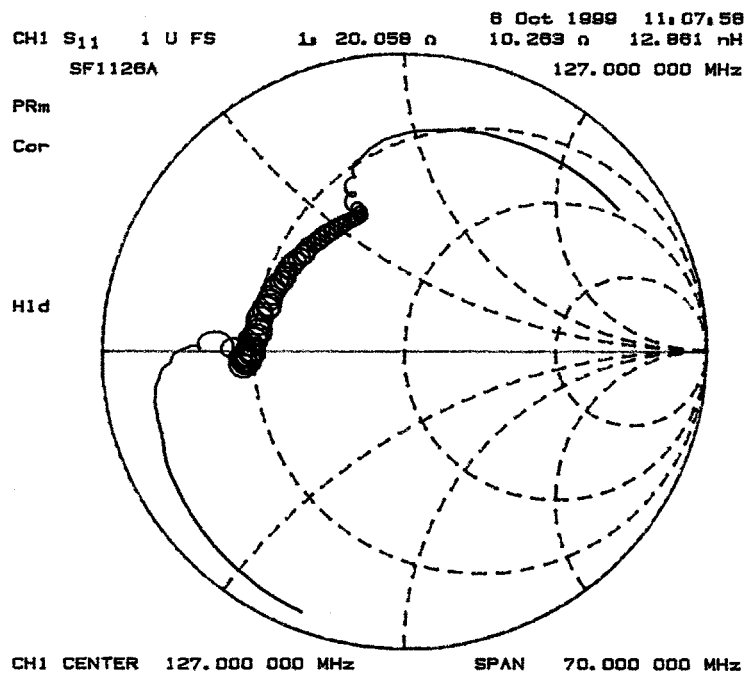
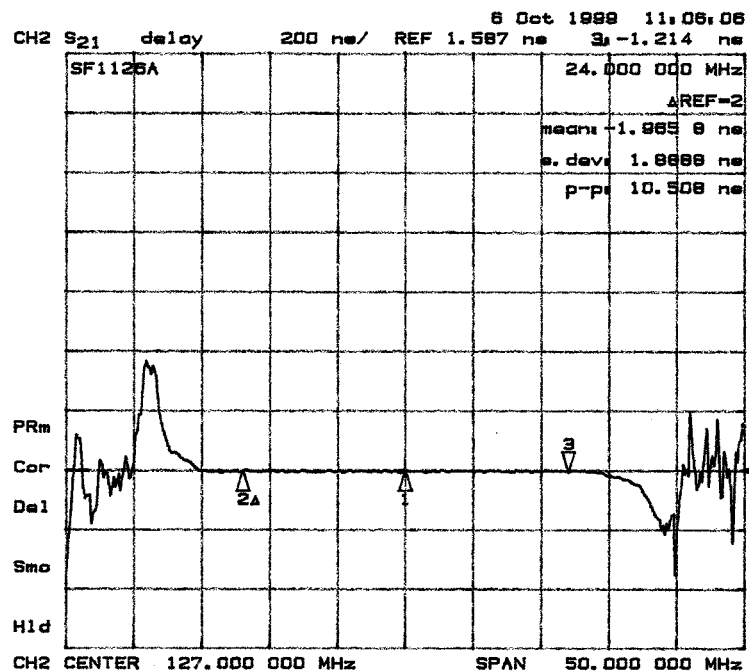
REV A
SHEET 1/3

NOTES:

1. SOLDER MOUNT COMPONENTS AND CONNECTORS TO PCB1
2. SOLDER SHLD1 AS SHOWN AND TRIM TAB FROM SHIELD SO THAT IT IS FLUSH WITH PCB.
3. ORIENT THE FLTR1 AND SOLDER IT DOWN TO THE BOARD AS SHOWN
4. LABEL AS SHOWN.



SF1126A
 DEMO BOARD #1
 10-6-99
 Lot #13



C₁, C₄ = 9.0 pF.
 C₂ = 1.6 pF.
 C₃ = 15 pF.
 L₁ = 120 nH
 L₂ = 100 nH

SF1126A - 000