SE 6200

Single Chip High Performance RF Transceiver

Applications

- *UHF wireless data transmitters and receivers*
- *Wireless alarm and security systems*
- *418 and 433 MHz ISM band systems*
- *Keyless entry with acknowledgement*
- *Remote control systems*
- *Home security and automation*
- *Low power telemetry*
- *Remote metering*
- *Environmental control*

Product Description

SE 6200 is a single-chip high performance half-duplex UHF transceiver designed for low-power and low-voltage wireless applications. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) frequency bands at 418 and 433 MHz, but can easily be programmed for operation at other frequency bands in the 300-500 MHz range.

The main operating parameters of *SE 6200* can be programmed via a serial interface, thus making *SE 6200* a very flexible and easy to use component. In a typical system *SE 6200* will be used together with a microcontroller and a few external passive components.

Features

- Single chip RF transceiver
- Ideal for low cost short range communication
- Frequency range 300MHz to 500MHz
- High sensitivity (typical -112 dBm)
- Programmable output power up to 25mW
- Small size (SSOP-28 package)
- Low supply voltage (2.7V to 3.3V)
- Very few external components required
- FSK modulation
- Data-rate up to 9.6 kbit/s
- Suitable for both narrow and wide band systems
- Suitable for frequency hopping protocols
- Frequency-Lock indicator
- Development kit available
- Easy-to-use software for generating the *SE 6200* configuration data.

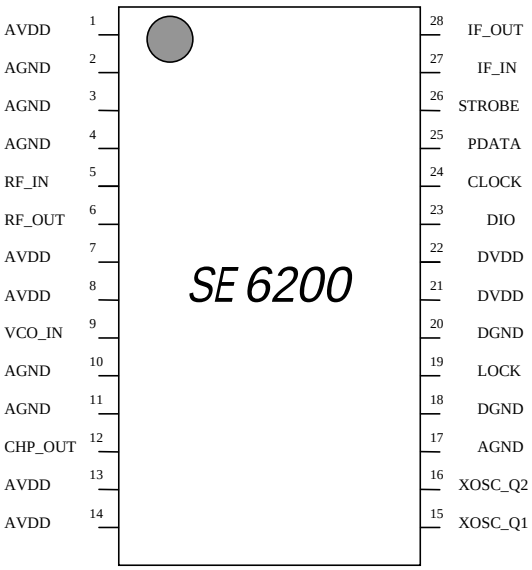
This document contains information on a preproduction product. Specifications and information herein are subject to change without notice.

Pin Assignment

Pin no.	Pin name	Pin type	Description
1	AVDD	Power (A)	Power supply (3V) for analog modules
2	AGND	Ground (A)	Ground connection (0V) for analog modules
3	AGND	Ground (A)	Ground connection (0V) for analog modules
4	AGND	Ground (A)	Ground connection (0V) for analog modules
5	RF_IN	RF Input	RF signal input from antenna (external ac-coupling)
6	RF_OUT	RF output	RF signal output to antenna
7	AVDD	Power (A)	Power supply (3V) for analog modules
8	AVDD	Power (A)	Power supply (3V) for analog modules
9	VCO_IN	Analog input	External VCO-tank input
10	AGND	Ground (A)	Ground connection (0V) for analog modules
11	AGND	Ground (A)	Ground connection (0V) for analog modules
12	CHP_OUT	Analog output	Charge pump current output
13	AVDD	Power (A)	Power supply (3V) for analog modules
14	AVDD	Power (A)	Power supply (3V) for analog modules
15	XOSC_Q1	Analog input	Crystal, pin 1, or external clock input
16	XOSC_Q2	Analog output	Crystal, pin 2
17	AGND	Ground (A)	Ground connection (0V) for analog modules
18	DGND	Ground (D)	Ground connection (0V) for digital modules
19	LOCK	Digital output	PLL Lock indicator. Output is high when PLL is in lock.
20	DGND	Ground (D)	Ground connection (0V) for digital modules
21	DVDD	Power (D)	Power supply (3V) for digital modules
22	DVDD	Power (D)	Power supply (3V) for digital modules
23	DIO	Digital input/output (bidirectional)	Data input in transmit mode Demodulator output in receive mode
24	CLOCK	Digital input	Programming clock for 3-wire bus
25	PDATA	Digital input	Programming data for 3-wire bus
26	STROBE	Digital input	Programming strobe (Load) for 3-wire bus
27	IF_IN	Analog input	Input to IF chain (from external ceramic filter). The input impedance is 1.5 kΩ so a direct connection to an external ceramic filter is possible.
28	IF_OUT	Analog output	Output from first amplifier in IF-chain (to external ceramic filter). The output impedance is 1.5 kΩ so a direct connection to an external ceramic filter is possible.

A=Analog, D=Digital

(Top view)



Absolute Maximum Ratings

Parameter	Min.	Max.	Units	Condition
Supply voltage, VDD	-0.3	7.0	V	
Voltage on any pin	-0.3	VDD+0.3, max 7.0	V	
Input RF level		10	dBm	
Storage temperature range	-50	150	°C	
Operating ambient temperature range	-30	85	°C	
Lead temperature		260	°C	T = 10 s

Under no circumstances the absolute maximum ratings given above should be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

Electrical Specifications

Parameter	Min.	Typ.	Max.	Unit	Condition
Overall					
RF Frequency Range	300	418 433.92	500	MHz	Programmable in steps of 5 kHz
Transmit Section					
Transmit data rate	0.3	2.4	9.6	kbit/s	Manchester code is required. (9,6 kbit/s equals 19,2 kbaud using Manchester code)
Binary FSK frequency separation	2	10	100	kHz	The frequency corresponding to the digital "0" is denoted f_0, while f_1 corresponds to a digital "1". The frequency separation is f_1-f_0. The RF carrier frequency, f_c, is then given by $f_c=(f_0+f_1)/2$. (The frequency deviation is given by f_d=+/-(f_1-f_0)/2) The frequency separation is programmable in steps of 1 kHz.
Programmable output power	0	10	14	dBm	Delivered to matched load. The output power is programmable in steps of 1 dB.
RF output impedance			400Ω || 3pF		Transmit mode, parallel equivalent. For matching details see “Input/ output matching” p. 13.
Harmonics		-30		dBc	Using high output power level an external LC or SAW filter may be used to reduce harmonics emission to comply with ISM requirements. See p.13

Parameter	Min.	Typ.	Max.	Unit	Condition
Receive Section					
Receiver Sensitivity		-112		dBm	Measured at a data rate of 1.2 kbit/s and 10 kHz frequency separation with a bit error rate better than 10^{-3}
Cascaded noise figure		3		dB	
LO leakage		-57		dBm	
Input impedance		39Ω +4.9pF			Receive mode, series equivalent. For matching details see “Input/ output matching” p. 13
Turn on time		500 3 5 30		µs ms ms ms	With precharging, 9.6 kbit/s Without precharging, 9.6 kbit/s With precharging, 1.2 kbit/s Without precharging, 1.2 kbit/s See “Demodulator precharging for reduced turn-on time” p. 15
IF Section					
Intermediate frequency (IF)		60 200 455		kHz kHz kHz	The IF is programmable. Either 60kHz, 200kHz or 455kHz can be chosen. An optional external IF filter can be used if 455 kHz is chosen. The impedance level is 1,5 kOhm
Frequency Synthesiser Section					
Crystal Oscillator Frequency	4	12	13	MHz	
Crystal frequency accuracy requirement		+/- 50		ppm	The crystal frequency accuracy and drift (ageing and temperature dependency) will determine the frequency accuracy of the transmitted signal.
Crystal operation		parallel			12 pF load capacitance
Output signal phase noise		-70 -90		dBc/Hz dBc/Hz	10kHz offset from carrier 100 kHz offset from carrier
RX / TX turn time		100		µs	
PLL turn-on time, crystal oscillator off in power down mode		4		ms	

Parameter	Min.	Typ.	Max.	Unit	Condition
PLL turn-on time, crystal oscillator on in power down mode		2		ms	
Digital Inputs/Outputs					
Logic "0" input voltage	0		0.3*VDD	V	
Logic "1" input voltage	0.7*VDD		VDD	V	
Logic "0" output voltage	0		0.4	V	Output current -2.5mA, 3.0V supply voltage
Logic "1" output voltage	2.5		VDD	V	Output current 2.5mA, 3.0V supply voltage
Logic "0" input current	NA		-1	µA	Input signal equals GND
Logic "1" input current	NA		1	µA	Input signal equals VDD
Power Supply					
Supply voltage		3.0		V	Recommended operation voltage
	2.7		3.3	V	Operating limits
Current Consumption, receive mode		18		mA	
Current Consumption, transmit mode:					
P=1mW (0dBm)		29		mA	The ouput power is delivered to a 50Ω load
P=10mW (10dBm)		50		mA	
P=20mW (13dBm)		62		mA	
P=25mW (14dBm)		69		mA	
Current Consumption, Power Down		23 0.2	 1	µA µA	Oscillator core on Oscillator core off

Circuit Description

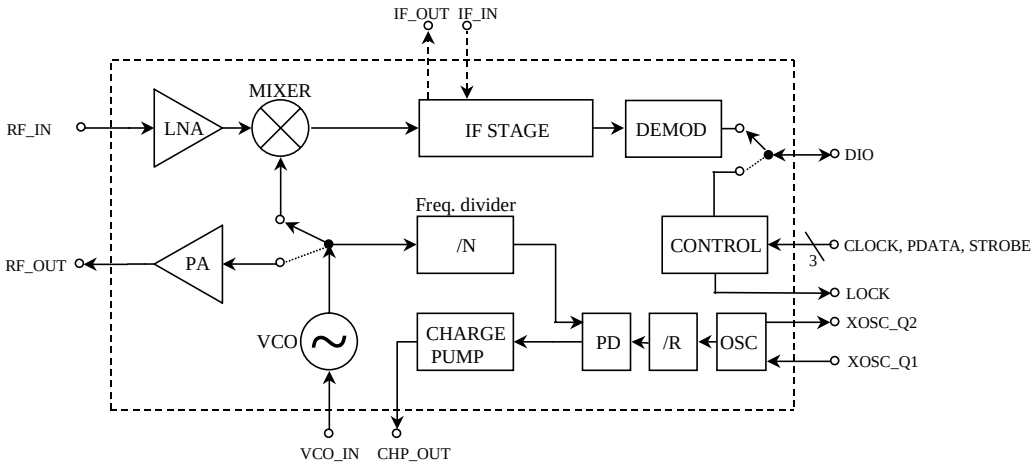


Figure 1. Simplified block diagram of the *SE 6200*.

A simplified block diagram of *SE 6200* is shown in figure 1. Only signal pins are shown.

In receive mode *SE 6200* is configured as a traditional heterodyne receiver. The RF input signal is amplified by the low-noise amplifier (LNA) and converted down to the intermediate frequency (IF) by the mixer (MIXER). In the intermediate frequency stage (IF STAGE) this downconverted signal is amplified and filtered before being fed to the demodulator (DEMOD). As an option an external IF filter can be used for improved performance. After demodulation *SE 6200* outputs the raw digital demodulated data on the pin DIO. Synchronisation and final qualification of the demodulated data is done by the interfacing digital system (microcontroller).

In transmit mode the voltage controlled oscillator (VCO) output signal is fed directly to the power amplifier (PA). The RF output is frequency shift keyed (FSK) by the digital bit stream fed to the pin DIO. The internal T/R switch circuitry makes the antenna interface and matching very easy.

The frequency synthesiser generates the local oscillator signal which is fed to the MIXER in receive mode and to PA in transmit mode. The frequency synthesiser consists of a crystal oscillator (XOSC), phase detector (PD), charge pump (CHARGE PUMP), VCO, and frequency dividers (/R and /N). An external crystal must be connected to XOSC, and an external LC-tank with a varactor diode is required for the VCO. For flexibility the loop filter is external.

For chip configuration *SE 6200* includes a 3-wire digital serial interface (CONTROL).

Configuration Overview

SE 6200 can be configured to achieve the best performance for different applications. Through the programmable configuration registers the following key parameters can be programmed:

- Receive/Transmit mode
- RF output power level
- Power amplifier operation class (A, AB, B or C)
- Frequency synthesiser key parameters: (RF output frequency, FSK modulation frequency separation (deviation), crystal oscillator reference frequency
- Power-down/power-up mode
- Reference oscillator on or off in power down mode (when on, shorter frequency synthesiser start-up time is achieved).
- The IF (intermediate frequency) can be set to either 60kHz, 200kHz or 455kHz using on-chip filters, or 455kHz using an external filter
- Data rate can be selected
- Synthesiser lock indicator mode. The lock detection can be enabled/disabled. When enabled, two lock detection modes can be chosen, either "mono-stable" or continuous.
- In receive mode precharging of the demodulator can be used to achieve faster settling time (see p. 15).

Configuration Software

HKW ELEKTRONIK GMBH will provide users of *SE 6200* with a program (Windows interface) that generates all necessary *SE 6200* configuration data based on the user's selections of various parameters. Based on the selections 8 hexadecimal numbers are generated. These hexadecimal numbers will then be the necessary input to the microcontroller for configuration of *SE 6200*. In addition the program will provide the user with the component values needed for the PLL loop filter and the input/output matching circuit.

Figure 2 shows the user interface of the *SE 6200* configuration software.

Figure 2. *SE 6200* **configuration software user interface**

3-wire Serial Interface

SE 6200 is programmed via a simple 3-wire interface (STROBE, PDATA and CLOCK). A full configuration of *SE 6200* requires sending 8 data frames of 16 bits each. With a clock rate of 2MHz the time needed for a full configuration will therefore be less than 100µs. Setting the device in power down mode requires sending one frame only and will therefor take less than 10 µs.

In each write-cycle 16 bits are sent on the PDATA-line. The three most significant bits of each data frame (*bit15*, *bit14* and *bit13*) are the address-bits. *Bit15* is the MSB of the address and is sent as the first bit. See figure 3.
A timing diagram for the programming is shown in figure 4. The clocking of the data on PDATA is done on the negative edge of CLOCK. When the last bit, *bit0*, of the sixteen bits has been loaded, the STROBE-pulse must be brought high and then low to load the data.

The configuration data will be valid after a programmed power-down mode, but not when the power-supply is turned off.

The timing specifications are given in table 1.

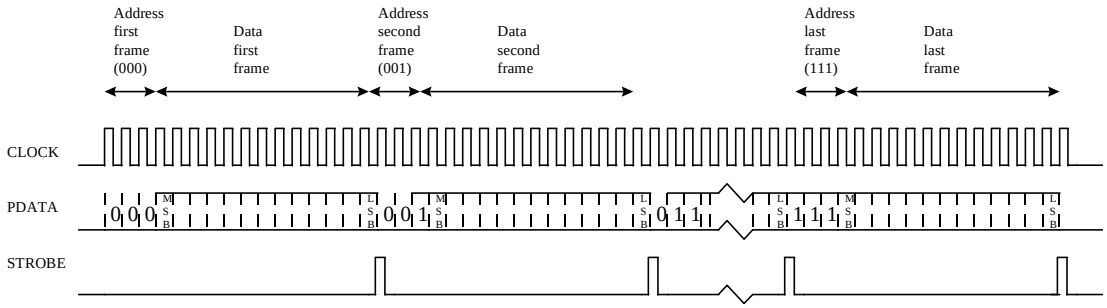


Figure 3. Serial data transfer (full configuration)

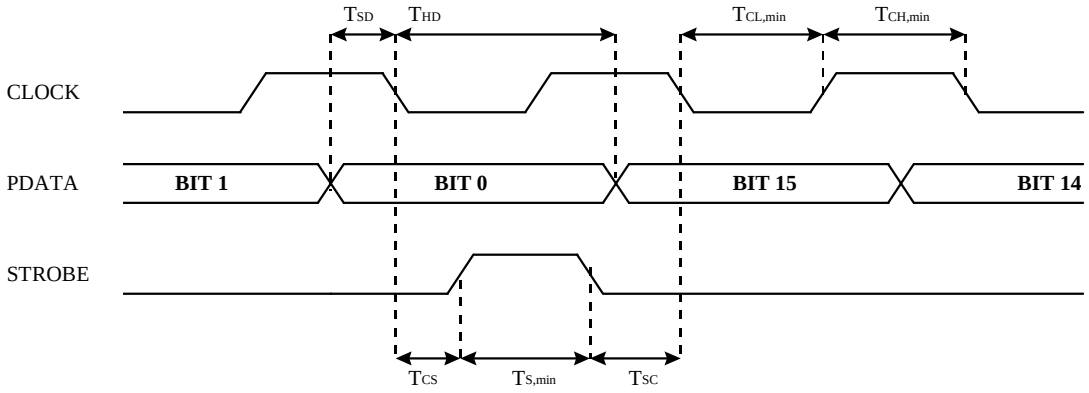


Figure 4. Timing diagram, serial interface

Table 1. Serial interface, timing specification

Parameter	Symbol	Min	Max	Units	Conditions
CLOCK, clock frequency	F_{CLOCK}	-	2	MHz	
CLOCK low pulse duration	$T_{CL,min}$	50		ns	The minimum time CLOCK can be low.
CLOCK high pulse duration	$T_{CH,min}$	50		ns	The minimum time CLOCK can be high.
PDATA setup time	T_{SD}	5	-	ns	The minimum time data on PDATA must be ready before the negative edge of CLOCK.
PDATA hold time	T_{HD}	5	-	ns	The minimum time data must be held at PDATA, after the negative edge of CLOCK.
CLOCK to STROBE time	T_{CS}	5	-	ns	The minimum time after the negative edge of CLOCK before positive edge of STROBE.
STROBE to CLOCK time	T_{SC}	5	-	ns	The minimum time after the negative edge of STROBE before negative edge of CLOCK.
STROBE pulse duration	$T_{S,min}$	50		ns	The minimum time STROBE can be high.
Rise time	T_{rise}		100	ns	The maximum rise time for CLOCK and STROBE
Fall time	T_{fall}		100	ns	The maximum fall time for CLOCK and STROBE

Note: The set-up- and hold-times refer to 50% of VDD.

Microcontroller Interface

Used in a typical system, *SE 6200* will interface to a microcontroller. This microcontroller must be able to:

- Program the *SE 6200* into different modes via the 3-wire serial interface (PDATA, STROBE, CLOCK).
- Operate with the bidirectional data pin DIO.
- Perform oversampling of the demodulator output (on pin DIO), recover the clock corresponding to the actual datarate, and perform data qualification (on Manchester encoded data).
- Data to be sent must be Manchester encoded.
- Optionally the microcontroller can monitor the frequency lock status from pin LOCK.
- Optionally the microcontroller can perform precharging of the receiver in order to reduce the turn-on time (see p.15).

Connecting the microcontroller
The microcontroller uses 3 output pins for the serial interface (PDATA, STROBE and CLOCK. A bi-directional pin is used for data to be transmitted and data received. Optionally another pin can be used to monitor the LOCK signal. This signal is logic level high when the PLL is in lock. See figure 6.

Data transmission
The data to be sent has to be Manchester encoded (also known as bi-phase-level coding). The Manchester code ensures that the signal has a constant DC component that is necessary for the FSK demodulator. The Manchester code is based on transitions; a “0” is encoded as a low-to-high transition, a “1” is encoded as a high-to-low transition. See figure 5. When the DIO is logic level high, the upper FSK frequency is transmitted. The lower frequency is transmitted when DIO is low.

Note that the receiver data output is inverted when using low-side LO.

Data reception
The output of the demodulator (*DIO*) is a digital signal (alternating between 0V and VDD). For small input signals, there will be some noise on this signal, located at the edges of the digital signal. The datarate of this signal may be up to 9.6 kbit/s. Due to the Manchester coding, the fundamental frequency of the signal is also 9.6kHz. An oversampling of 10-20 times the frequency of the demodulator-output is recommeded. I.e. the sampling frequency should at least be 100-200kHz for 9.6kbit/s. For a lower datarate the sampling frequency can be reduced.

The data sampled by the microcontroller, must be stored in an accumulating register. The length of this register will typically be 10-20 bits (depending on the oversampling ratio). The qualification of the data (decide whether the signal is “0” or “1”) *can* be based on comparing the number 0’s with the number of 1’s.

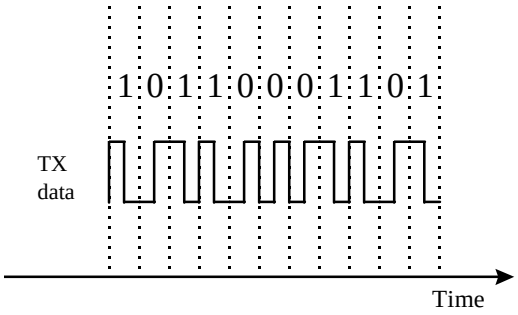


Figure 5. Manchester encoding

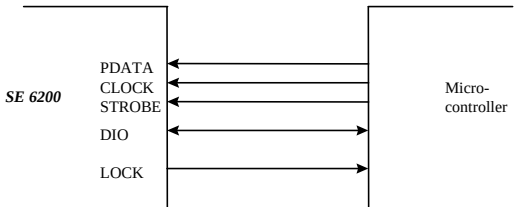


Figure 6. Microcontroller interface

Application Circuit

Very few external components are required for operation of *SE 6200*. A typical application circuit for 433.92 MHz operation is shown in figure 7. 1.2kbps data rate and 10 kHz FSK separation is used. Component values are shown in table 2.

Input / output matching
L51 and C51 are the input match for the receiver, and L61 and C61 is the output match for the transmitter. An internal T/R switch circuitry makes it possible to connect the input and output together matching to 50Ω. See “Input/output matching” p.13 for details.

Synthesiser loop filter and VCO tank
The PLL loop filter consist of C121-C123 and R121-R123.

The VCO tank consist of C91-C93, L91 and the varactor (VAR). C91 determines the coupling to the internal VCO amplifier, and thus the VCO loop gain. This loop gain is also controlled by the “VCO gain” setting in the Configuration data software by changing the amplifier curent. C92 together with the varactor´s capacitance ratio determines the VCO sensitivity (MHz/V). The sensitivity should be 20 MHz/V. L91 and C93 is used to set the absolute range of the VCO.
Component values are easily calculated using the Configuration data software.

Additional filtering
Additional external components (e.g. ceramic IF-filter, RF LC or SAW-filter) may be used in order to improve the performance for specific applications.
See also “Optional LC filter” p.13 for further information.

Voltage supply decoupling
C10-C12, C210 and C211 are voltage supply de-coupling capacitors. These capacitors should be placed as close as possible to the voltage supply pins of *SE 6200*

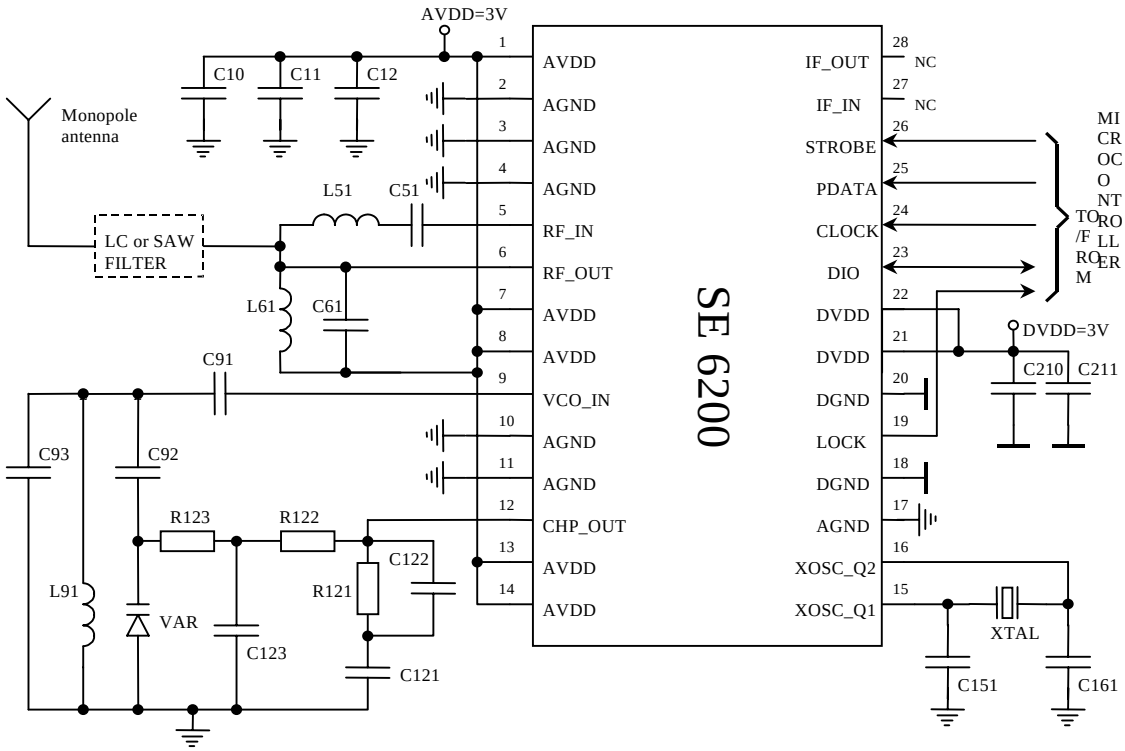


Figure 7
Typical SE 6200 application for 433.92 MHz operation.

Table 2. Bill of materials for application circuit

Item	Description
C10	33nF, X7R, 0805
C11	1nF, C0G, 0603
C12	220pF, COG, 0603
C51	220pF, COG, 0603
C61	15pF, C0G, 0603
C91	4.7pF, C0G, 0603
C92	8.2pF, C0G, 0603
C93	3,9pF, C0G, 0603
C121	33nF, X7R, 0603
C122	1,5nF, C0G, 0603
C123	330pF, C0G, 0603
C161	15pF , C0G, 0603
C151	15pF , C0G, 0603
C210	33nF, X7R, 0603
C211	1nF, C0G, 0603
L51	39nH, 0805
L61	8,2nH, 0805
L91	10nH, 0805
R121	5,6kΩ, 0603
R122	27kΩ, 0603
R123	22kΩ, 0603
VAR	KV1832C, TOKO
XTAL	12 MHz crystal, 12pF load

Input / Output Matching

Four passive external components combined with the internal T/R switch circuitry ensures match in both RX and TX mode. The matching network for 433.92 MHz is shown in figure 8. The component values may have to be optimised to include layout parasitics. Matching components for other frequencies can be found using the configuration software.

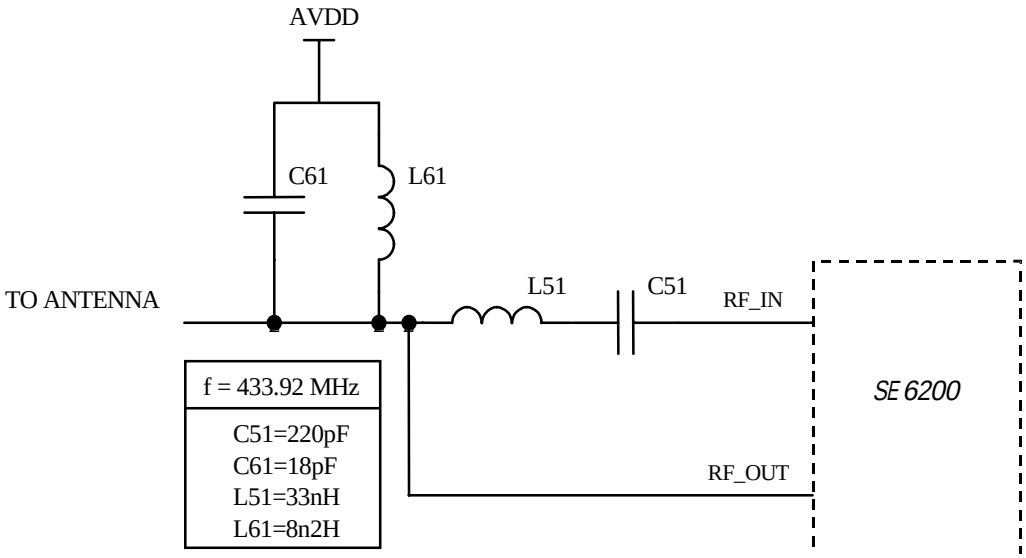


Figure 8.
Input/output matching network

Optional LC Filter

An optional LC filter may be added between the antenna and the matching network in certain applications. The filter will reduce the emission of harmonics and increase the receiver selectivity. The filter for use at 433.92 MHz is shown in figure 9. The filter is designed for 50Ω terminations. The component values may have to be optimised to include layout parasitics and the values for other frequencies can be found using the configuration software.

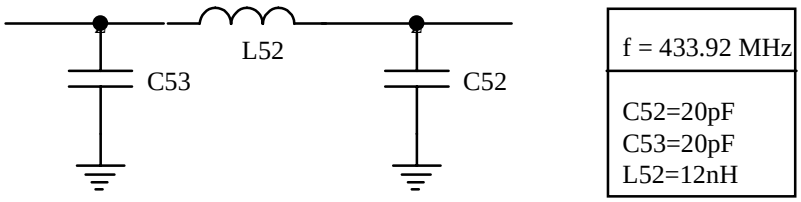


Figure 9.
LC filter

Antenna Considerations

The *SE 6200* can be used together with various types of antennas. The most common antennas for short range communication are monopole, helical and loop antennas.

Monopole antennas are resonant antennas with a length corresponding to one quarter of the electrical wavelength (λ/4) . They are very easy to design and can be implemented simply as a “piece of wire” or integrated into the PCB.

Non-resonant monopole antennas shorter than λ/4 can also be used, but at the expense of range. In size and cost critical applications such an antenna may very well be integrated into the PCB.

Helical antennas can be thought of as a combination of a monopole and a loop antenna. They are a good compromise in size critical applications. But helical antennas tend to be more difficult to optimise than the simple monopole.
Loop antennas are easy to integrate into the PCB, but are less effective due to difficult impedance matching because of their very low radiation resistance.

For low power applications the λ/4-monopole antenna is recommended giving the best range and because of its simplicity.

The length of the λ/4-monopole antenna is given by:

$$L = 7125 / f$$

where f is in MHz, giving the length in cm. An antenna for 433.92 MHz should be 16.4 cm.

The antenna should be connected as close as possible to the IC. If the antenna is located away from the input pin the antenna should be matched to the feeding transmission line.

System Considerations And Guidelines

Low cost systems
In systems where low cost is of great importance the 200kHz IF should be used. The oscillator crystal can then be a low cost crystal with 50ppm frequency tolerance.

Battery operated systems
In low power applications the power down mode should be used when not being active. Depending on the start-up time requirement, the oscillator core can be powered during power down. Precharging of the demodulator may also be used to reduce the receiver turn-on time, see description p. 15.

Narrow band systems
SE 6200 is also suitable for use in narrow band systems. However, it is then required to use a crystal with low temperature drift and ageing. A trimmer capacitor in the crystal oscillator circuit (in parallel with C151) may also be necessary to set the initial frequency.

It is also possible to include an external IF-filter at 455kHz. This should be a ceramic filter with 1.5kΩ impedance connected between IF_OUT and IF_IN.

Due to the high Q of such a filter, a 1-2 dB increase in sensitivity can be achieved.

High reliability systems
Using a SAW filter as a preselector will improve the communication reliability in harsh environments by reducing the probability of blocking.

Spread spectrum frequency hopping systems
Due to the very fast frequency shift properties of the PLL, the *SE 6200* may very well be used in frequency hopping systems.

Demodulator Precharging For Reduced Turn-on Time

The demodulator data slicer has an internal AC coupling giving a time constant of approximately 30 periods of the bit rate period. This means that before proper demodulation can take place, a minimum of 30 start-bits has to be received.

In critical applications where the start-up time should be decreased in order to reduce the power consumption, this time constant can be reduced to 5 periods using the optional precharging possibility. The precharging is done during data reception by setting the precharging bit in the configuration register active with a duration of at least 5 bit periods.

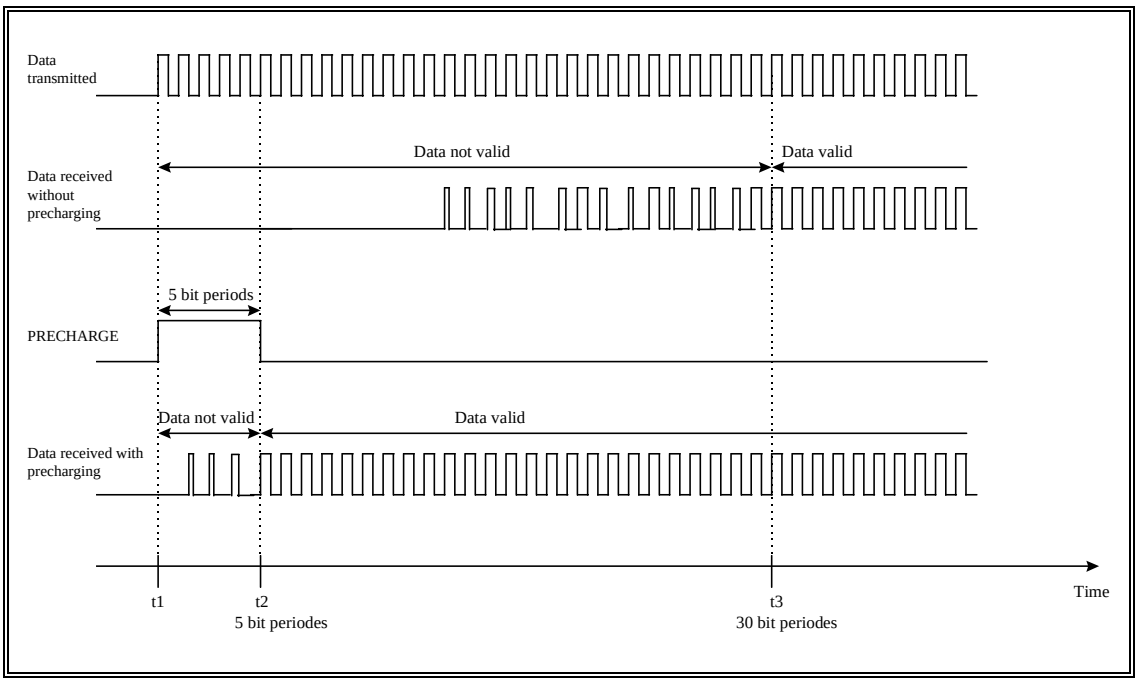


Figure 10: Demodulation using precharging

In the example shown in figure 10, data are transmitted continuously from the transmitter (all 1's). At $t=t_1$ the receiver is turned on, and then the precharging is kept on for about 5 bit periods. At $t=t_2$ the received data are valid and precharging is turned off. When not using precharging, data is not valid until 30 bit periods, at $t=t_3$.

PCB Layout Recommendations

A two layer PCB is highly recommended. The bottom layer of the PCB should be the "ground-layer".

The top layer should be used for signal routing, and the open areas should be filled with metallisation connected to ground using several vias.

The ground pins should be connected to ground as close as possible to the package pin. The decoupling capacitors should also be placed as close as possible to the supply pins and connected to the ground plane by separate vias.

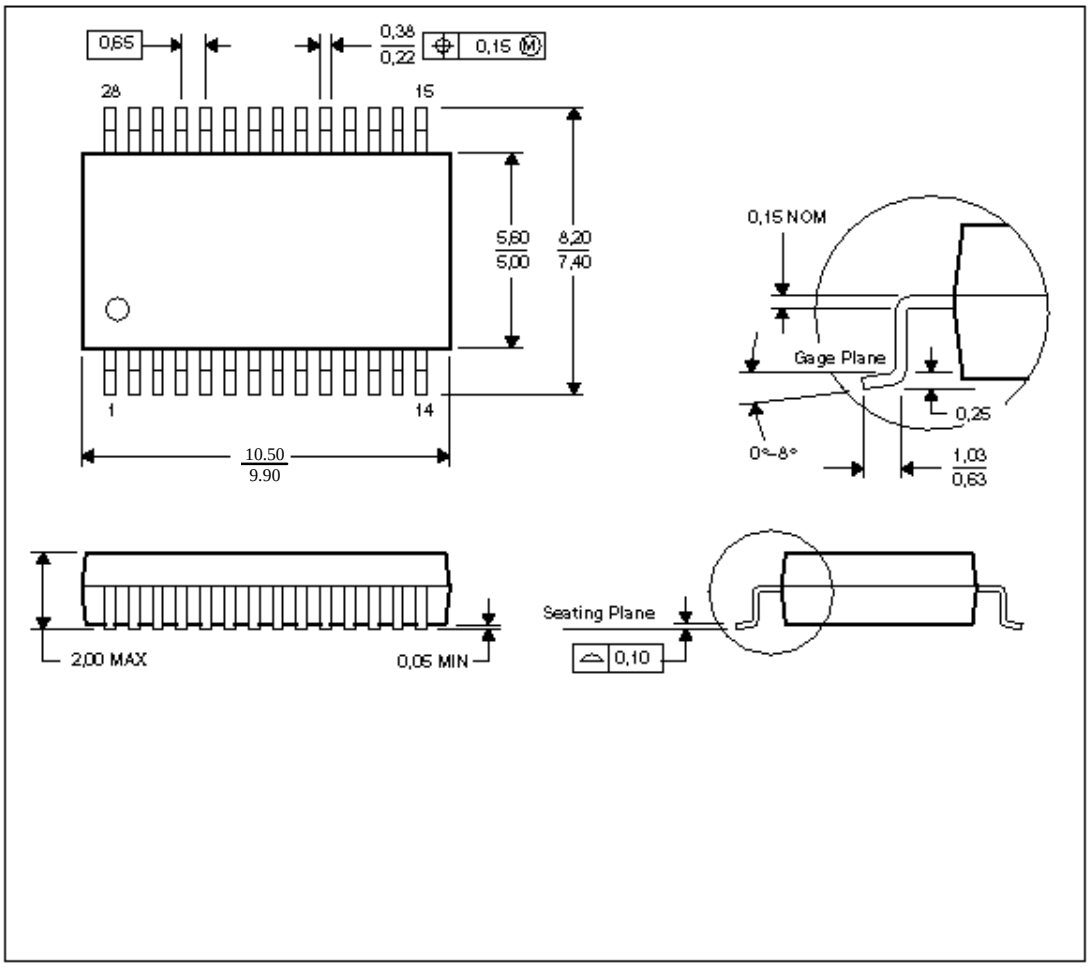
The external components should be as small as possible and surface mount devices should be used.

Precaution should be used when placing the microcontroller in order to avoid interference with the RF circuitry.

In certain applications where the ground plane for the digital circuitry is expected to be noisy, the ground plane may be split in an analogue and a digital part. All AGND pins and AVDD decoupling capacitors should be connected to the analogue ground plane. All DGND pins and DVDD decoupling capacitors should be connected to the digital ground. The connection between the two ground planes should be implemented as a star connection with the power supply ground.

A development kit with fully assembled PCB is available, and can be used as a guideline for layout.

Package Description (SSOP-28)



NOTES :

A. All linear dimensions are inn millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.1mm
D. Falls within JEDEC MO-150

Ordering Information

Ordering part number	Description
SE 6200	Single Chip RF Transceiver
SE 6200-DBK	Demonstration Board Kit
SE 6200-SK	SE 6200 Sample Kit (5 pcs.)

Note

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SE6200-a.doc