

The SL3522 is a monolithic seven stage successive detection logarithmic amplifier integrated circuit for use in the 100MHz to 500MHz frequency range. It features an on-chip video amplifier with provision for external adjustment of log Slope and offset. It also features a balanced RF output. The SL3522 operates from supplies of $\pm 5V$.

FEATURES

- 75dB Dynamic Range
- Surface Mount SO Package
- Adjustable Log Slope and Offset
- 0dBm RF Limiting Output
- 60dBm Limiting Range
- 2V Video Output Range
- Low Power (Typ. 1W)
- Temperature Range (T_{CASE}): $-55^{\circ}C$ to $+125^{\circ}C$

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised and Monpulse Radar
- Instrumentation

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 6.0V$
Storage temperature	$-65^{\circ}C$ to $+175^{\circ}C$
Junction temperature	$+175^{\circ}C$
Thermal resistance	
Die-to-case	$15.5^{\circ}C/W$
Die-to-ambient	$76.5^{\circ}C/W$
Applied DC voltage to RF input	$\pm 400mV$
Applied RF power to RF input	$+15dBm$

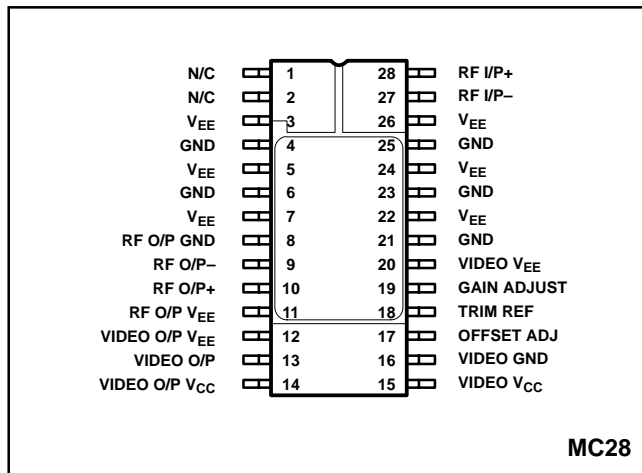


Fig.1 Pin connections - top view

ORDERING INFORMATION

SL3522 A MC (Miniature Ceramic package)

SL3522 C MC (Miniature Ceramic package)

SL3522 NA 1C (Probe-tested bare die)

(Also available: SL3522 AA MC screened to Zarlink HI-REL level A. Contact Zarlink Semiconductor sales outlet for a separate datasheet.)

ESD PROTECTION

To achieve the high frequency performance there are no ESD protection structures on the RF input pins (27, 28). These pins are **highly static sensitive**, typically measured as 250V using MIL-STD-883 method 3015. Therefore, ESD handling precautions are **essential** to avoid degradation of performance or permanent damage to this device.

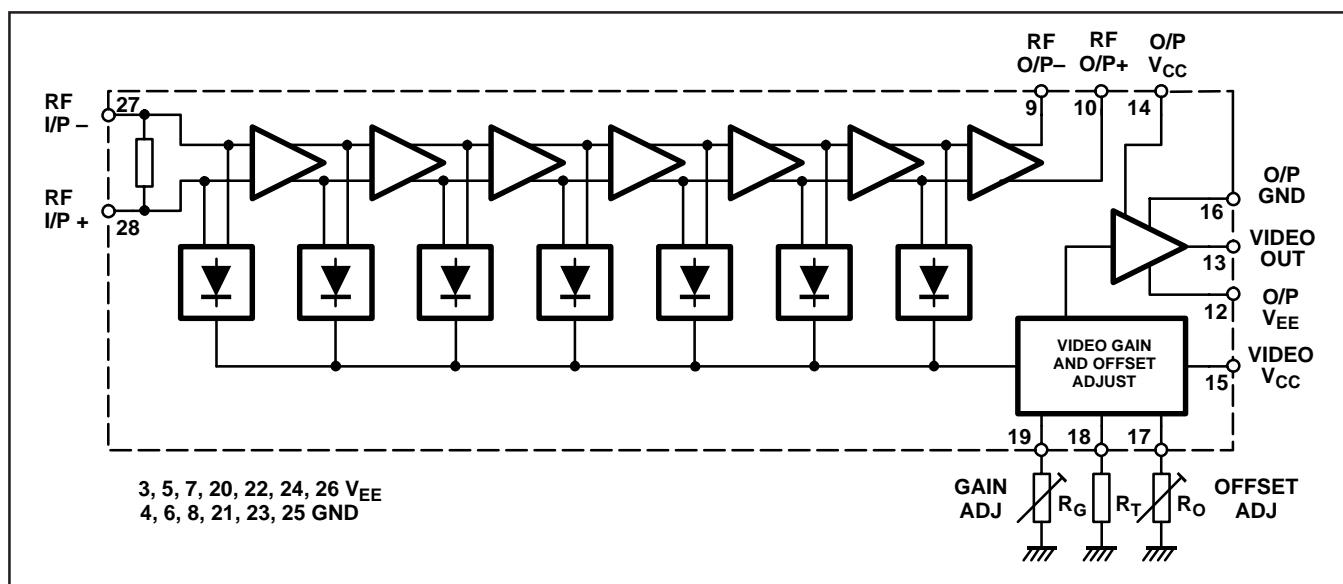


Fig.2 Functional block diagram

ELECTRICAL CHARACTERISTICS

The electrical characteristics are guaranteed over the following range of operating conditions, using test circuit in Fig. 3 (unless otherwise stated):

Temperature range:	Military:	SL3522 A MC, SL3522 NA 1C	55°C to +125°C (T _{CASE})
	Commercial:	SL3522 C MC	0°C to +70°C (T _{CASE})
Supply voltage:	V _{CC} : +4.50V to +5.50V (all grades)		
	V _{EE} : -4.5V to -5.50V (all grades)		
Frequency	=100MHz to 500MHz		
R _g , R _o , R _t	=1.5KΩ		
Video output load	=200Ω//20pF		
Test conditions (unless otherwise stated):			
Temperature:	SL3522 A MC:	+25°C, +125°C & -55°C (T _{CASE})	
	SL3522 C MC:	+25°C	
	SL3522 NA 1C	+25°C	
Supply voltage:	V _{CC} = +5.0V, V _{EE} = -5.0V		

Parameter	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current (quiescent)	14, 15		28	35	mA	V _{CC} = +5.0V
Negative supply current (quiescent)	ALL V _{EE}		150	175	mA	V _{EE} = -5.0V See note 1
	Pins		180	210	mA	V _{EE} = -5.0V See note 2
Dynamic range		75			dB	100 to 400MHz See note 1, 3
		70			dB	See note 1, 4
Linearity		-1		+1	dB	T _{CASE} = -55°C
		-1		+1	dB	T _{CASE} = +25°C
		-1.25		+1.25	dB	T _{CASE} = +125°C
Video output range	13	1.30	1.75	2.00	V	
Video slope	13	18	21	24	mV/dB	
Video slope variation	13	-5		+5	%	See note 5
Video slope adjust range	13	±20	±30		%	R _G = 1kΩ to 2.2kΩ
Video offset	13	-0.1	+0.25	+0.5	V	
Video offset variation	13		-05		mV/°C	T _{CASE} = +25°C
Video offset adjust range	13	±0.5			V	R _O = 1kΩ to 2.2kΩ
Video trim reference voltage	17, 18, 19	-0.59	-0.54	-0.49	V	
Video output impedance	13		10		Ω	See note 8
Video rise time	13		16		ns	10% - 90% (60dB step) See note 7
Input VSWR	27, 28		1.5:1			Z _s = 50Ω See note 7
RF bandwidth	9, 10		450		MHz	T _{CASE} = +25°C R _{FIN} = -70dBm See notes 2, 7
RF limiting range	9, 10		60		dB	See notes 2, 6, 7
RF limited output level	9, 10	-3.0	-1.0	+1.0	dBm	R ₁ = 50Ω single ended See note 2
RF output impedance	9, 10		50		Ω	Single ended See notes 2, 8

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Phase variation with RF Input level			15		Degrees	Freq = 300MHz $RF_{IN} = -60$ to $+10$ dBm See notes 2, 7
Phase tracking between units			3		Degrees	$T_{CASE} = +25^{\circ}C$ FREQ = 300MHz See notes 2, 7

Notes

- 1 RF output buffer OFF (pin 8 disconnected from 0V)
- 2 RF output buffer ON (pin 8 connected to 0V)
- 3 Minimum dynamic range under any single set of operating conditions
- 4 Log linearity guaranteed for pin = -64 dBm to $+6$ dBm for ALL supply, temperature and frequency conditions
- 5 Full range of supply, temperature and frequency conditions
- 6 Input limiting range typically -50 dBm to $+10$ dBm
- 7 Not tested, but guaranteed by characterisation
- 8 Not tested, but guaranteed by design

The SL3522 CANNOT be GUARANTEED to operate below 100MHz and meet the electrical characteristics shown above.

However, characterisation has shown that the device can still function adequately down to frequencies of 50MHz, with the following reservations:-

- 1) The video bandwidth is fixed to approx 40MHz a certain amount of carrier breakthrough on the video O/P (pin 13) will occur, with input signal frequencies below 100MHz.
- 2) There are 2 RF coupling capacitors (20pF) on-chip, which couple the output signal from stage 3 to the input of stage 4 (ref Fig. 24). These can introduce undesirable limiting phase performance for input signal frequencies below 100MHz.

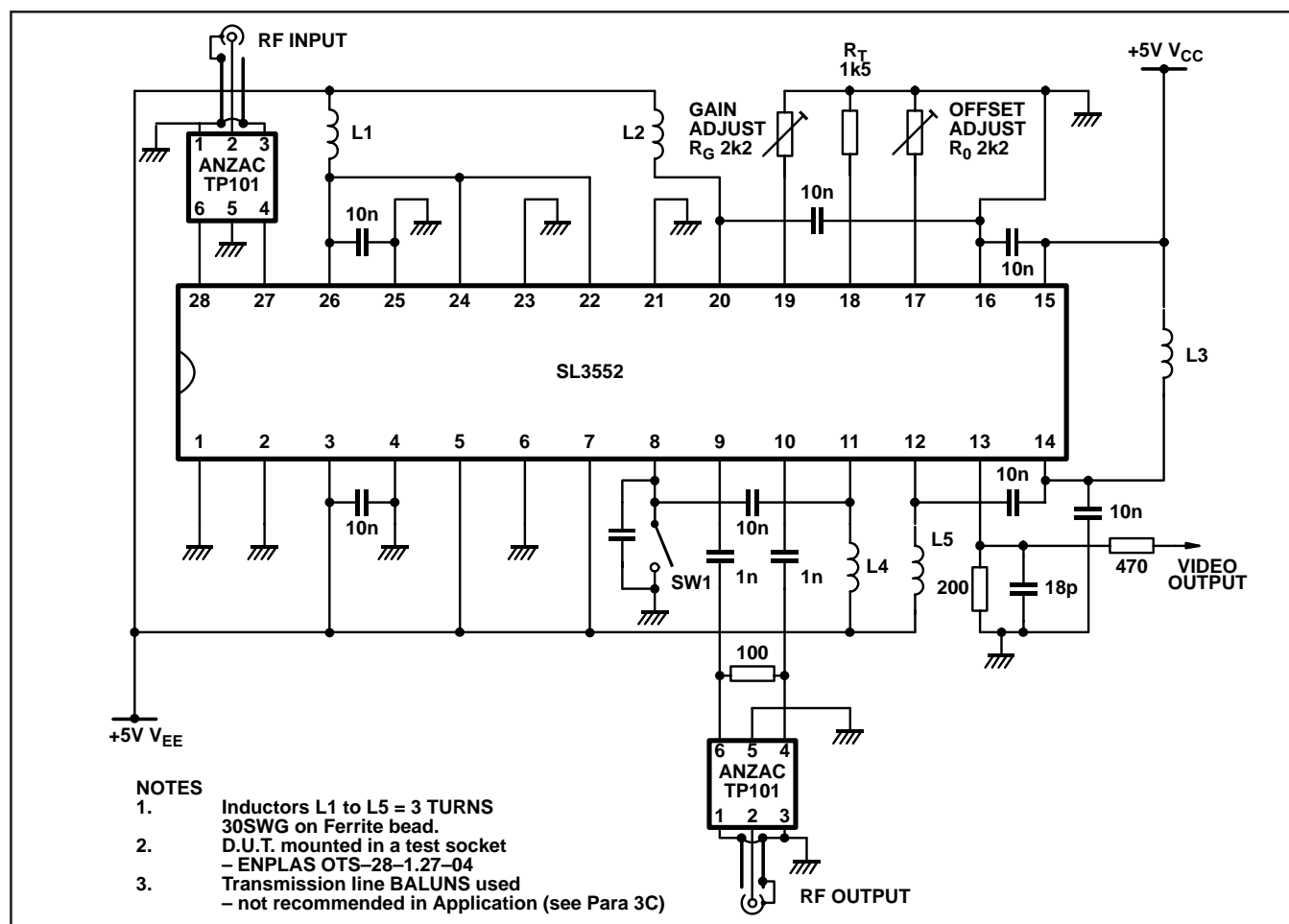


Fig.3 Test circuit

PRODUCT DESCRIPTION

The SL3522 is a complete monolithic successive detection Log/limiting amplifier which can operate over an input frequency range of 100MHz to 500MHz. Producing a log/lin characteristic for input signals between -64dBm and +6dBm, the log amplifier can provide an accuracy of better than $\pm 1.00\text{dB}$ at case temperatures of -55°C and $+25^\circ\text{C}$ and an accuracy of better than $\pm 1.25\text{dB}$ at $+125^\circ\text{C}$. The dynamic range is better than 75dB over a frequency range of 100MHz to 400MHz. The graph in fig 4 shows how the dynamic range is guaranteed over frequency.

The SL3522 consists of 6 Gain stages, 7 Detector stages, a limiting RF Output buffer and a Video Output amplifier. The power supply connections to each section are isolated from each other to aid stability.

The SL3522 consumes 1.1W of power when ALL parts of the circuit are powered up from a $\pm 5.0\text{V}$ power supply. As the circuit uses a differential architecture, the power consumption of the RF gain/detector stages and RF Output Buffer will be independent of RF input signal level. However, the Video Output (pin 13) is driven by a single ended emitter follower and so the power consumption of the Video amplifier will vary with RF input signal level between pins 27 and 28. (upto 10mA over 2V video output range with max video load of $200\Omega // 20\text{pF}$) The SL3522 has a high RF gain ($>50\text{dB}$) across a wide bandwidth ($>450\text{MHz}$) when the limiting RF Output Buffer is enabled. The limiting RF Output Buffer provides a balanced Limited Output level of nominally -1.0dBm on each RF Output connection (pin 9 and 10), for RF input signal levels on pins 27 and 28 in excess of -50dBm .

The limiting RF Output Buffer can be isolated from the other sections of the SL3522, by disconnecting the RF Output Buffer GND (pin 8) from 0V, and leave the pin floating. This feature aids stability in applications NOT requiring a Limited RF Output signal, and lowers the power consumption of the SL3522 to 0.95Watts, when the other sections are powered up from a $\pm 5.0\text{V}$ power supply.

Each of the Gain and Detector stages has approximately 12dB of gain, and a significant amount of on-chip RF decoupling (200pF per stage), also to aid stability. The Video amplifier provides a positive going output signal proportional to the log of the amplitude of an RF input applied between pins 27 and 28. The gain and the offset of the Video amplifier can be adjusted by 3 resistors; R_G , R_T , and R_O which are connected to Gain adjust (pin 19), Trim reference (pin 18) and Offset adjust (pin 17). With R_T set to $1.5\text{k}\Omega$, R_G can be set to any value between $1\text{k}\Omega$ and $2\text{k}\Omega$ and achieve a range in Video Slope of $\pm 20\%$, centred on 21mV/dB . Similarly, R_O can be set to any value between $1\text{k}\Omega$ and $2.2\text{k}\Omega$ and achieve an offset range of $\pm 0.5\text{V}$, which should allow the Video Offset to be trimmed to 0V if required.

The RF input pins (27 and 28) have a 50Ω terminating resistor connected between them on-chip. These are capacitively coupled to the I/P gain stage with 20pF on-chip capacitors. (Refer to APPLICATION NOTES section for information on how to connect an RF input signal to the device).

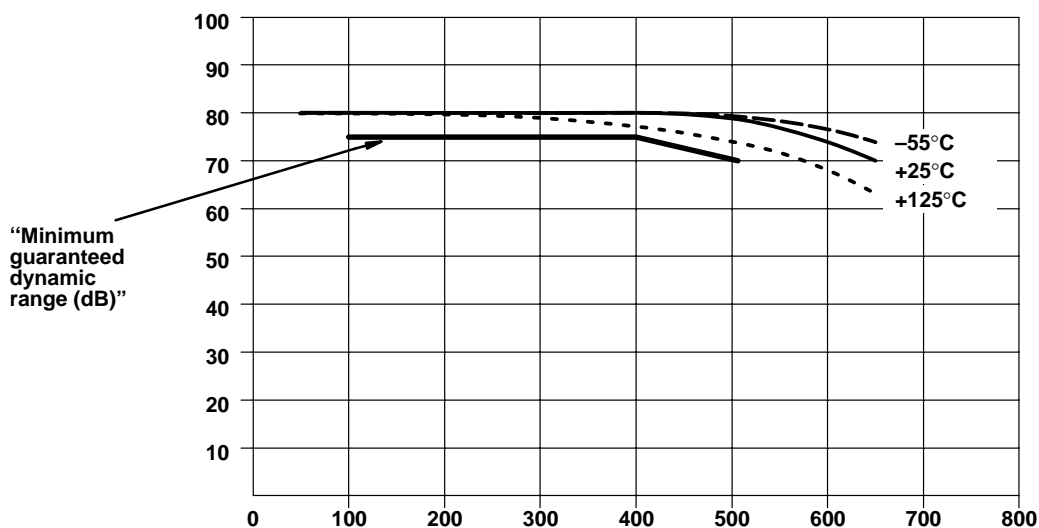


Fig.4 Plot showing guaranteed dynamic range v. frequency
(typical achievable dynamic range lines indicated across temperature)

APPLICATION NOTES

1) VIDEO-AMPLIFIER

The SL3522 uses a single ended Video amplifier to produce a trimmable Video transfer characteristic. Both the gain (Slope) and Offset of the amplifier can be externally adjusted.

a) Gain and Offset trimming (ref Applications circuits in figs 5 and 6)

The Gain and Offset control is achieved by adjusting R_G and R_O respectively. The control is dependent upon their difference from the Trim reference resistor, R_T . Adjustment of Gain has an effect on Offset, but adjustment of Offset does NOT affect the Gain. Therefore the Gain should be optimised first. The Offset should only be adjusted once the Gain has been set.

Fig 7 shows the variation of Video Offset with value of R_O , for a fixed value of R_T and $R_G = 1k5\Omega$.

Fig 8 shows the variation of Video Slope with value of R_G , for a fixed value of R_T and $R_O = 1k5\Omega$.

The Video amplifier incorporates temperature compensation for Video gain (Slope). To ensure temperature stability for Video gain (Slope) over the operating temperature range, it is recommended that the resistors with identical temperature coefficients of resistance are used for R_T and R_G .

The Video amplifier does NOT incorporate temperature compensation for Video Offset. Although it is recommended that a resistor with identical temperature coefficient of resistance to R_T be used for R_O , it may be necessary to use an additional external temperature compensating network.

b) Video performance

The Video-amplifier has a critically damped rise time of 16ns (10% - 90%). In order to achieve this transient performance, it is important to ensure that:-

i) the resistor connected to Trim reference (pin 18), has a nominal resistance of 1.5k Ω , with a parasitic capacitance LESS than 5pF.

ii) the load applied to the Video Output (pin 13) does NOT exceed 200 Ω resistance in parallel with 20pF.

Also, the following decoupling should be incorporated:-

i) The Video Output V_{CC} (pin 14) should be decoupled with a 10nF capacitor to the RETURN line from the video load, connected to Video GND (pin 16), avoiding any common impedance path.

ii) The Video Output Vee (pin 12) should be decoupled with a 10nF capacitor DIRECTLY to Video-Output V_{CC} (pin 14).

2) SL3522 AS A LOG AMPLIFIER

with RF output buffer disabled (pin 8 floating)

If the SL3522 is to be used as a Logarithmic successive detection amplifier only, with no requirement for a limited RF Output, the RF input (pins 27 and 28) can be driven EITHER differentially or single ended from a 50 Ω source. If being used with a single ended input, the SIGNAL should be applied to pin 27 and the RETURN should be connected to pin 28, as shown in the Application circuit diagram in Fig 5.

The SL3522 is VERY stable when used in this way. Although not a crucial requirement, it is recommended that the device should be mounted using a ground plane.

3) SL3522 AS A LOG/LIMITING AMPLIFIER

- with RF Output-Buffer ENABLED (pin 8 connected to GND)

If the SL3522 is to be used as a Limiting or Log/limiting amplifier with a requirement for a Limited RF Output signal, care is required in the layout of components and connections around the device to ensure stability. The following precautions should be observed (refer to Application circuit diagram in Fig. 6):-

a) The device should be mounted on a ground plane, ensuring that the impedance between the ground plane and ALL the GND pins is kept as low as possible. If a multilayer PCB is used where the ground plane is connected to the GND pins using through-plated holes (vias), it is essential to ensure that the vias have a very low impedance. ALL supply decoupling capacitors should be RF chip capacitors whose leads should be kept as short as possible.

b) The RF V_{EE} connections (pins 3,5,7,11,20,22,24,26) should be connected to a low impedance copper plane. A two layer PCB should help to achieve this.

c) The RF input (pins 27 and 28) should be driven with a balanced source impedance. One way of achieving this is to use an **isolating** BALUN transformer (50 Ω UNBALANCED \rightarrow 50 Ω BALANCED) connected between the signal source and the RF input pins. (e.g. Mini circuits TT1-6, TO-75). The device stability is VERY sensitive to an imbalance of the differential source impedance at pins 27 and 28. Use of a transmission line BALUN though, is NOT recommended.

d) The RF Output connections (pins 9 and 10) should each be loaded with matched impedances ideally 50 Ω transmission lines. The RF Output lines leading away from the device should be balanced. Driving highly reactive SWR loads is NOT recommended as these can encourage device instability, as can an imbalance of the differential load impedance at pins 9 and 10.

e) The RF Output connections (pins 9 and 10) are DC coupled, and ideally the output pins should be capacitively coupled to their loads using 1nF capacitors. However the RF Outputs can drive a DC load to GND and a DC offset of approx. 400mV will exist on each RF Output pin. IT WILL NOT BE POSSIBLE TO DISABLE THE RF OUTPUT BUFFER UNDER THESE CONDITIONS.

f) The RF output (pins 9 and 10) has a tendency to limit on self noise, particularly at low ambient temperatures (-55 $^{\circ}$ C), when the RF output buffer is enabled.

NOTE that this will effect the limiting range as the gain of the RF output buffer will reduce as the amount of noise limiting increases.

If required the limited RF Output can be attenuated using an attenuation network as shown in fig. 9. Under these conditions the effective RF Output currents will be reduced, allowing the device to operate with a greater margin of stability. It may be possible to run the device without a BALUN transformer on the RF input if the total output impedance on the RF Output $\gg 50\Omega$, and the attenuation components are mounted as close as possible to the RF Output connections (pins 9 and 10). The RF input connection could then be configured as in Fig 5.

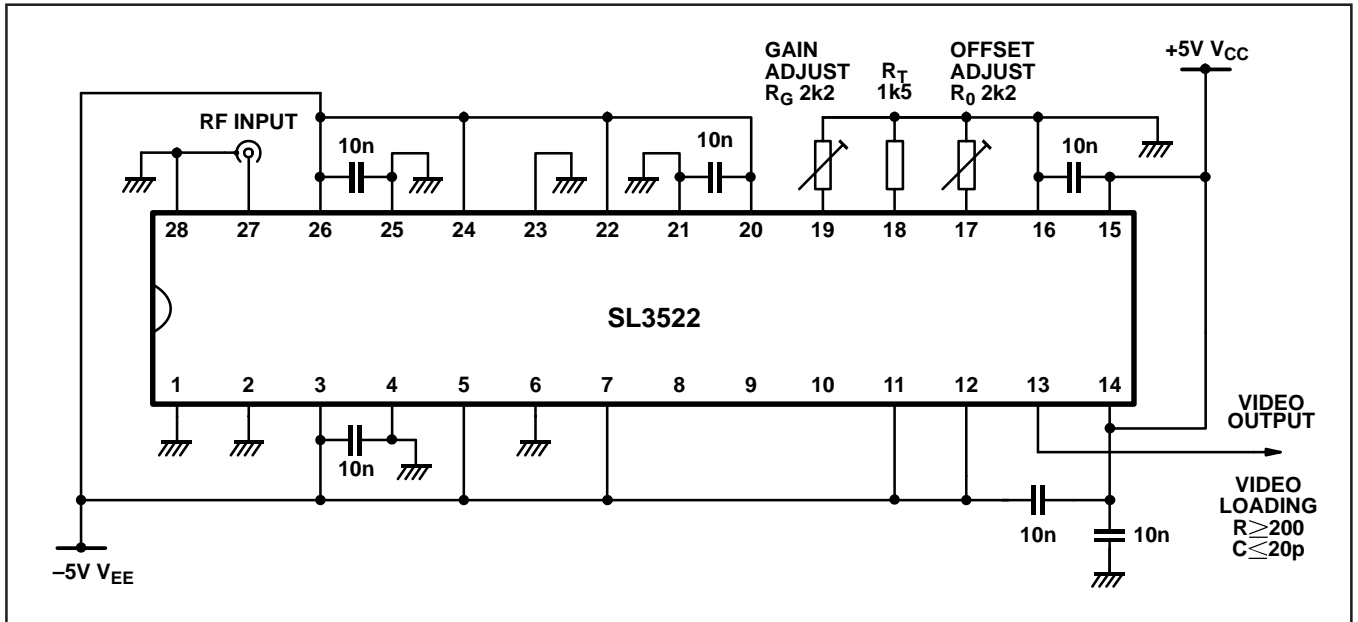


Fig.5 Application circuit successive detection logarithmic function only

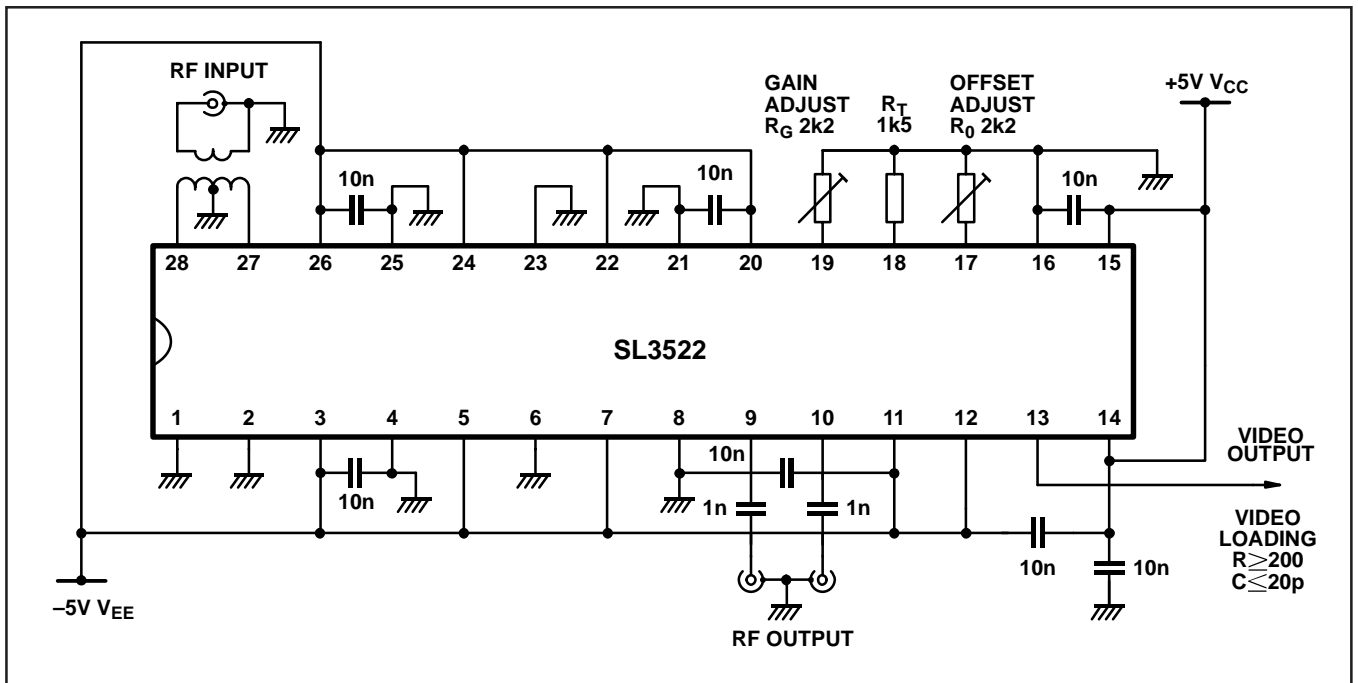


Fig.6 Application circuit - Log / Limiting function

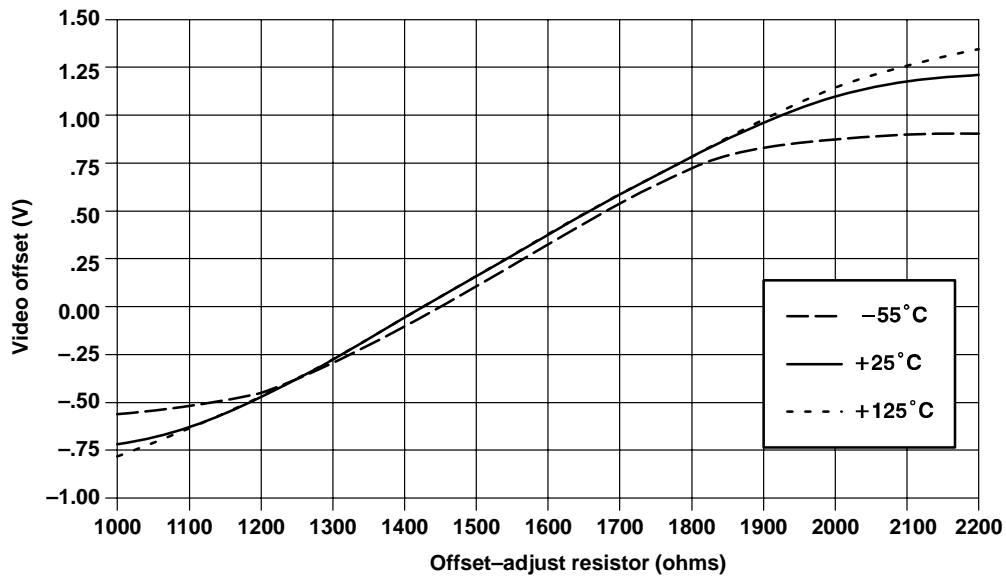


Fig.7 Video offset v. offset-adjust resistor (pin17 to gnd) across temperature

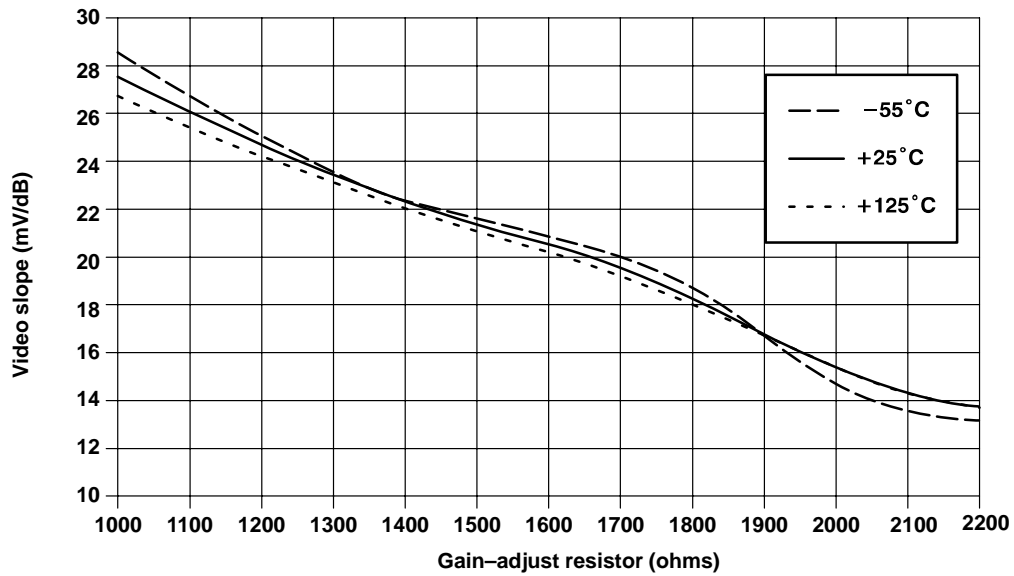


Fig.8 Video slope v. gain-adjust resistor (pin19 to gnd) across temperature

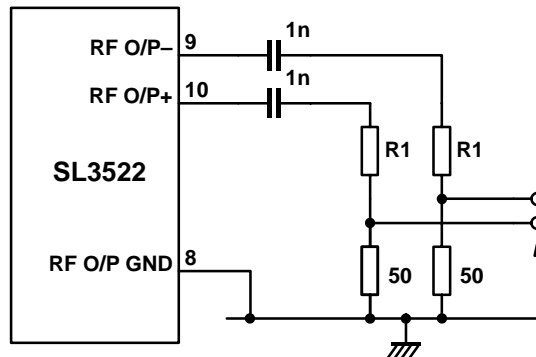


Fig.9 Network for attenuating limited RF output

A PRACTICAL APPLICATION FOR THE SL3522 AS A LOG/LIMITING AMPLIFIER

The SL3522, with the RF Output-Buffer ENABLED, has a large limited RF Output level (0dBm on each of two RF Output pins (9 and 10)) and a wide RF bandwidth (450MHz) in a small 28 pin Miniature Ceramic S.O package. As a result, there is a tendency for the device to become unstable unless care is used in the application.

The PCB layout for a "SL3522 DEMONSTRATION BOARD" in Fig. 11 has proved reliably stable. The PCB is a double layer Fibre epoxy board which uses SMDs where possible. A circuit diagram for the Demonstration PCB appears in Fig. 10.

The following points should be noted when this application is realised practically:-

- 1) A wire needs to connect the two pads connected to pins 14 and 15 of the SL3522, to allow +5V to appear at both pins.
- 2) ALL the GND connections to the SL3522 are made through the PCB to a Ground plane on the bottom side. It is important to ensure that the impedance of each of these connections is kept to an absolute minimum to prevent instability. If these connections are achieved using through plated holes, it is recommended that they are filled with solder to lower their impedance.
- 3) The PCB is configured to accept SMA, SMB or SMC connectors for the RF input, RF Output and Video Output connections. These can be changed if necessary to an alternative type, but it is vital to ensure that the ground plane is solidly connected to the Guard Ring which surrounds the RF Output tracks.

4) The PCB is configured to accept a small surface mounting DC isolating BALUN transformer (e.g VANGUARD VE43666, available from Vanguard Electronics Company Inc, 1480 West 178th St. GARDENA, C.A. 90248, U.S.A. Tel:- U.S.A. (213) 323 – 4100) to couple a signal into the RF input connections (pins 27 and 28). It is NOT recommended to attempt operating the SL3522 with the RF Output Buffer enabled, WITHOUT using an input BALUN, although it may be possible, provided the input source impedance to both pins 27 and 28 remains balanced. The centre tap of the secondary winding of the transformer should be soldered to the small ground plane on the upper side of the PCB.

5) The RF Output connection to the PCB is from pin 9 of the SL3522 only, with pin 10 being terminated on the PCB using a 51Ω resistor. It is important to ensure that both pin 9 and 10 are terminated with equal impedances.

6) The RF Output Buffer can be enabled by soldering a link (LK) between pin 8 of the SL3522 and the adjacent guard track around the RF Output lines. Similarly, the buffer can be disabled by removing the same link. When the buffer is disabled, the following components can be omitted:-

- 1nF capacitors (C1, C2)
- 10nF capacitor (C8)
- 51Ω resistor (R_{FO})

7) The Slope (gain) and Offset of the Video Output can be adjusted using two 1kΩ trimmers, provision for which is included in the PCB layout.

The plots in Fig. 12 to fig. 23 are typical of the performance of SL3522 devices used with the PCB layout detailed in Fig.11.

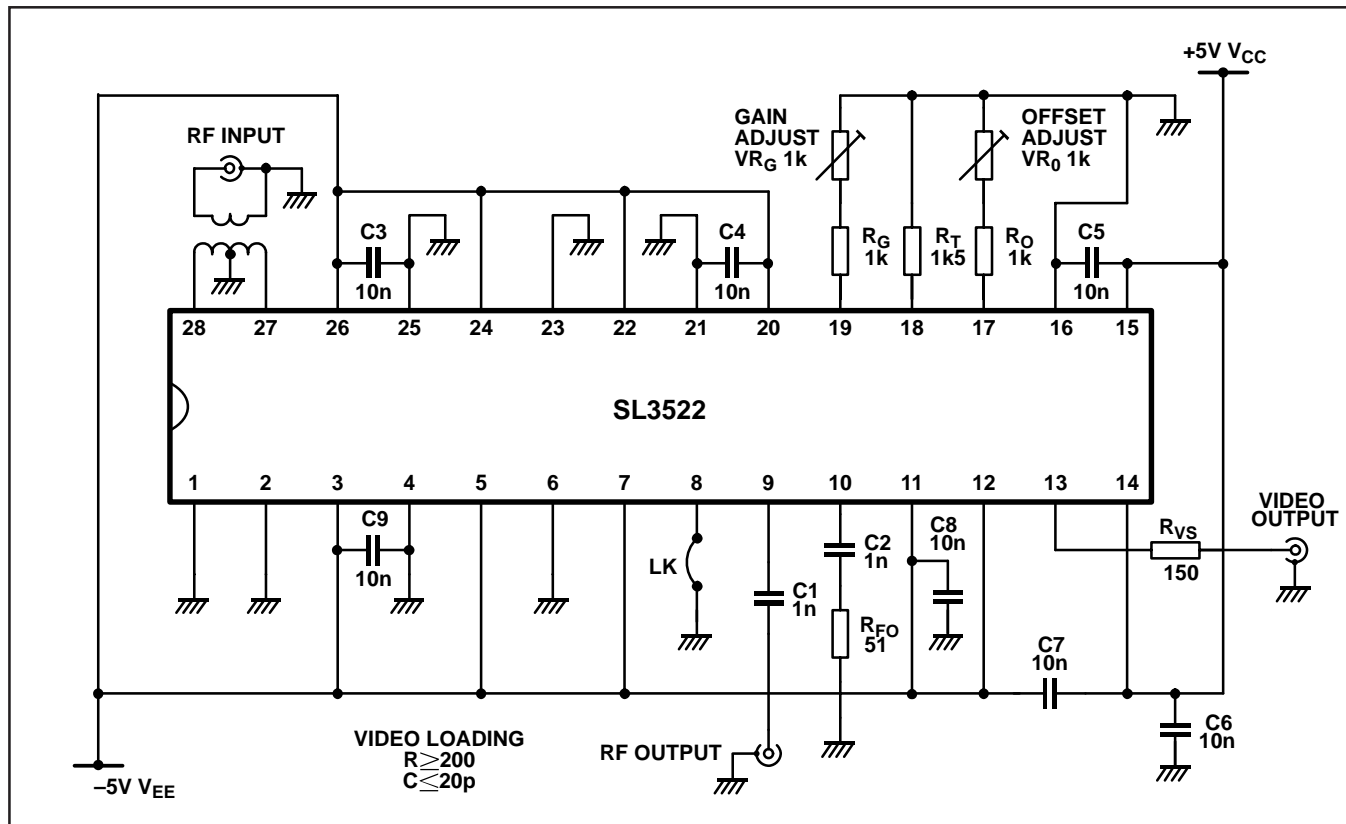


Fig.10 SL3522 demonstration board circuit diagram

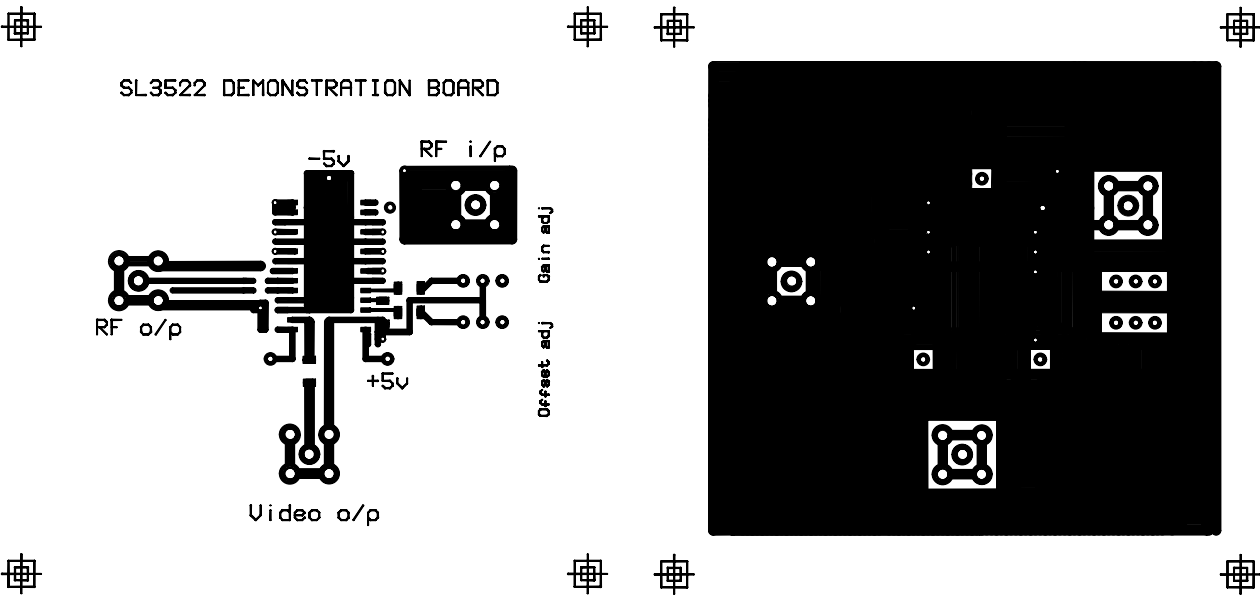
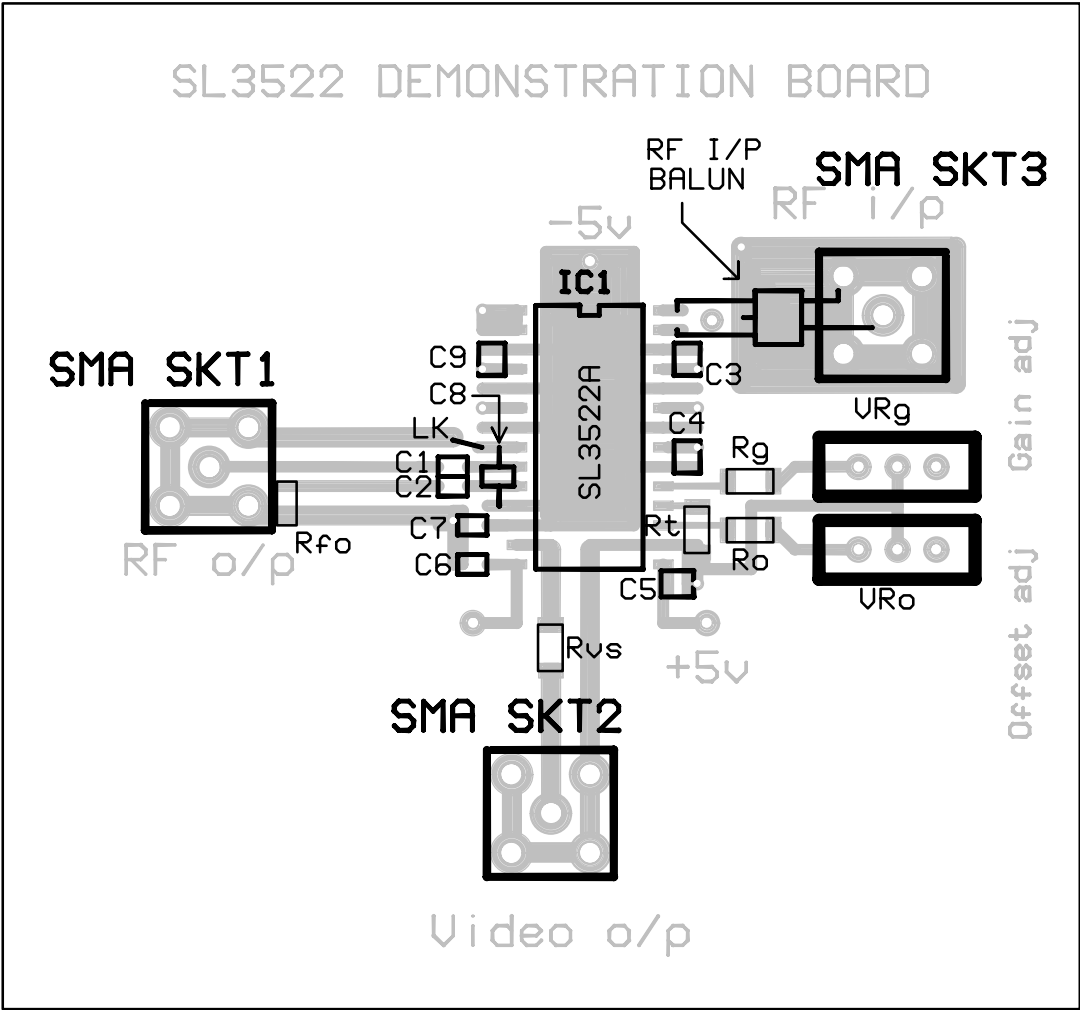


Fig.11 Demonstartion Circuit PCB showing components positions (2x full size) with top and bottom copper masks (full size)

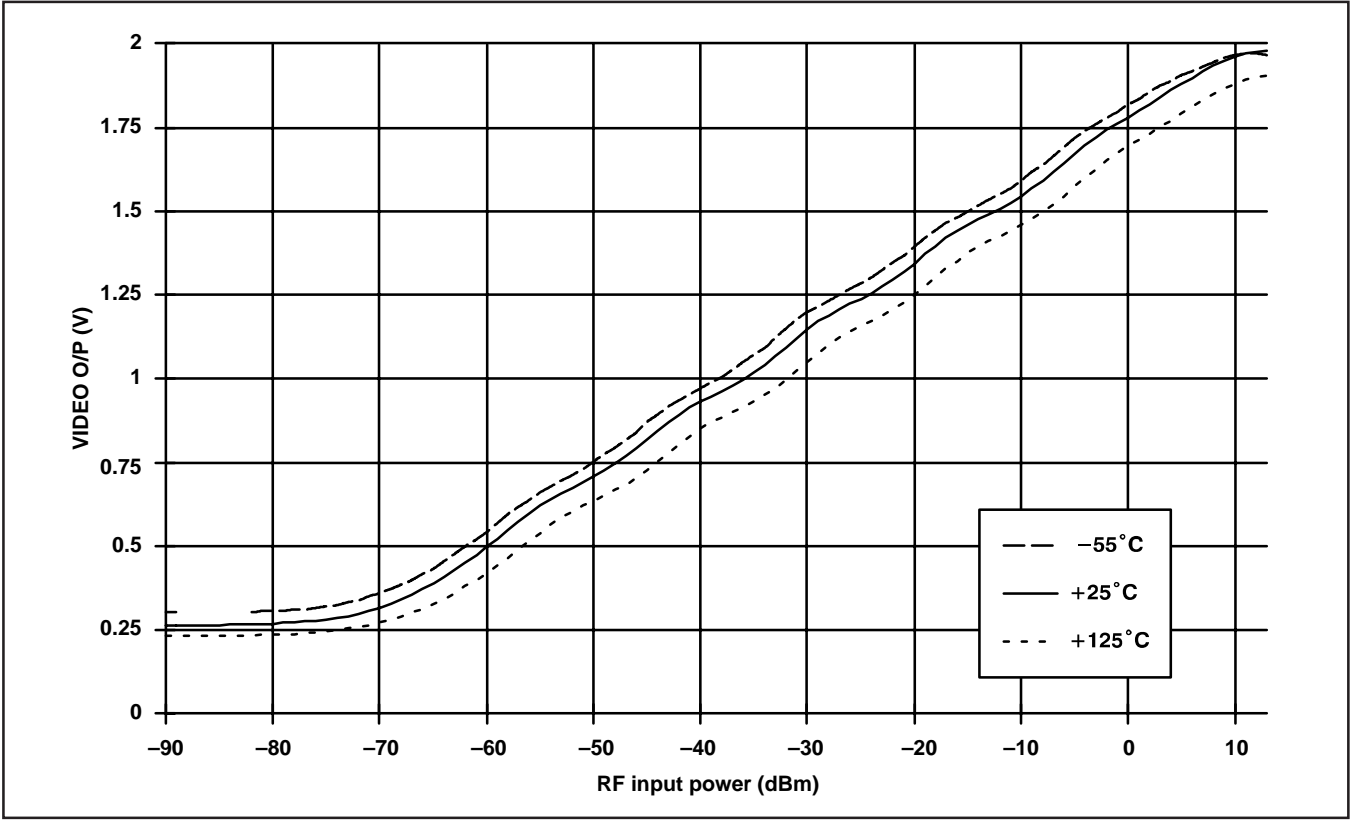


Fig.12 Video O/P vs CW input level at 325MHz across temperature ($V_{CC} = +5.0V$, $V_{EE} = -5.0V$)

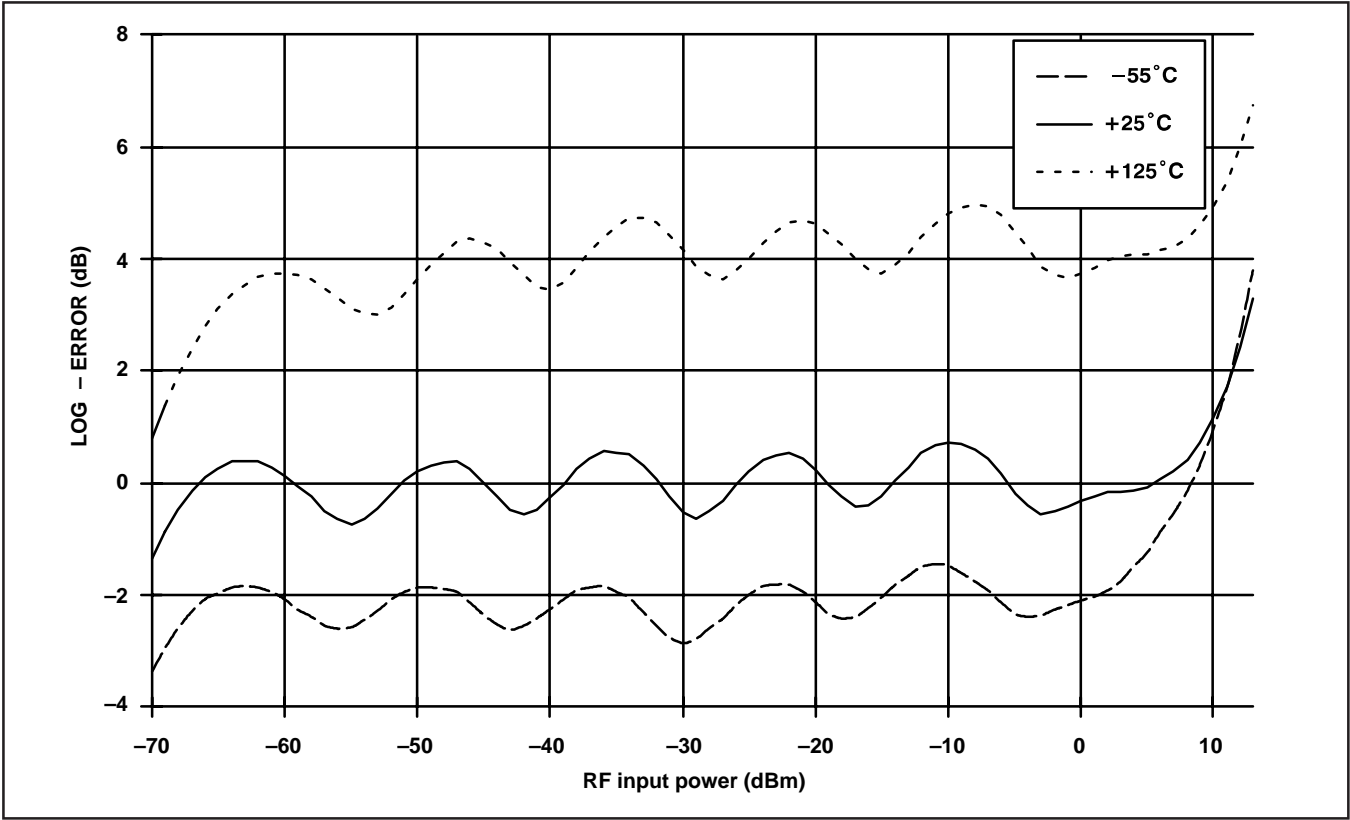


Fig.13 Video O/P log-error, (referenced to single straight line measured at 325MHz, +25°C, 5.0V PSUs) across temperature

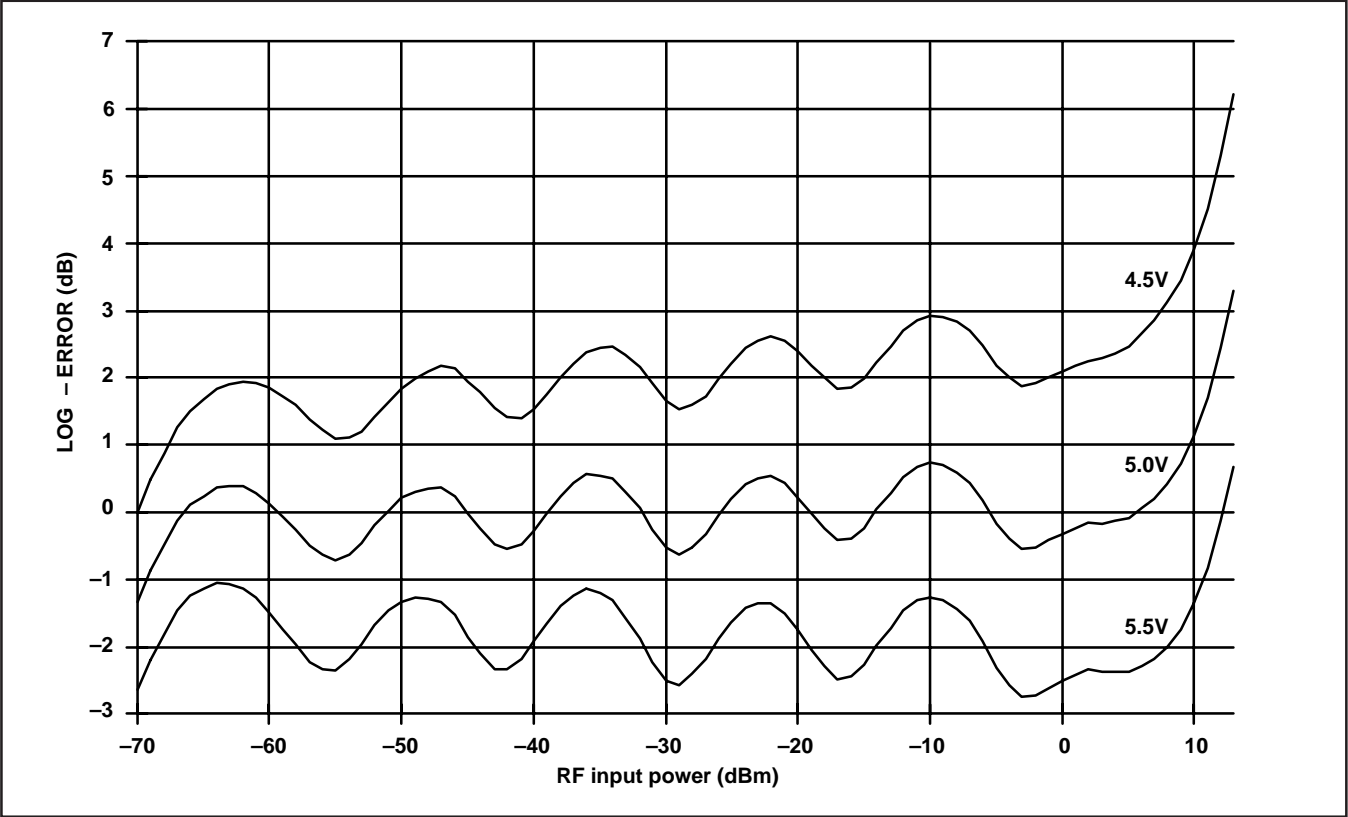


Fig.14 Video log error, (referenced to single straight line measured at 325MHz, 25°C, 5.0V PSUs), across supply voltage

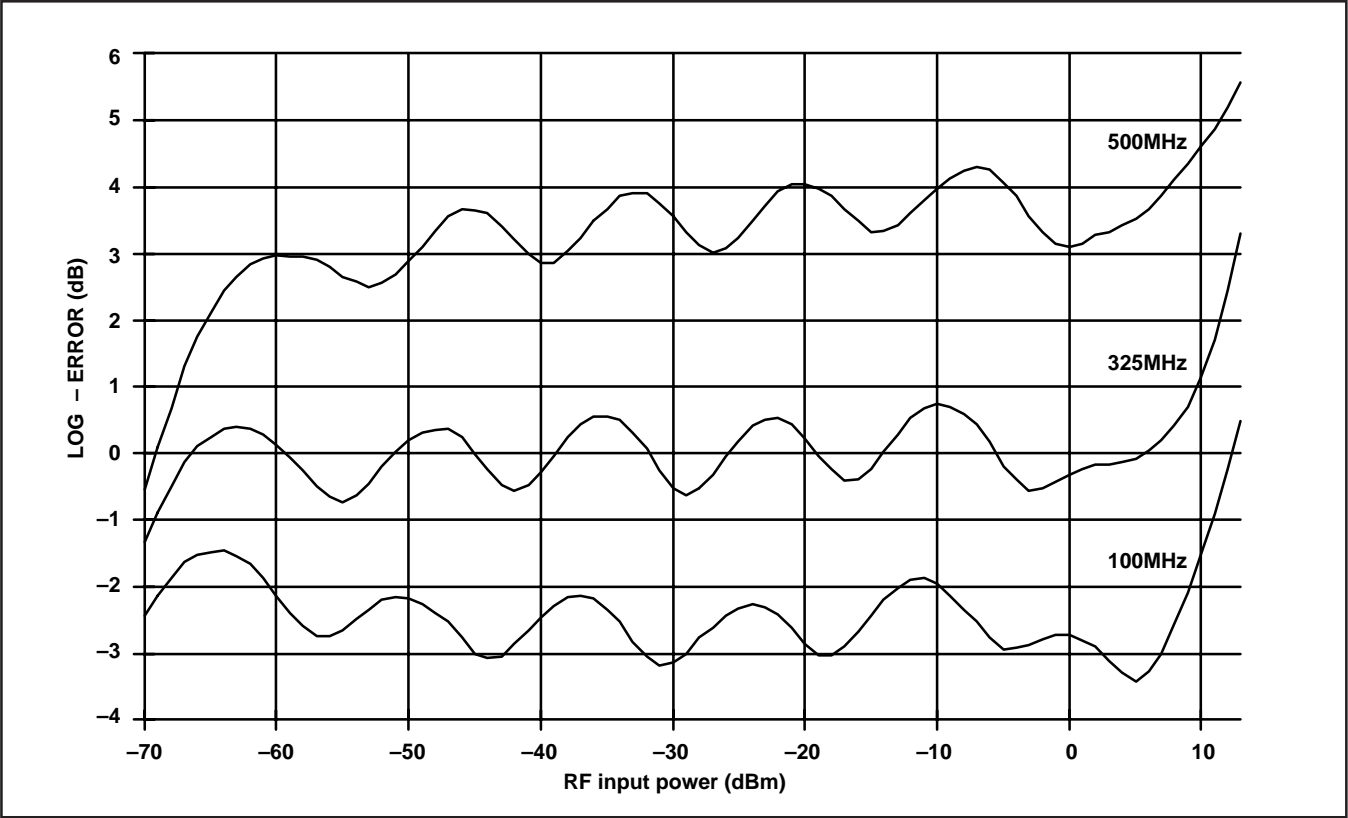


Fig.15 Video log error, (referenced to single straight line measured at 325MHz, 25°C,

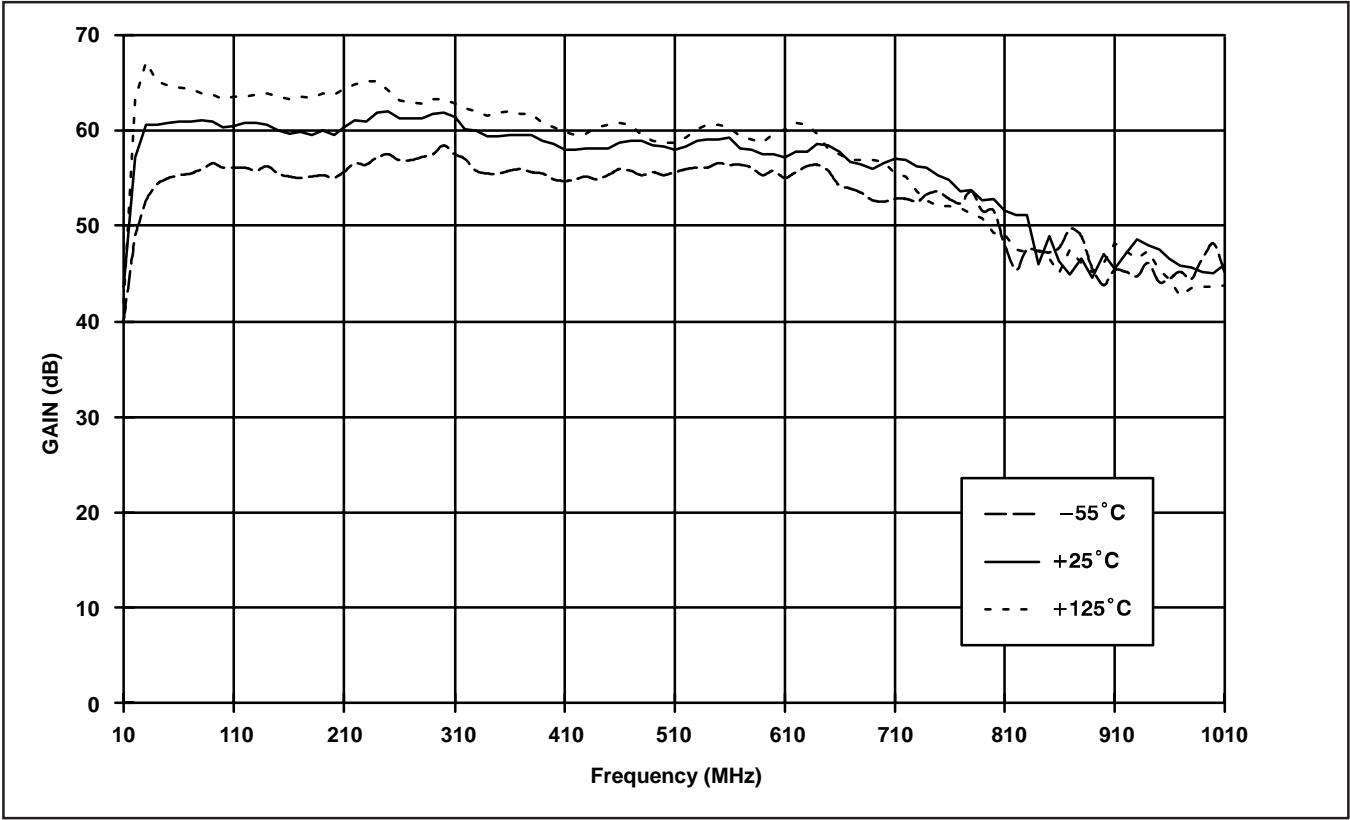


Fig.16 Linear gain (-70dBm I/P)

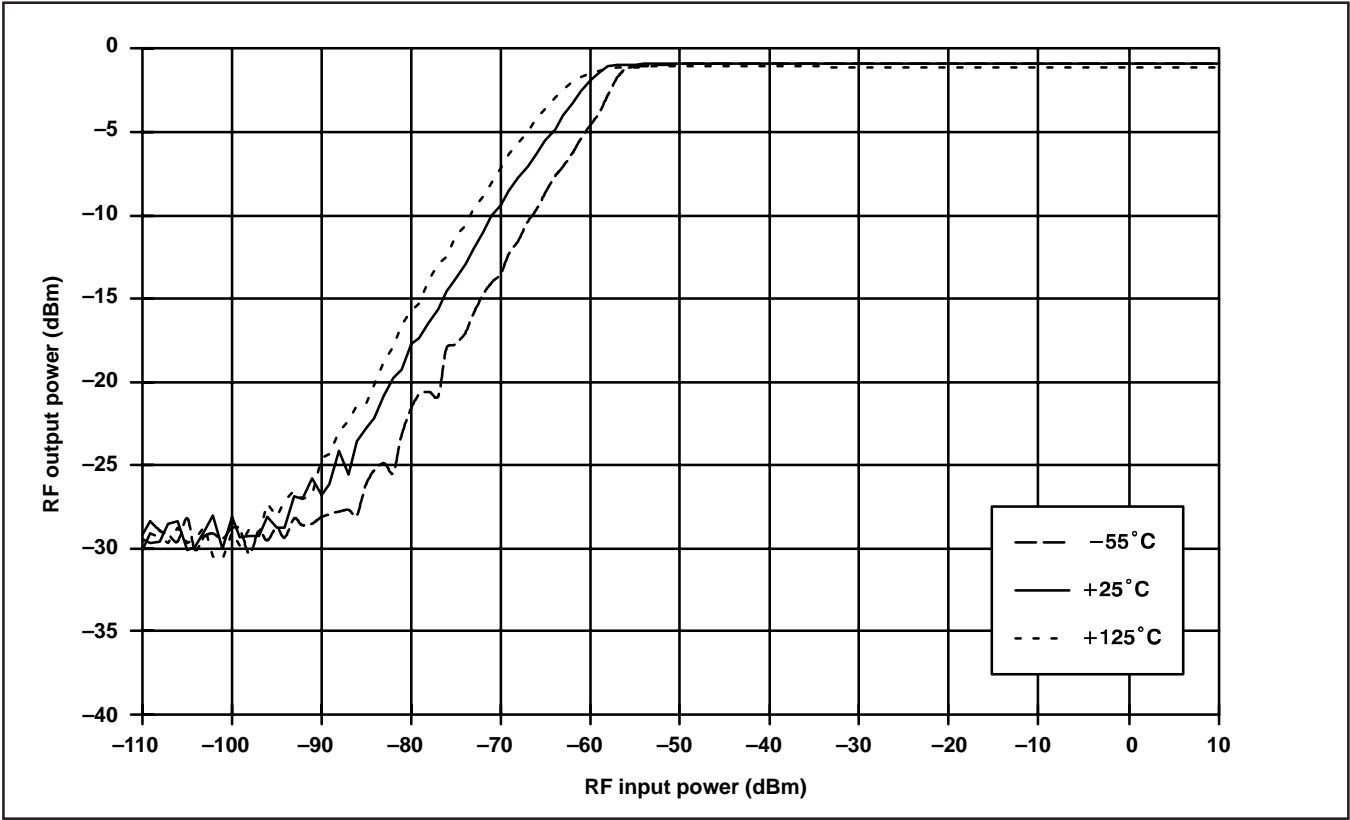


Fig.17 RF input → output limiting transfer characteristic at Frequency = 100MHz

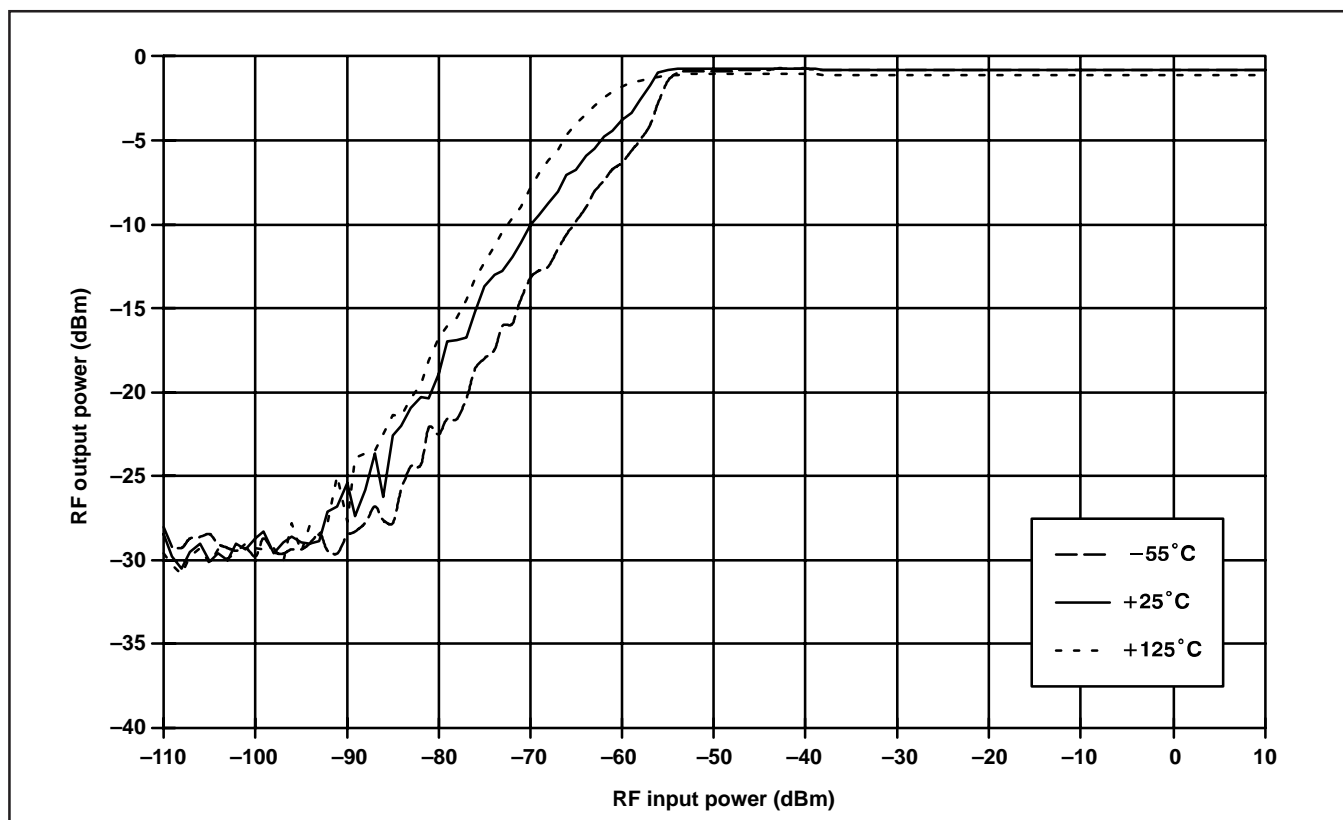


Fig.18 RF input → output limiting transfer characteristic at Frequency = 325MHz

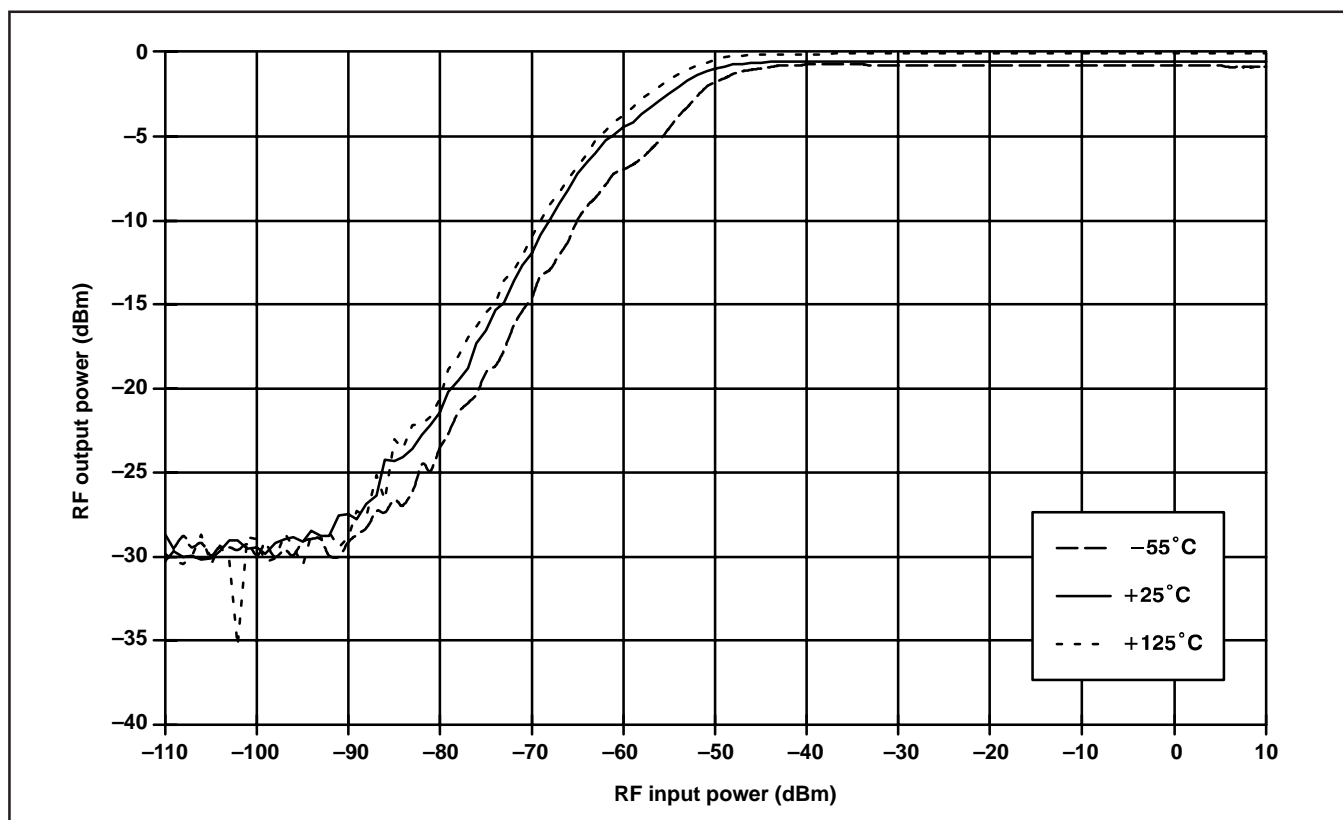


Fig.19 RF input → output limiting transfer characteristic at Frequency = 500MHz

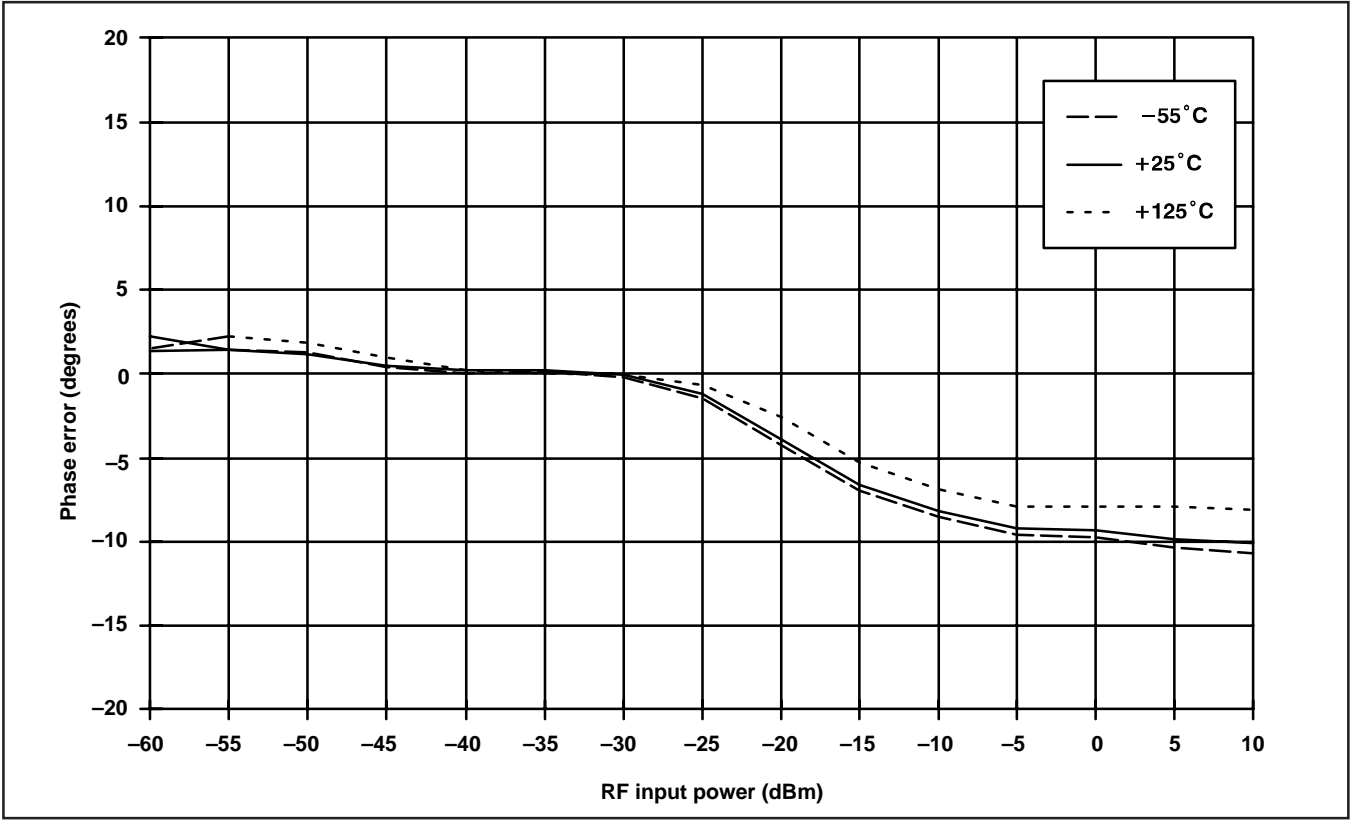


Fig.20 Limiting phase (100MHz) normalised at -30dBm

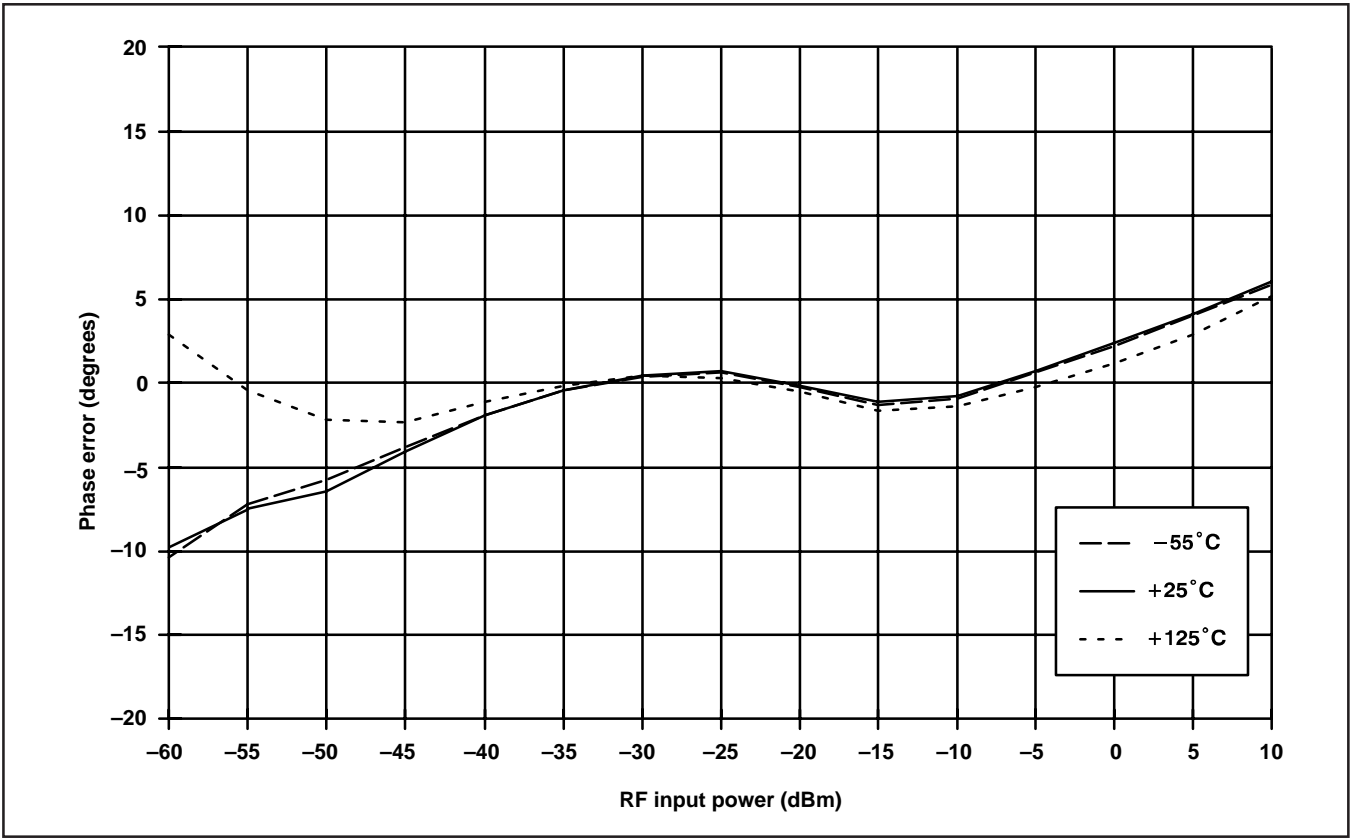


Fig.21 Limiting phase (300MHz) normalised at -30dBm

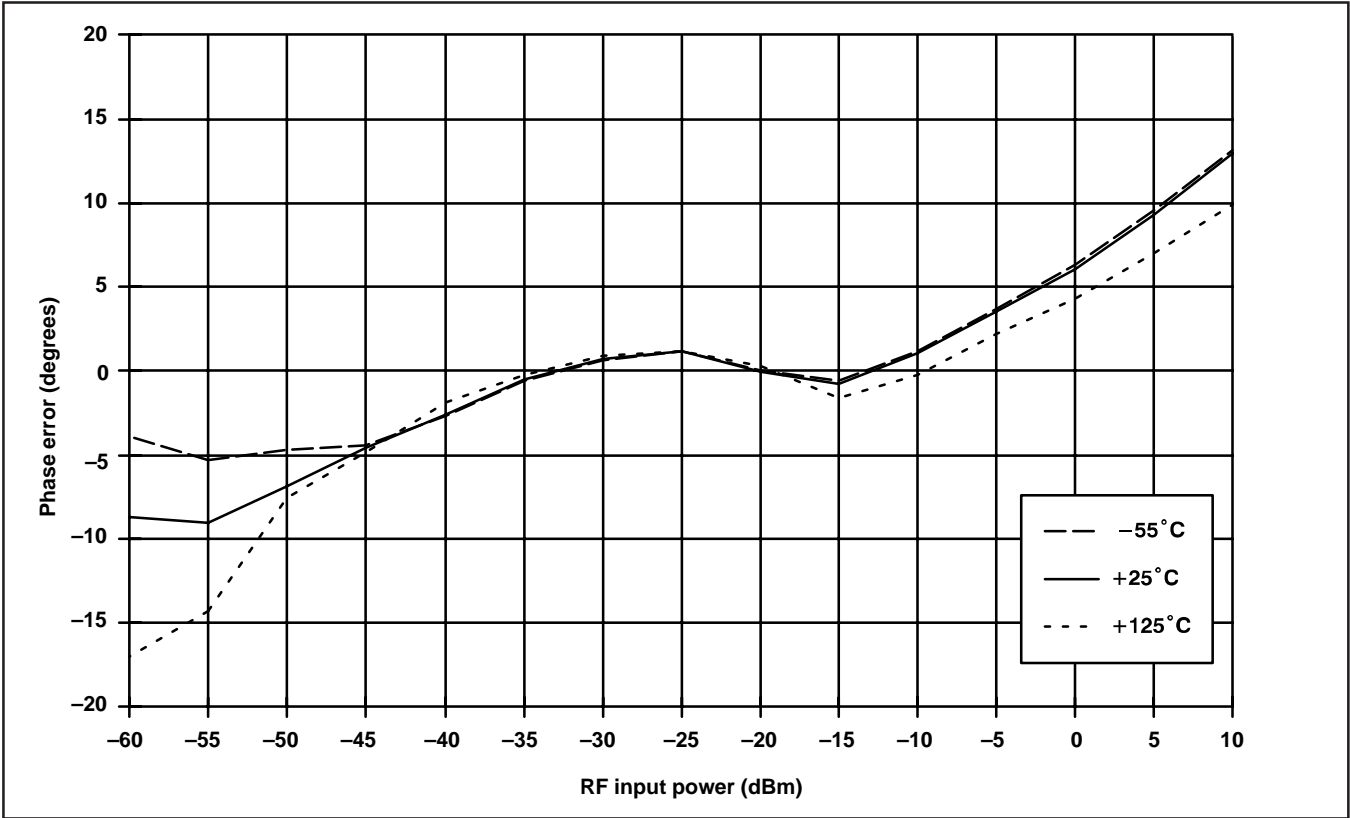


Fig.22 Limiting phase (500MHz) normalised at -30dBm

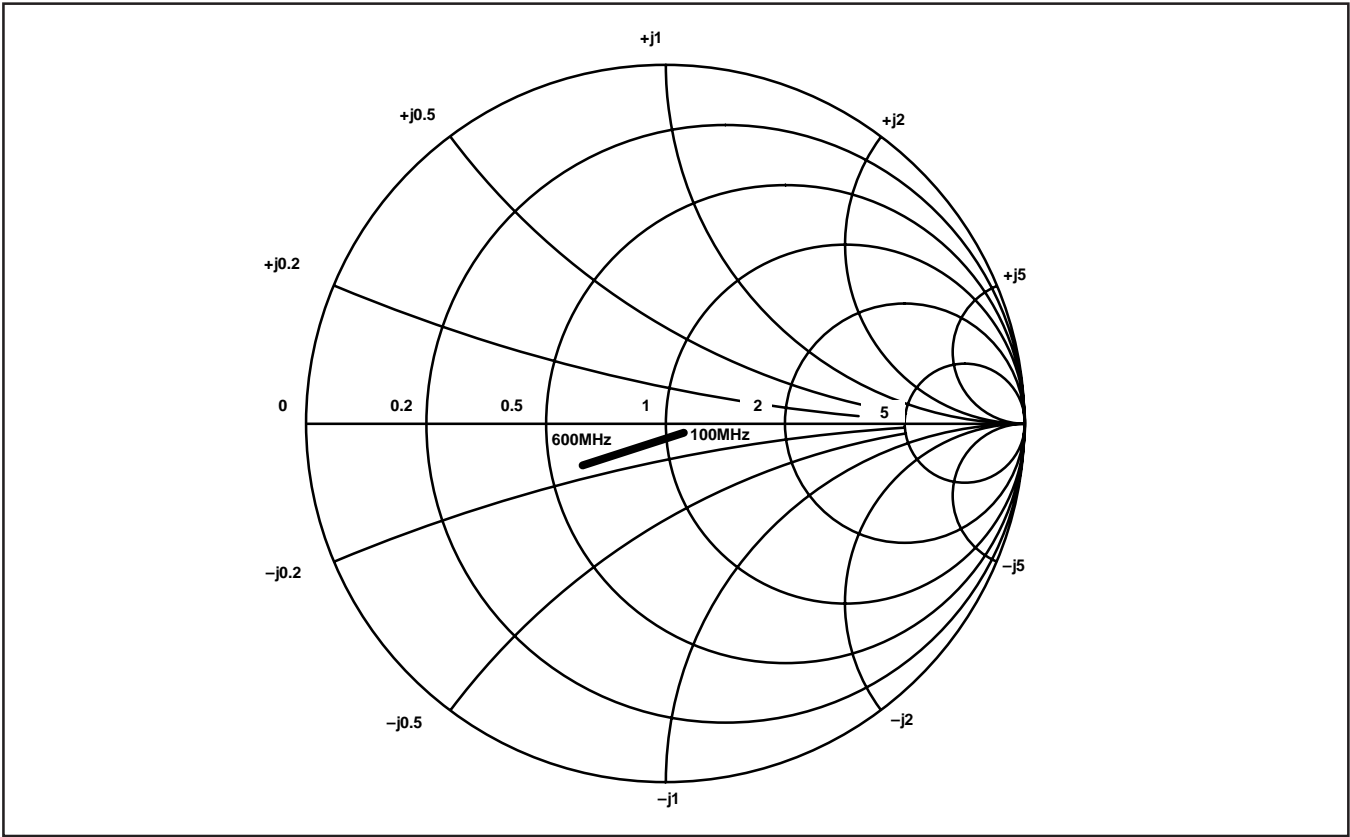


Fig.23 Typical input impedance normalised to 50Ω - 20dBm I/P level

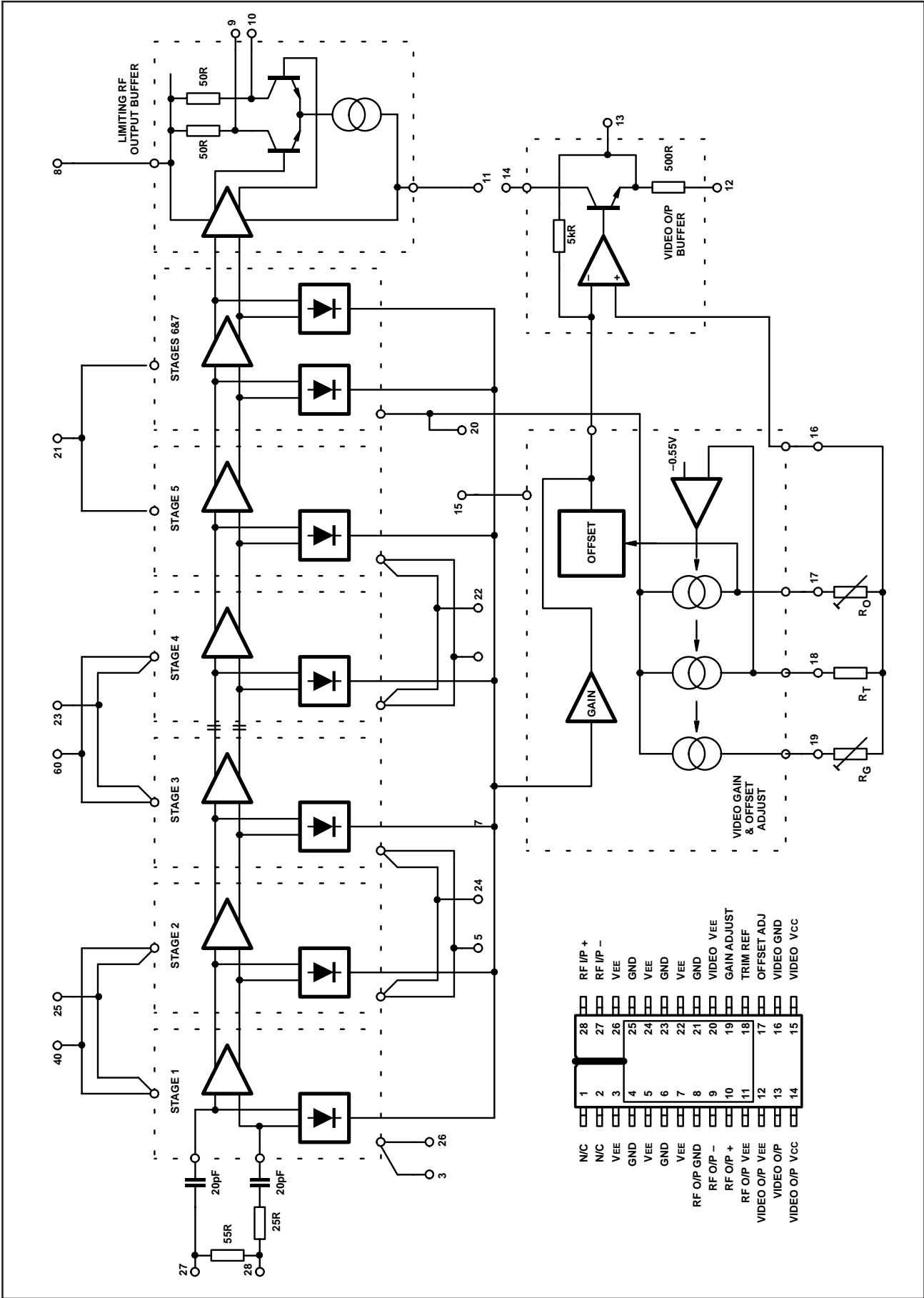
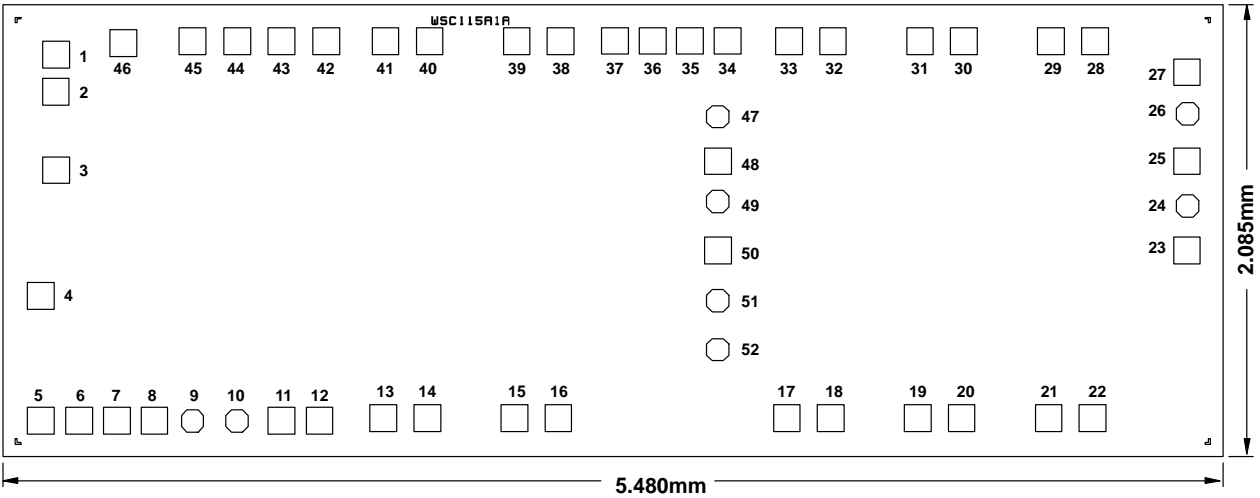


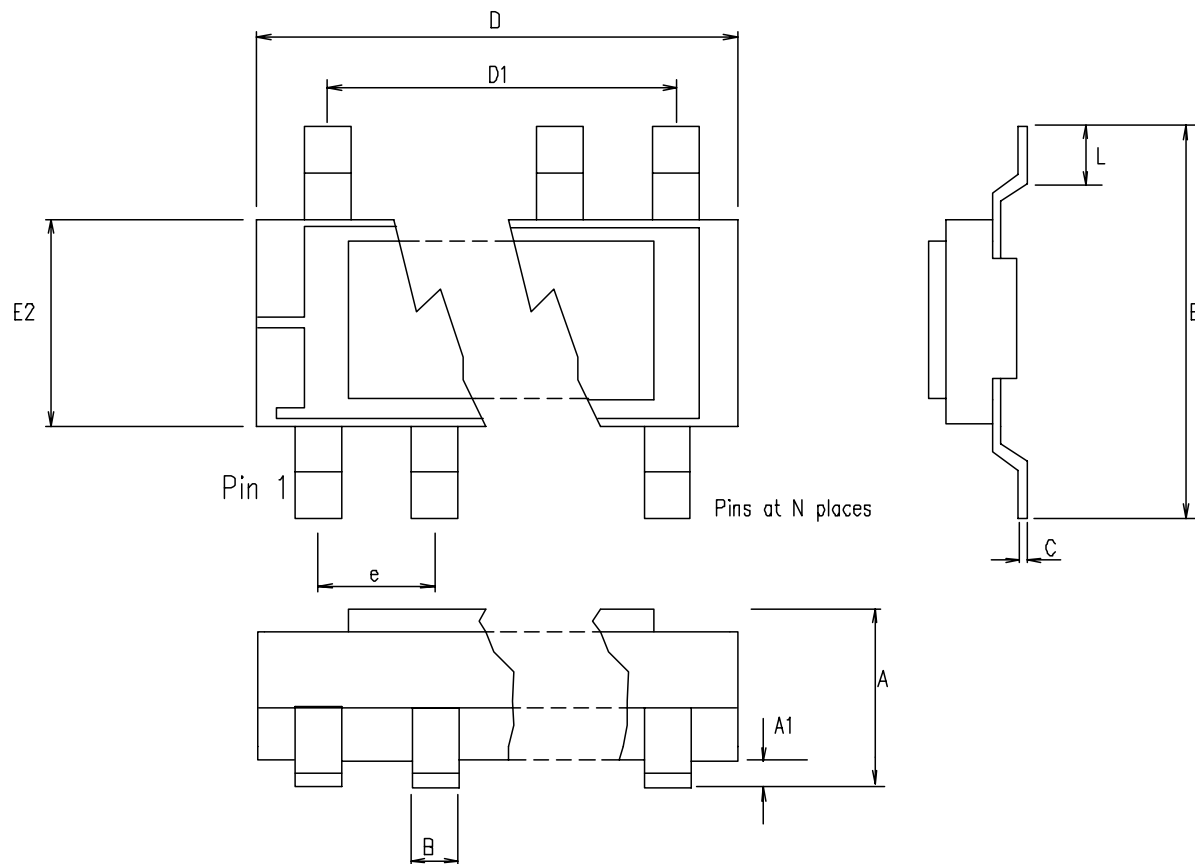
Fig.24 SL3522 Schematic diagram



TERMINALS ((X) DENOTES MC PACKAGE PIN NUMBER)					
1	Video O/P (13)	14	V _{EE} 5A (22)	27	Test point
2	Video O/P V _{CC} (14)	15	V _{EE} 4A (22)	28	V _{EE} 1B (3)
3	Gain V _{CC} (15)	16	GND 4B (23)	29	GND 1B (4)
4	Video GND (16)	17	GND 3A (23)	30	GND 2B (4)
5	Offset ADJ (17)	18	V _{EE} 3A (24)	31	V _{EE} 2A (5)
6	Trim REF (18)	19	V _{EE} 2A (24)	32	V _{EE} 3A (5)
7	Gain ADJ (19)	20	GND 2A (25)	33	GND 3B (6)
8	Gain V _{EE} (20)	21	GND 1A (25)	34	Test point
9	Test point	22	V _{EE} 1A (26)	35	Test point
10	Test point	23	Test point	36	Test point
11	V _{EE} 6A (20)	24	RF I/P signal (27)	37	Test point
12	GND 6A (21)	25	Test point	38	GND 4B (6)
13	GND 5A (21)	26	RF I/P return (28)	39	V _{EE} 4B (7)
				40	V _{EE} 5B (7)
				41	RF BUF O/P GND (8)
				42	RF BUF O/P GND (8)
				43	RF O/P – (9)
				44	RF O/P + (10)
				45	RF BUF O/P V _{EE} (11)
				46	Video O/P V _{EE} (12)
				47	Test point
				48	Test point
				49	Test point
				50	Test point
				51	Test point
				52	Test point

- NOTES
1. All pads with square cross-section = 120µm × 120µm
 2. All pads with octagonal cross-section = 100µm × 100µm
 3. Chip is passivated with polyimide

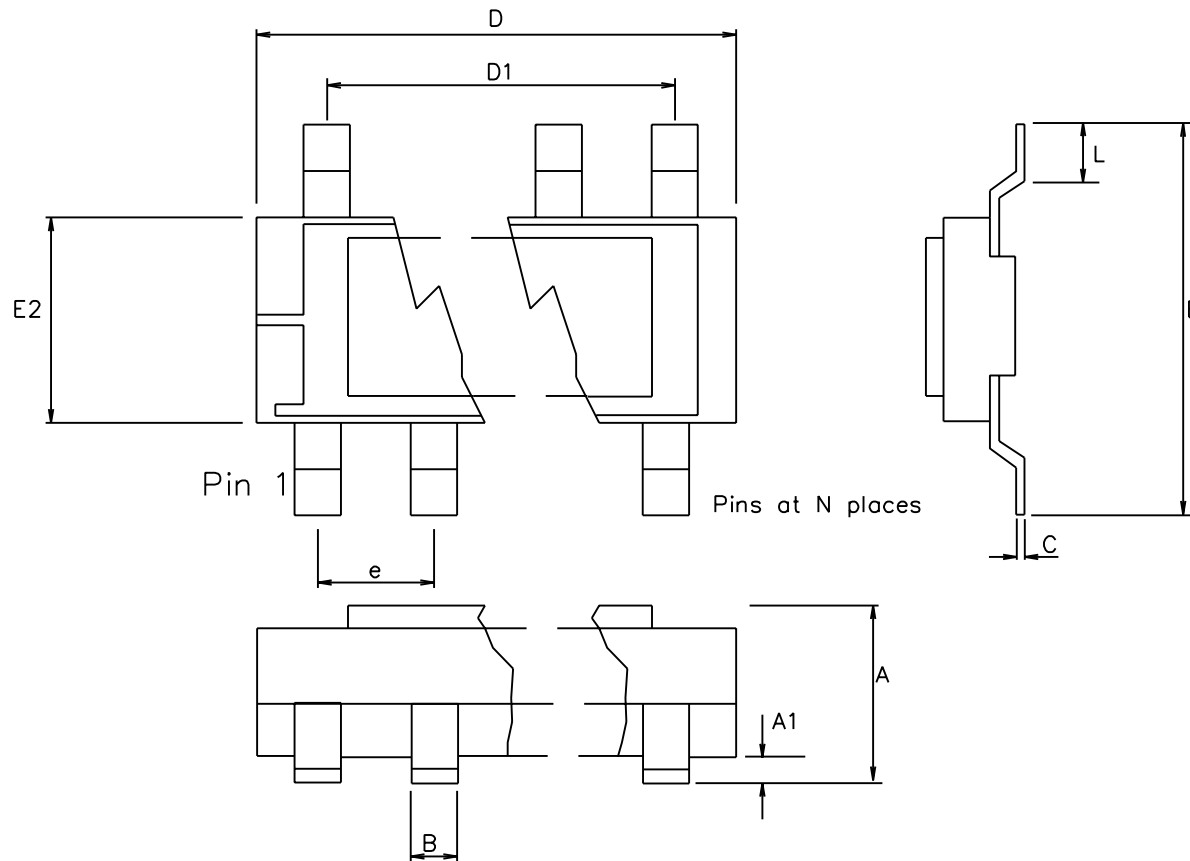
Fig.25 SL3522 pad map for bare IC dice



Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.20		2.75		0.087		0.108
A1			0.30				0.012
B	0.37		0.47		0.015		0.019
C	0.17		0.23		0.007		0.009
D	17.70		18.10		0.697		0.713
D1	16.36		16.66		0.644		0.656
E	10.00		10.67		0.394		0.420
E2	7.30		7.60		0.287		0.299
e	1.27 BSC.				0.050 BSC.		
L	0.75		1.08		0.030		0.043
	Pin features						
N	28						
ND	14						
NE	0						
NOTE	RECTANGULAR						

This drawing supersedes 418/ED/51300/005 issue 1 (Swindon)

						ORIGINATING SITE: SWINDON	
ISSUE	1	2				Title:	Outline drawing for 28 Lead S.O. (MC)
ACN	201634	201849				Drawing Number	GPD00267
DATE	12.NOV.96	11.FEB.97					
APPROVED							



Symbol	Altern. Dimensions in millimetres			Control Dimensions in inches		
	MIN	Nominal	MAX	MIN	Nominal	MAX
A	2.20		2.75	0.087		0.108
A1			0.30			0.012
B	0.37		0.47	0.015		0.019
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	Pin features					
N	28					
ND	14					
NE	0					
NOTE	RECTANGULAR					

This drawing supersedes 418/ED/51300/005 issue 1 (Swindon)

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ISSUE	1	2	3		Previous package codes	Package Outline for 28 lead SOIC (ceramic) (0.150" Body Width)
ACN	201634	201849	212449		MC	
DATE	12Nov96	11Feb97	26Mar02			
APPRD.						GPD00267





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