64M X 72 Bits (512MB) 144-Pin SDRAM SO-DIMM with ECC (PC133)

FEATURES

- PC133 Compliant (t_{CYC}=7.5ns@CL=3) (see *Ordering Information* for options)
- Burst Mode Operation
- Auto and self refresh capability (8192 cycles/64ms refresh)
- LVTTL compatible inputs and outputs
- +3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (access from column address)
  - Burst Length (1, 2, 4, 8, and Full Page)
  - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with 256 Byte EEPROM
- ECC

GENERAL DESCRIPTION

The SimpleTech SL72G8M64M8H-A75AV is a 64M x 72 bits Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of nine 16M x 8 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP II monolithic packages mounted on a 144-pin glass epoxy substrate.

A serial EEPROM using the two pin I^2C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.1µF are mounted. Damping resistors are mounted for the data lines. A PLL supplies clocks to the SDRAMs from one clock input.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V.

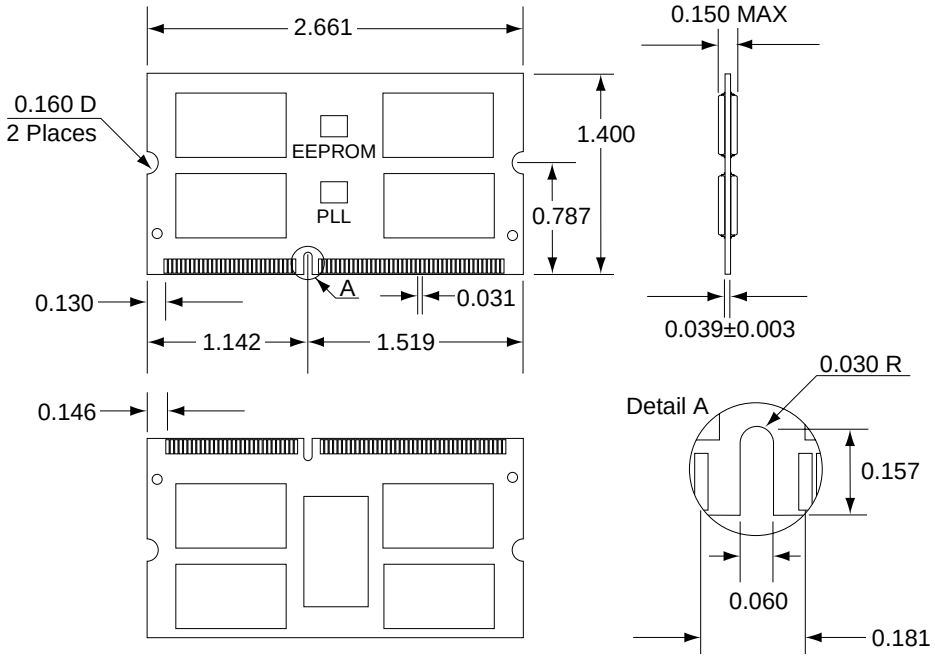
See *Ordering Information* for PC133 performance options.

ORDERING INFORMATION

SimpleTech Manuf. Part Number	PC133 133MHz Parameters			
	CL	t_{RCD}	t_{RP}	t_{RC}
SL72G8M64M8H-A75AV	3clks	20ns	20ns	67.5ns

PACKAGE DIMENSIONS

Units are in inches. Tolerances are ±0.005 unless otherwise specified.



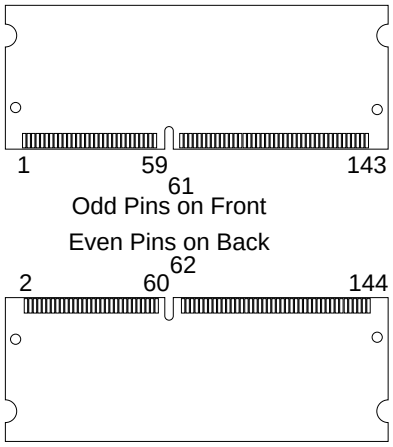
PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	21	V_{SS}	41	DQ_{10}	61	CLK_0	81	V_{DD}	101	V_{DD}	121	DQ_{24}	141	SDA
2	V_{SS}	22	V_{SS}	42	DQ_{42}	62	CKE_0	82	V_{DD}	102	V_{DD}	122	DQ_{56}	142	SCL
3	DQ_0	23	$DQMB_0$	43	DQ_{11}	63	V_{DD}	83	DQ_{16}	103	A_6	123	DQ_{25}	143	V_{DD}
4	DQ_{32}	24	$DQMB_4$	44	DQ_{43}	64	V_{DD}	84	DQ_{48}	104	A_7	124	DQ_{57}	144	V_{DD}
5	DQ_1	25	$DQMB_1$	45	V_{DD}	65	$\overline{RAS}$	85	DQ_{17}	105	A_8	125	DQ_{26}		
6	DQ_{33}	26	$DQMB_5$	46	V_{DD}	66	$\overline{CAS}$	86	DQ_{49}	106	BA_0	126	DQ_{58}		
7	DQ_2	27	V_{DD}	47	DQ_{12}	67	$\overline{WE}$	87	DQ_{18}	107	V_{SS}	127	DQ_{27}		
8	DQ_{34}	28	V_{DD}	48	DQ_{44}	68	CKE_1*	88	DQ_{50}	108	V_{SS}	128	DQ_{59}		
9	DQ_3	29	A_0	49	DQ_{13}	69	$\overline{S}_0$	89	DQ_{19}	109	A_9	129	V_{DD}		
10	DQ_{35}	30	A_3	50	DQ_{45}	70	A_{12}	90	DQ_{51}	110	BA_1	130	V_{DD}		
11	V_{DD}	31	A_1	51	DQ_{14}	71	$\overline{S}_1$*	91	V_{SS}	111	A_{10}/AP	131	DQ_{28}		
12	V_{DD}	32	A_4	52	DQ_{46}	72	A_{13}*	92	V_{SS}	112	A_{11}	132	DQ_{60}		
13	DQ_4	33	A_2	53	DQ_{15}	73	NC	93	DQ_{20}	113	V_{DD}	133	DQ_{29}		
14	DQ_{36}	34	A_5	54	DQ_{47}	74	CLK_1*	94	DQ_{52}	114	V_{DD}	134	DQ_{61}		
15	DQ_5	35	V_{SS}	55	V_{SS}	75	V_{SS}	95	DQ_{21}	115	$DQMB_2$	135	DQ_{30}		
16	DQ_{37}	36	V_{SS}	56	V_{SS}	76	V_{SS}	96	DQ_{53}	116	$DQMB_6$	136	DQ_{62}		
17	DQ_6	37	DQ_8	57	CB_0	77	CB_2	97	DQ_{22}	117	$DQMB_3$	137	DQ_{31}		
18	DQ_{38}	38	DQ_{40}	58	CB_4	78	CB_6	98	DQ_{54}	118	$DQMB_7$	138	DQ_{63}		
19	DQ_7	39	DQ_9	59	CB_1	79	CB_3	99	DQ_{23}	119	V_{SS}	139	V_{SS}		
20	DQ_{39}	40	DQ_{41}	60	CB_5	80	CB_7	100	DQ_{55}	120	V_{SS}	140	V_{SS}		

* Not used

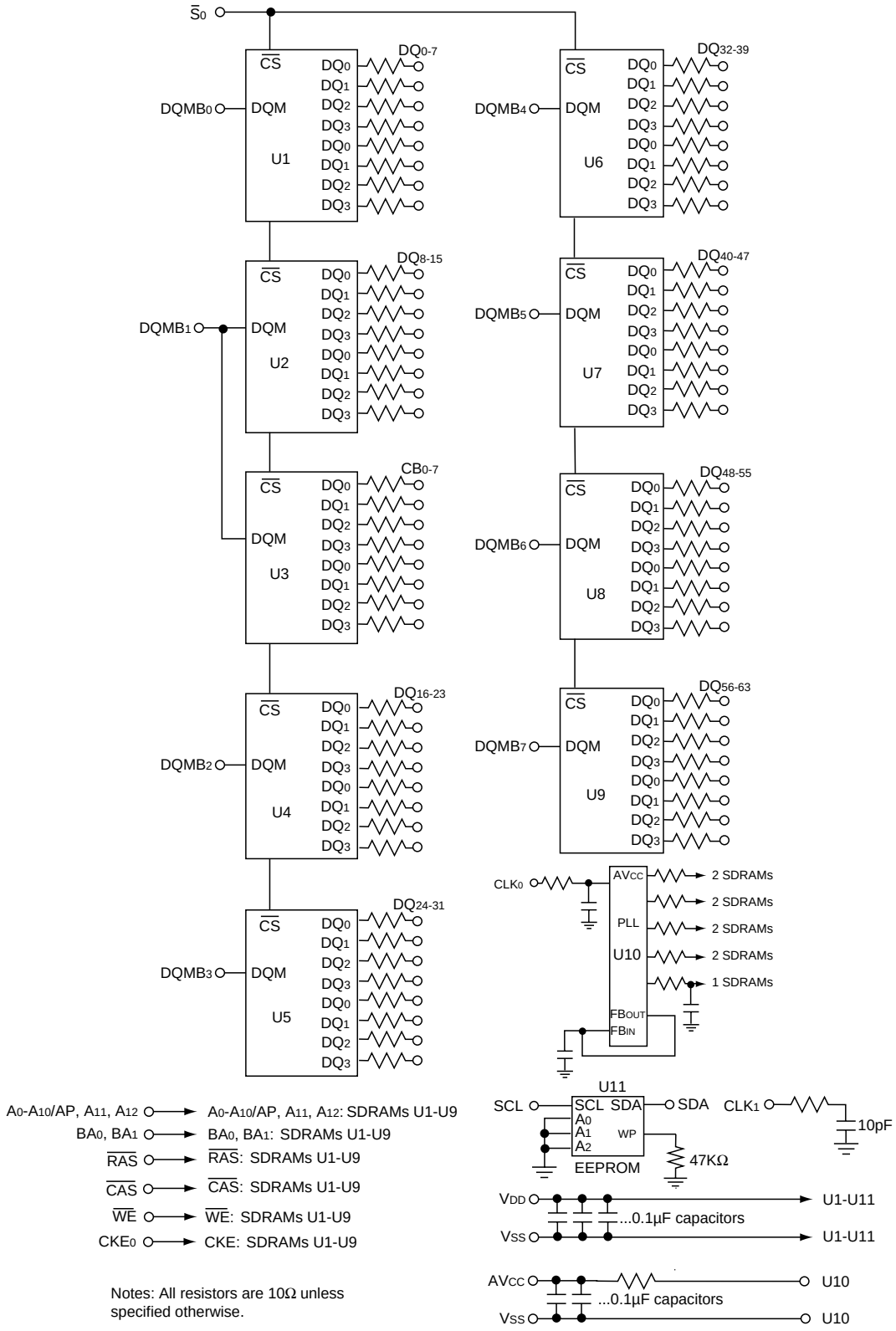
Pin Arrangement



Pin Functions

Pin Name	Pin Function
A_0-A_{10}/AP, A_{11}, A_{12}	Address Inputs (multiplexed)
BA_0, BA_1	Select Bank
DQ_0-DQ_{63}	Data In/Out
CB_0-CB_7	Check Bits
$\overline{WE}$	Read/Write Enable
CLK_0	Clock Input
CKE_0	Clock Enable Input
$\overline{RAS}$	Row Adress Strobe
$\overline{CAS}$	Column Address Strobe
$DQMB_0$-$DQMB_7$	Data Input/Output Mask
$\overline{S}_0$	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
V_{DD}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



Notes: All resistors are 10Ω unless specified otherwise.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I^2C; Current sink capability of SDA driver ≤3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	SDRAM	04h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	11	0Bh
5	# of module banks on this assembly	1 bank	01h
6	Data width of this assembly	72 bits	48h
7	…Data width of this assembly (continued)	—	00h
8	Voltage interface standard of this assembly	LVTTL	01h
9	SDRAM cycle time at CL=3 (t_{CYC})	7.5ns	75h
10	SDRAM access time from clock at CL=3 (t_{AC})	5.4ns	54h
11	DIMM configuration type	ECC	02h
12	Refresh rate/type	7.8µs, Self-refresh	82h
13	SDRAM width	8 bits	08h
14	Error Checking DRAM data width	8 bits	08h
15	Min. CLK delay for back-to-back rand. col. addr.	t_{CCD}=1 CLK	01h
16	SDRAM device attributes: burst lengths supported	1,2,4,8, and Full Page	8Fh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2,3	06h
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 0	01h
21	SDRAM module attributes	on-card PLL, non-buff., non-reg.	04h
22	SDRAM device attributes: general	V_{CC}10%, B/R, S/W, P/A, A/P	0Eh
23	Minimum clock cycle time at CL=2 (t_{CYC})	10ns	A0h
24	Max. data access time form clock at CL=2 (t_{AC})	6ns	60h
25	Minimum clock cycle time at CL=1 (t_{CYC})	—	00h
26	Max. data access time from clock at CL=1 (t_{AC})	—	00h
27	Minimum row precharge time (t_{RP})	20ns	14h
28	Minimum row active to row active delay (t_{RRD})	15ns	0Fh
29	Minumum RAS to CAS (t_{RCD})	20ns	14h
30	Minumum RAS pulse width (t_{RAS})	45ns	2Dh
31	Module bank density	512MB	80h
32	Min. command and address signal setup time (t_{AS})	1.5ns	15h
33	Min. command and address signal hold time (t_{AH})	0.8ns	08h
34	Min. data signal input setup time (t_{DS})	1.5ns	15h

(Serial Presence Detect Information continued on the next page)

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Byte #	Function Described	Function Supported	Hex Value
35	Min. data signal input hold time (t_{DH})	0.8ns	08h
36-61	Superset information (may be used in future)	—	00h
62	SPD revision	1.2	12h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	SimpleTech's ID	A8h
66-71			00h
72	Manufacturing location	SimpleTech USA	01h
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)	01h
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	ww
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
98		Serial number (bits 23-16)	ss
99-125	Manufacturer's specific data		xxh
126	Intel specification frequency	100MHz	64h
127	Intel specification details	Detailed 100MHz Info	8Fh

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{DD}	-1.0 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}=0, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	2
Output High Voltage Level	V_{OH}	2.4	—	—	V	3
Output Low Voltage Level	V_{OL}	—	—	0.4	V	4
Input Leakage Current	I_{IL}	-90	—	90	µA	5

1. V_{IH}(max)=5.6 V AC (pulse width ≤3 ns acceptable)
2. V_{IL}(min) = -2.0 V AC (pulse width ≤3 ns acceptable)
3. I_{OH}=-2mA for Samsung parts; I_{OH}=-4mA for Micron parts.
4. I_{OL}=2mA for Samsung parts; I_{OL}=4mA for Micron parts.
5. Any input $0 \le V_{IN} \le V_{DD}$.

CAPACITANCE (T_A=23 °C, V_{DD}=3.3V, f=1MHz, V_{REF}=1.4±200mA)

Item	Symbol	Max	Units
Input Capacitance (A_0-A_{10}/AP, A_{11}, A_{12}, BA_0, BA_1)	C_{IN1}	44	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	44	pF
Input Capacitance (CLK_0)	C_{IN3}	12	pF
Input Capacitance (CKE_0)	C_{IN4}	44	pF
Input Capacitance ($\overline{S_0}$)	C_{IN5}	44	pF
Input Capacitance ($DQMB_0$, $DQMB_2$-$DQMB_7$)	C_{IN6}	14	pF
Input Capacitance ($DQMB_1$)	C_{IN7}	18	pF
Input/Output Capacitance (DQ_0-DQ_{63})	C_{IO1}	16	pF

DC CHARACTERISTICS

Recommended operating conditions unless otherwise noted.
T_A=0 to 70°C.

Parameter	Symbol	Test Condition	Max	Units
Operating Current (One Bank Active)	I_{CC1S}	Burst length=1, $t_{RC} \geq t_{RC}$(min), I_{OL}=0mA, Outputs open	1800	mA
Precharge Standby Current in Power-Down Mode	I_{CC2P} I_{CC2PS}	CKE≤V_{IL}(max), t_{CLK}=10ns, CKE and CLK≤V_{IL}(max), t_{CLK}=∞	54 45	mA mA
Precharge Standby Current in Non Power-Down Mode	I_{CC2N}	CKE and S≥V_{IH}(min), t_{CLK}=10ns Input signals are changed one time during 20ns	270	mA
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CLK}=∞ Input signals are stable	90	mA
Active Standby Current in Power-Down Mode	I_{CC3P} I_{CC3PS}	CKE≤V_{IL}(max), t_{CLK}=10ns CKE and CLK≤V_{IL}(max), t_{CLK}=∞	90 72	mA mA
Active Standby Current in Non Power-Down Mode (One Bank Active)	I_{CC3N}	CKEand S≥V_{IH}(min), t_{CLK}=10ns, Input signals are changed one time during 20ns	450	mA
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CLK}=∞ Inputs are stable	315	mA
Operating Current (Burst Mode)	I_{CC4}	I_{OL}=0mA, BL=Full Page, 4 banks activated I_{CCD}=2 CLKs, Outputs open	1800	mA
Refresh Current (Refresh Period is 64ms)	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	2970	mA
Self Refresh Current	I_{CC6}	CKE≤0.2V	63	mA

AC TIMING PARAMETERS (T_A=0-65°C; V_{CC}=3.0V-3.6V; CL=2, 3)

Parameter	Symbol	Speed Grade 100MHz		Speed Grade 133MHz/100MHz		Unit	Notes
		Min	Max	Min	Max		
Clock Period	t_{CLK}	10		7.5		ns	
Clock High Time (Rated @1.5V)	t_{CH}	3		2.5		ns	
Clock Low Time	t_{CL}	3		2.5		ns	
Input Setup Times (Data) (Address/Command & CKE)	t_{SI}	2 2		1.5 1.5		ns	
Input Hold Times (Data) (Address/Command & CKE)	t_{HI}	1 1		0.8 0.8		ns	
Output Valid From Clock (CL=2; limited application; 2 banks; all outputs switching)	t_{AC}		7.0		N/A	ns	1
Output Valid From Clock (CL=2; LVTTL levels; Rated@50pF; all outputs switching)	t_{AC}		6.0 (t_{CO}= 5.2)		5.4 (t_{CO}= 4.6)	ns	1
Output Valid From Clock (CL=3; LVTTL levels; Rated@50pF; all outputs switching)	t_{AC}		6.0 (t_{CO}= 5.2)		5.4 (t_{CO}= 4.6)	ns	1
Output Hold From Clock (Rated@50pF; 1.8ns@0pF)	t_{OH}	3		2.7		ns	
Output Valid to Z	t_{OHZ}	3	9	2.7	7	ns	
CAS to CAS Delay	t_{CCD}	1		1		t_{CLK}	
CAS Bank Delay	t_{CBD}	1		1		t_{CLK}	
CKE to Clock Disable	t_{CKE}	1		1		t_{CLK}	
RAS Precharge Time	t_{RP}	20.0		20.0		ns	
RAS Active Time	t_{RAS}	50		45		ns	
Active to Command Delay (RAS to CAS Delay)	t_{RCD}	20.0		20.0		ns	
RAS to RAS Bank Activate Delay	t_{RRD}	20		15		ns	
RAS Cycle Time	t_{RC}	70		67.5		ns	
DQM to Input Data Delay	t_{DQD}	0		0		t_{CLK}	
Write Cmd. to Input Data Delay	t_{DWD}	0		0		t_{CLK}	
Mode Register Set to Active Delay	t_{MRD}	3		3		t_{CLK}	
Precharge to O/P in High-Z	t_{ROH}		CL		CL	t_{CLK}	2
DQM to Data in Hi-Z for Read	t_{DQZ}	2		2		t_{CLK}	
DQM to Data Mask for Write	t_{DQM}	0		0		t_{CLK}	3
Data-In to PRE Command Period	t_{DPL}	20		15		ns	
Data-In to ACT (PRE) Cmd Period (Auto Precharge)	t_{DAL}	5		5		t_{CLK}	
Power Down Mode Entry	t_{SB}		1		1	t_{CLK}	
Self Refresh Exit Time	t_{SRX}	10		10		ns	4
Power Down Exit Set Up Time	t_{PDE}	1		1		t_{CLK}	5
Clock Stop During Self Refresh or Power Down	t_{CLKSTP}	200		200		t_{CLK}	6
Refresh Period (4096 refresh cycles)	t_{REF}		64		64	ms	7
Row Refresh Cycle Time	t_{RFC}	80.0		75.0		ns	

1. Access times to be measured with input signals of 1V/ns edge rate, 0.8V to 2.0V. t_{ACN}=access time with 0pF load.
2. CL=CAS Latency.
3. Data Masked on the same clock.
4. Self refresh Exit is asynchronous, requiring 10ns to ensure initiation. Self refresh exit is complete in 10ns + t_{RC}.
5. Timing is asynchronous. If t_{set} is not met by rising edge of CLK then CKE is assumed latched on next cycle.
6. If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.
7. For 64Mbit and 128Mbit SDRAM technology, 4096 refresh cycles. For 256Mbit and 512 Mbit technology, 8192 refresh cycles.

REVISION HISTORY

Rev.	Change Description from Previous Revision
-101	Initial Release. 3/21/2002.