

128M X 72 Bits (1GB) 144-Pin SDRAM SO-DIMM with ECC (PC133)**FEATURES**

- PC133 Compliant ($t_{CYC}=7.5ns@CL=3$) (see *Ordering Information* for options)
- Burst Mode Operation
- Auto and self refresh capability (8192 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- $+3.3V \pm 0.3V$ power supply
- MRS cycle with address key programs
 - Latency (access from column address)
 - Burst Length (1, 2, 4, 8, and Full Page)
 - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with 256 Byte EEPROM
- ECC

GENERAL DESCRIPTION

The SimpleTech SL72G7M128M8H-A75AV is a 128M x 72 bits Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-Line Memory Module (SO-DIMM).

The module consists of nine IC Towers (stack of two SDRAMs) mounted on a 144-pin glass epoxy substrate.

Each IC Tower consists of two 16M x 8 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP II monolithic packages. The IC Tower stacking technology is patented by SimpleTech with Patent Number RE.36,916.

A serial EEPROM using the two pin I²C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.1 μ F are mounted. Damping resistors are mounted for the data lines. A PLL supplies clocks to the SDRAMs from one clock input.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V.

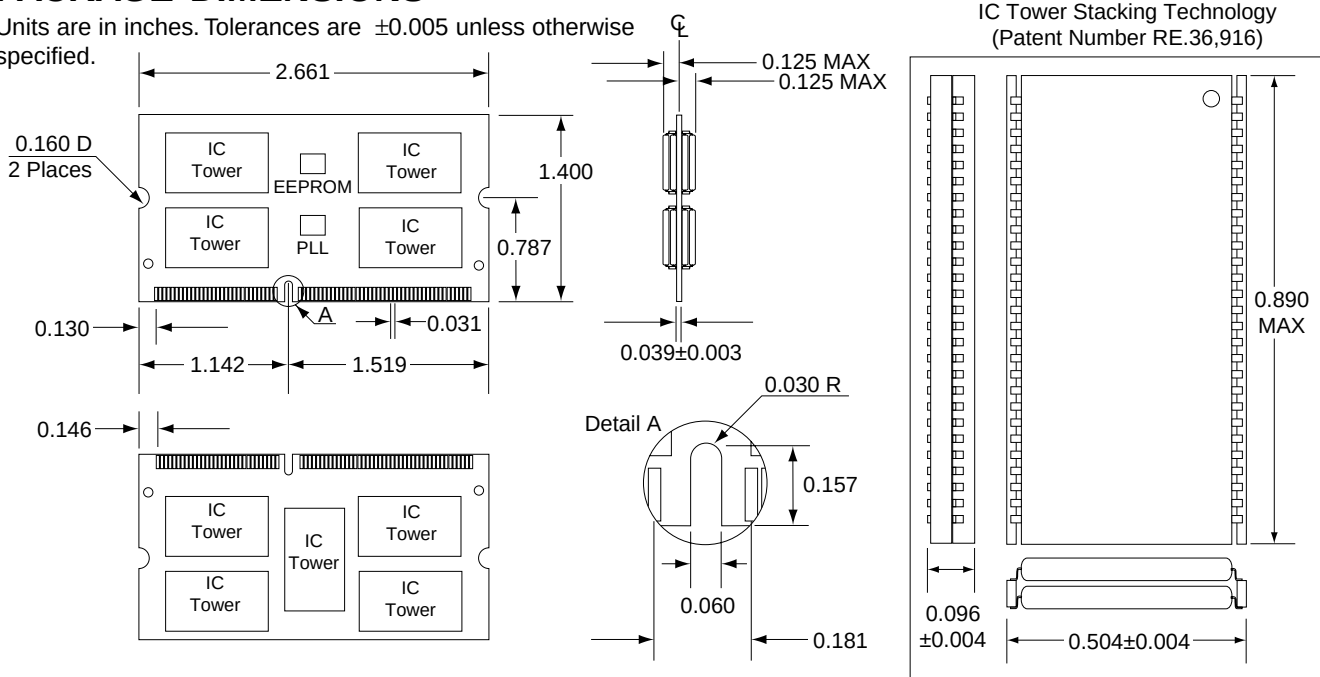
See *Ordering Information* for PC133 performance options.

ORDERING INFORMATION

SimpleTech Manuf. Part Number	PC133 133MHz Parameters			
	CL	tRCD	tRP	tRC
SL72G7M128M8H-A75AV	3clks	20ns	20ns	67.5ns

PACKAGE DIMENSIONS

Units are in inches. Tolerances are ± 0.005 unless otherwise specified.



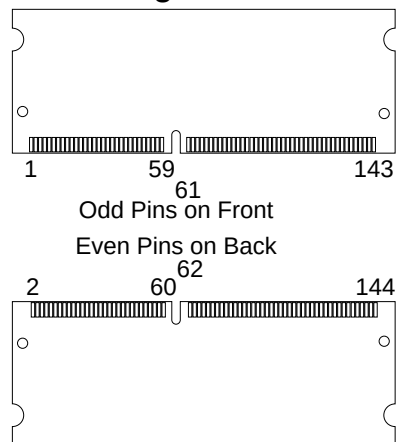
PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS	21	VSS	41	DQ10	61	CLK0	81	VDD	101	VDD	121	DQ24	141	SDA
2	VSS	22	VSS	42	DQ42	62	CKE0	82	VDD	102	VDD	122	DQ56	142	SCL
3	DQ0	23	DQMB0	43	DQ11	63	VDD	83	DQ16	103	A6	123	DQ25	143	VDD
4	DQ32	24	DQMB4	44	DQ43	64	VDD	84	DQ48	104	A7	124	DQ57	144	VDD
5	DQ1	25	DQMB1	45	VDD	65	$\overline{\text{RAS}}$	85	DQ17	105	A8	125	DQ26		
6	DQ33	26	DQMB5	46	VDD	66	$\overline{\text{CAS}}$	86	DQ49	106	BA0	126	DQ58		
7	DQ2	27	VDD	47	DQ12	67	$\overline{\text{WE}}$	87	DQ18	107	VSS	127	DQ27		
8	DQ34	28	VDD	48	DQ44	68	CKE1	88	DQ50	108	VSS	128	DQ59		
9	DQ3	29	A0	49	DQ13	69	$\overline{\text{S}}_0$	89	DQ19	109	A9	129	VDD		
10	DQ35	30	A3	50	DQ45	70	A12	90	DQ51	110	BA1	130	VDD		
11	VDD	31	A1	51	DQ14	71	$\overline{\text{S}}_1$	91	VSS	111	A10/AP	131	DQ28		
12	VDD	32	A4	52	DQ46	72	A13*	92	VSS	112	A11	132	DQ60		
13	DQ4	33	A2	53	DQ15	73	NC	93	DQ20	113	VDD	133	DQ29		
14	DQ36	34	A5	54	DQ47	74	CLK1*	94	DQ52	114	VDD	134	DQ61		
15	DQ5	35	VSS	55	VSS	75	VSS	95	DQ21	115	DQMB2	135	DQ30		
16	DQ37	36	VSS	56	VSS	76	VSS	96	DQ53	116	DQMB6	136	DQ62		
17	DQ6	37	DQ8	57	CB0	77	CB2	97	DQ22	117	DQMB3	137	DQ31		
18	DQ38	38	DQ40	58	CB4	78	CB6	98	DQ54	118	DQMB7	138	DQ63		
19	DQ7	39	DQ9	59	CB1	79	CB3	99	DQ23	119	VSS	139	VSS		
20	DQ39	40	DQ41	60	CB5	80	CB7	100	DQ55	120	VSS	140	VSS		

* Not used

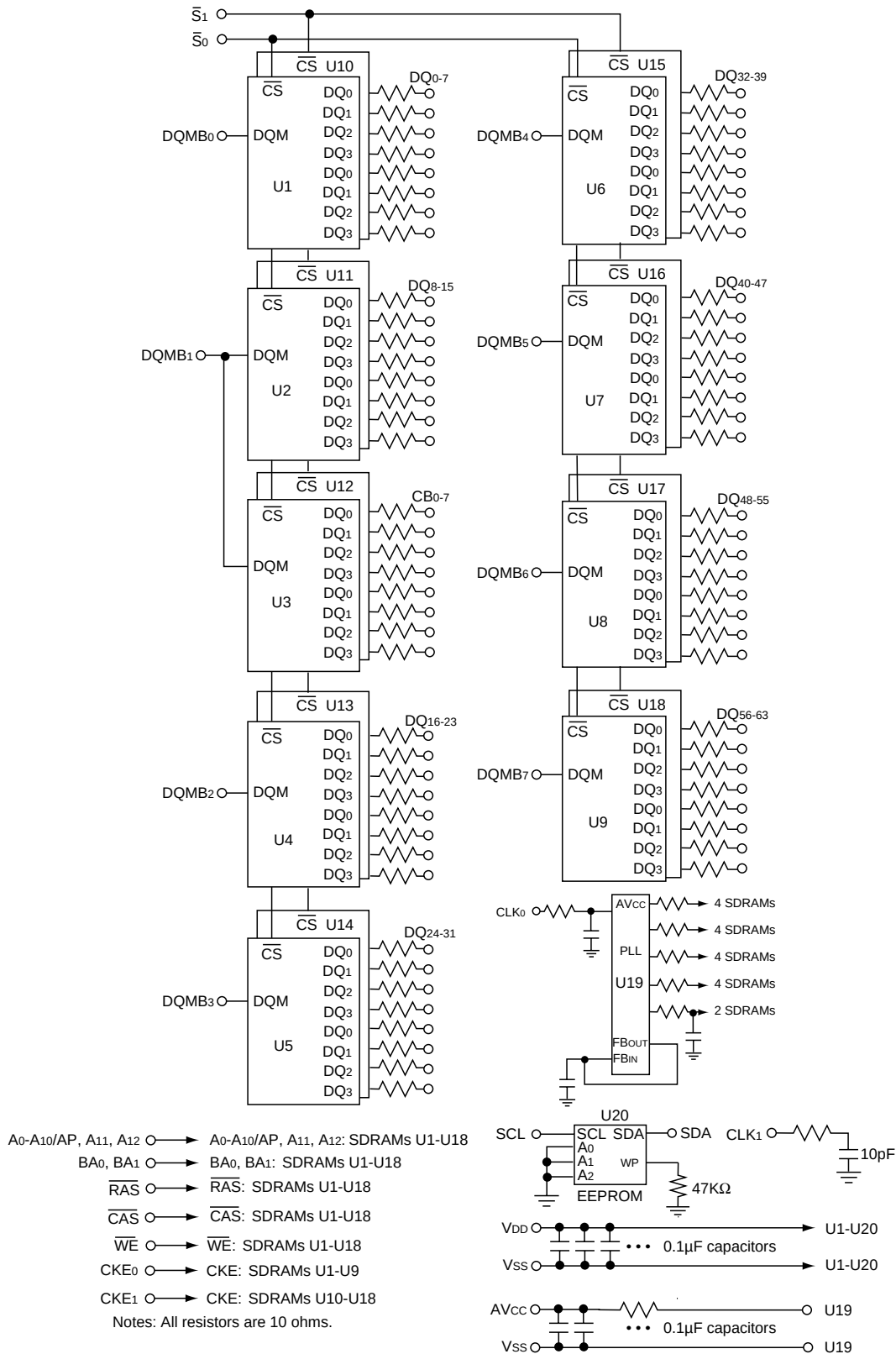
Pin Arrangement



Pin Functions

Pin Name	Pin Function
A0-A10/AP, A11, A12	Address Inputs (multiplexed)
BA0, BA1	Select Bank
DQ0-DQ63	Data In/Out
CB0-CB7	Check Bits
$\overline{\text{WE}}$	Read/Write Enable
CLK0	Clock Input
CKE0, CKE1	Clock Enable Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQMB0-DQMB7	Data Input/Output Mask
$\overline{\text{S}}_0, \overline{\text{S}}_1$	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I²C; Current sink capability of SDA driver ≤3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	SDRAM	04h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	11	0Bh
5	# of module banks on this assembly	2 banks	02h
6	Data width of this assembly	72 bits	48h
7	...Data width of this assembly (continued)	—	00h
8	Voltage interface standard of this assembly	LVTTTL	01h
9	SDRAM cycle time at CL=3 (t _{CYC})	7.5ns	75h
10	SDRAM access time from clock at CL=3 (t _{AC})	5.4ns	54h
11	DIMM configuration type	ECC	02h
12	Refresh rate/type	7.8μs, Self-refresh	82h
13	SDRAM width	8 bits	08h
14	Error Checking DRAM data width	8 bits	08h
15	Min. CLK delay for back-to-back rand. col. addr.	t _{CCD} =1 CLK	01h
16	SDRAM device attributes: burst lengths supported	1,2,4,8, and Full Page	8Fh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2,3	06h
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 0	01h
21	SDRAM module attributes	on-card PLL, non-buff., non-reg.	04h
22	SDRAM device attributes: general	V _{CC} 10%, B/R, S/W, P/A, A/P	0Eh
23	Minimum clock cycle time at CL=2 (t _{CYC})	10ns	A0h
24	Max. data access time from clock at CL=2 (t _{AC})	6ns	60h
25	Minimum clock cycle time at CL=1 (t _{CYC})	—	00h
26	Max. data access time from clock at CL=1 (t _{AC})	—	00h
27	Minimum row precharge time (t _{RP})	20ns	14h
28	Minimum row active to row active delay (t _{RRD})	15ns	0Fh
29	Minimum RAS to CAS (t _{RCD})	20ns	14h
30	Minimum RAS pulse width (t _{RAS})	45ns	2Dh
31	Module bank density	512MB	80h
32	Min. command and address signal setup time (t _{AS})	1.5ns	15h
33	Min. command and address signal hold time (t _{AH})	0.8ns	08h
34	Min. data signal input setup time (t _{DS})	1.5ns	15h

(Serial Presence Detect Information continued on the next page)

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Byte #	Function Described	Function Supported	Hex Value
35	Min. data signal input hold time (t _{DH})	0.8ns	08h
36-61	Superset information (may be used in future)	—	00h
62	SPD revision	1.2	12h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	SimpleTech's ID	A8h
66-71			00h
72	Manufacturing location	SimpleTech USA	01h
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	Eng(00), RevA(01), RevB(02)	01h
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	ww
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
98		Serial number (bits 23-16)	ss
99-125	Manufacturer's specific data		xxh
126	Intel specification frequency	100MHz	64h
127	Intel specification details	Detailed 100MHz Info	8Fh