32M X 64 Bits (256MB) 200-Pin DDR SDRAM SO-DIMM (PC2100)

FEATURES

- PC2100 Compliant
  (PC266B 133MHz—7.5ns@CL=2.5)
- 200-Pin SO-DIMM form factor
- Auto and self refresh capability
  (8192cycles/64ms refresh)
- SSTL_2 compatible inputs and outputs
- +2.5V ± 0.2V V_{DD}
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect with EEPROM

GENERAL DESCRIPTION

The SimpleTech SL64A8F32M8L-A75EW is a 32M x 64 bits Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of eight CMOS 8M x 8 bits x 4 banks DDR SDRAMs in 66-pin 400-mil TSOP II packages mounted on a 200-pin glass epoxy substrate.

A serial EEPROM using the two pin I^2C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.22µF are mounted. Damping resistors are mounted for DQ, DQS, and DM signals.

The module has gold edge connections and is intended for mounting into 200-pin SO-DIMM edge connector sockets keyed for 2.5V.

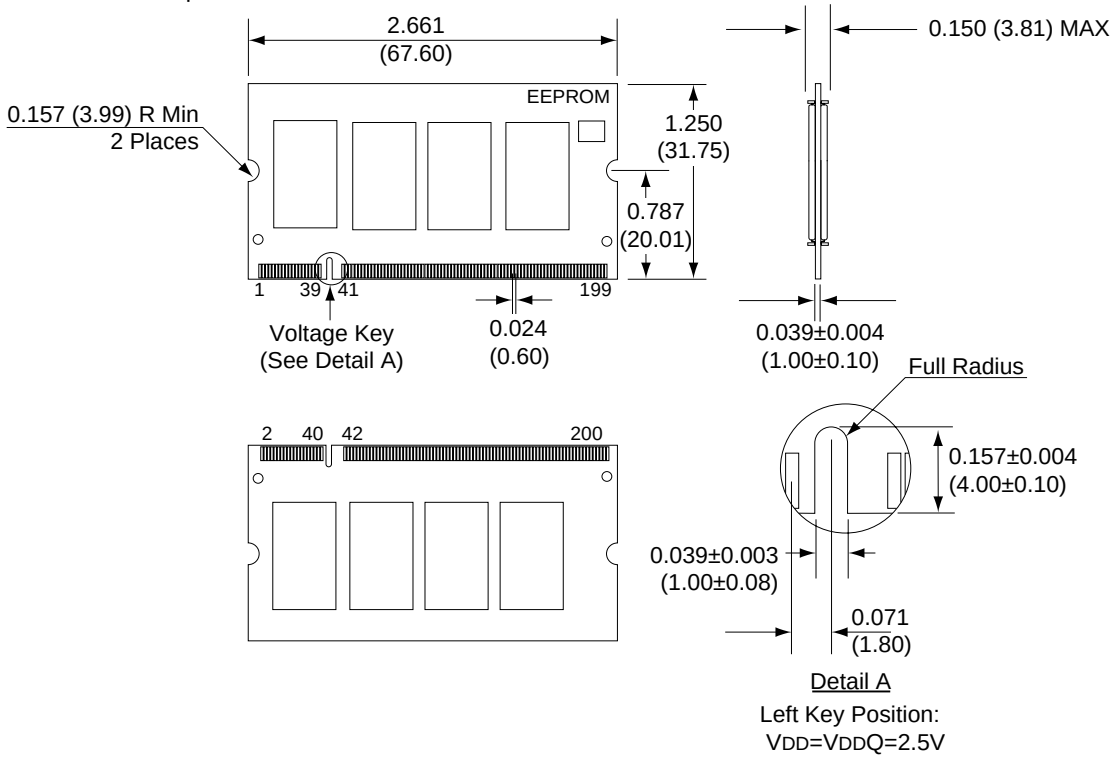
ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL64A8F32M8L-A75EW	2.5	133	2.1 GB/s

PACKAGE DIMENSIONS

Module Dimensions

Units are in inches (millimeters). Tolerances are ±0.005 (±0.127) unless otherwise specified.



922

PIN CONFIGURATION (*=Not Used; /=Active Low)

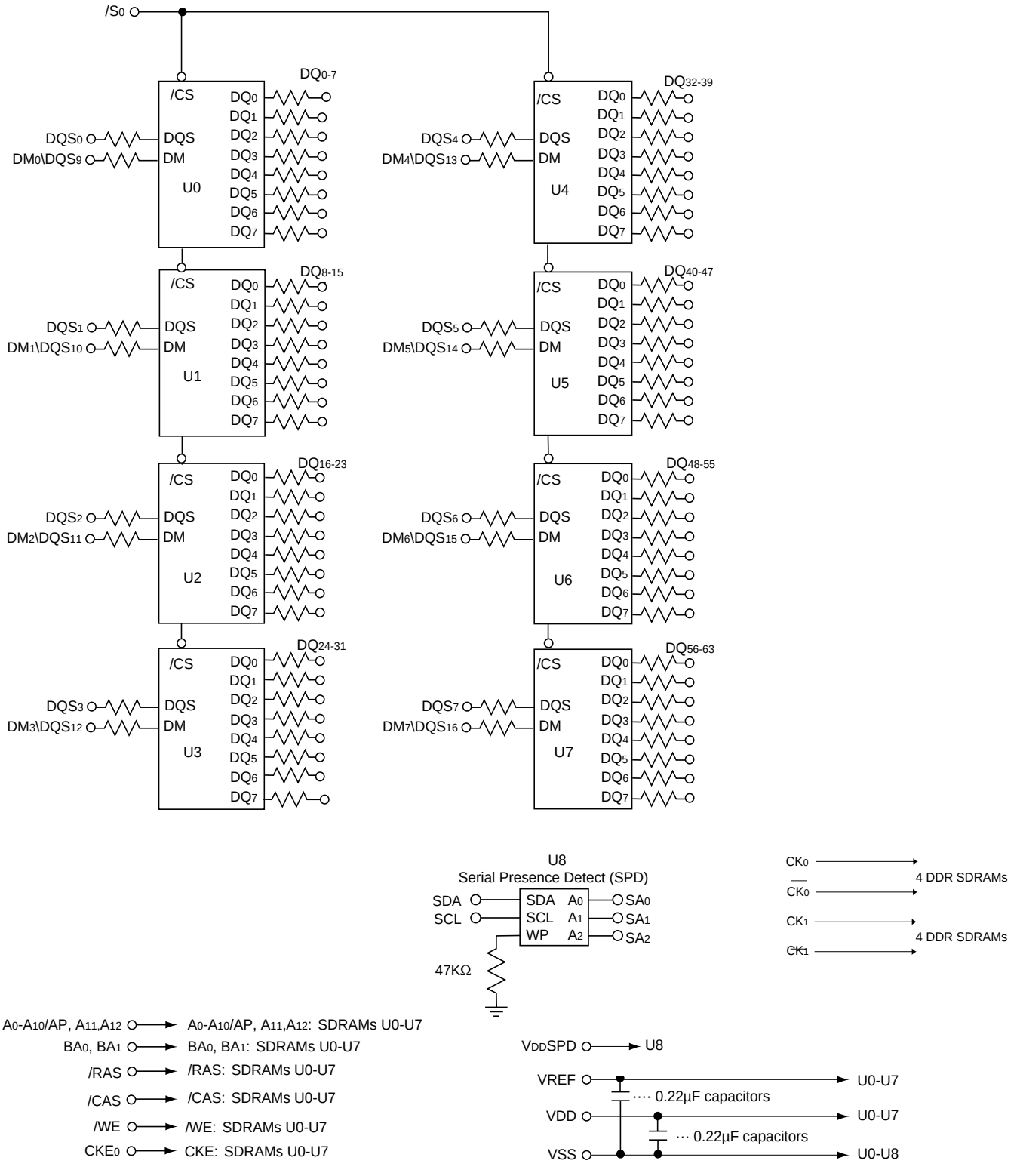
Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	2	V_{REF}	51	V_{SS}	52	V_{SS}	101	A_9	102	A_8	151	DQ_{42}	152	DQ_{46}
3	V_{SS}	4	V_{SS}	53	DQ_{19}	54	DQ_{23}	103	V_{SS}	104	V_{SS}	153	DQ_{43}	154	DQ_{47}
5	DQ_0	6	DQ_4	55	DQ_{24}	56	DQ_{28}	105	A_7	106	A_6	155	V_{DD}	156	V_{DD}
7	DQ_1	8	DQ_5	57	V_{DD}	58	V_{DD}	107	A_5	108	A_4	157	V_{DD}	158	$/CK_1$*
9	V_{DD}	10	V_{DD}	59	DQ_{25}	60	DQ_{29}	109	A_3	110	A_2	159	V_{SS}	160	CK_1*
11	DQS_0	12	DM_0\DQS_9	61	DQS_3	62	DM_3\DQS_{12}	111	A_1	112	A_0	161	V_{SS}	162	V_{SS}
13	DQ_2	14	DQ_6	63	V_{SS}	64	V_{SS}	113	V_{DD}	114	V_{DD}	163	DQ_{48}	164	DQ_{52}
15	V_{SS}	16	V_{SS}	65	DQ_{26}	66	DQ_{30}	115	A_{10}\AP	116	BA_1	165	DQ_{49}	166	DQ_{53}
17	DQ_3	18	DQ_7	67	DQ_{27}	68	DQ_{31}	117	BA_0	118	/RAS	167	V_{DD}	168	V_{DD}
19	DQ_8	20	DQ_{12}	69	V_{DD}	70	V_{DD}	119	/WE	120	/CAS	169	DQS_6	170	DM_6\DQS_{15}
21	V_{DD}	22	V_{DD}	71	CB_0*	72	CB_4*	121	$/S_0$	122	$/S_1$*	171	DQ_{50}	172	DQ_{54}
23	DQ_9	24	DQ_{13}	73	CB_1*	74	CB_5*	123	DU(A_{13})	124	DU(BA_2)	173	V_{SS}	174	V_{SS}
25	DQS_1	26	DM_1\DQS_{10}	75	V_{SS}	76	V_{SS}	125	V_{SS}	126	V_{SS}	175	DQ_{51}	176	DQ_{55}
27	V_{SS}	28	V_{SS}	77	DQS_8*	78	DM_8\DQS_{17}*	127	DQ_{32}	128	DQ_{36}	177	DQ_{56}	178	DQ_{60}
29	DQ_{10}	30	DQ_{14}	79	CB_2*	80	CB_6*	129	DQ_{33}	130	DQ_{37}	179	V_{DD}	180	V_{DD}
31	DQ_{11}	32	DQ_{15}	81	V_{DD}	82	V_{DD}	131	V_{DD}	132	V_{DD}	181	DQ_{57}	182	DQ_{61}
33	V_{DD}	34	V_{DD}	83	CB_3*	84	CB_7*	133	DQS_4	134	DM_4\DQS_{13}	183	DQS_7	184	DM_7\DQS_{16}
35	CK_0	36	V_{DD}	85	DU	86	DU(/RESET)	135	DQ_{34}	136	DQ_{38}	185	V_{SS}	186	V_{SS}
37	$/CK_0$	38	V_{SS}	87	V_{SS}	88	V_{SS}	137	V_{SS}	138	V_{SS}	187	DQ_{58}	188	DQ_{62}
39	V_{SS}	40	V_{SS}	89	CK_2*	90	V_{SS}	139	DQ_{35}	140	DQ_{39}	189	DQ_{59}	190	DQ_{63}
41	DQ_{16}	42	DQ_{20}	91	$/CK_2$*	92	V_{DD}	141	DQ_{40}	142	DQ_{44}	191	V_{DD}	192	V_{DD}
43	DQ_{17}	44	DQ_{21}	93	V_{DD}	94	V_{DD}	143	V_{DD}	144	V_{DD}	193	SDA	194	SA_0
45	V_{DD}	46	V_{DD}	95	CKE_1*	96	CKE_0	145	DQ_{41}	146	DQ_{45}	195	SCL	196	SA_1
47	DQS_2	48	DM_2\DQS_{11}	97	DU	98	DU	147	DQS_5	148	DM_5\DQS_{14}	197	V_{DD}SPD	198	SA_2
49	DQ_{18}	50	DQ_{22}	99	A_{12}*	100	A_{11}	149	V_{SS}	150	V_{SS}	199	V_{DD}ID*	200	DU

Pin Description

Pin Symbol	Pin Function	Pin Symbol	Pin Function
$CK_{(0:2)}$	Clock inputs, positive line	$DQ_{(0:63)}$	Data input/output
$/CK_{(0:2)}$	Clock inputs, negative line	$CB_{(0:7)}$	Data check bits input/output
$CKE_{(0:1)}$	Clock enables	$DM_{(0:8)}$\$DQS_{(9:17)}$	Low data masks/high data strobes
/RAS	Row address strobe	$DQS_{(0:8)}$	Low data strobes
/CAS	Column address strobe	/RESET	Register initialization
/WE	Write enable	V_{DD}	Core power
$/S_{(0:1)}$	Chip selects	V_{SS}	Ground
$A_{(0:9,11:13)}$	Address inputs	V_{REF}	Input/output reference
A_{10}/AP	Address input/Autoprecharge	V_{DD}SPD	SPD power
$BA_{(0:2)}$	SDRAM bank address	V_{DD}ID	V_{DD} identification flag
SCL	SPD clock input		
SDA	SPD data input/output	DU	Don't Use
$SA_{(0:2)}$	SPD address		

FUNCTIONAL BLOCK DIAGRAM



Notes: 1 Unless otherwise noted, all series resistors are 25Ω.
2 DQ wiring may differ from that described in this drawing; however DQ, DQS, DM, CKE, and /S relationships are maintained as shown.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I^2C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
		PC266B	**PC266B**
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	DDR SDRAM	07h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	10	0Ah
5	# of physical banks on this assembly	1 bank	01h
6	Data width of this assembly	64 bits	40h
7	…Data width of this assembly (continued)	—	00h
8	Voltage interface level of this assembly	SSTL 2.5V	04h
9	SDRAM cycle time at CL=2.5 (t_{CYC})	7.5ns	75h
10	SDRAM access time from clock at CL=2.5 (t_{AC})	0.75ns	75h
11	DIMM configuration type	none	00h
12	Refresh rate/type	7.8µs, Self -refresh	82h
13	SDRAM width	8 bits	08h
14	Error Checking SDRAM data width	none	00h
15	Min. CLK delay for back-to-back rand. col. addr.	t_{CCD}=1 CLK	01h
16	SDRAM device attributes: burst lengths supported	2,4,8	0Eh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5	0Ch
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 1	02h
21	SDRAM module attributes	Differential clock	24h
22	SDRAM device attributes: general	V_{DD}±0.2V	00h
23	Minimum clock cycle time at CL=2 (t_{CYC})	10ns	A0h
24	Max. data access time form clock at CL=2 (t_{AC})	0.75ns	75h
25	Minimum clock cycle time at CL=1.5 (t_{CYC})	N/A	00h
26	Max. data access time from clock at CL=1.5 (t_{AC})	N/A	00h
27	Minimum row precharge time (t_{RP})	20.0ns	50h
28	Minimum row active to row active delay (t_{RRD})	15.0ns	3Ch
29	Minumum RAS to CAS (t_{RCD})	20.0ns	50h
30	Minumum RAS pulse width (t_{RAS})	45ns	2Dh
31	Module bank density	128MB	20h
32	Min. command and address signal setup time (t_{IS})	0.9ns	90h
33	Min. command and address signal hold time (t_{IH})	0.9ns	90h
34	Min. data/data mask signal input setup time (t_{DS})	0.5ns	50h
35	Min. data/data mask signal input hold time (t_{DH})	0.5ns	50h

continued on the next page

Byte #	Function Described	Function Supported	Hex Value
		PC266B	PC266B
36-40	Superset information (may be used in future)	no superset	00h
41	Row cycle time (t_{RC})	65ns	41h
42	Auto refresh cycle time (t_{RFC})	75ns	4Bh
43	Maximum SDRAM device cycle time (t_{CK_MAX})	12ns	30h
44	DQS-DQ skew (t_{DQSQ})	0.50ns	32h
45	SDRAM device data hold skew factor (t_{QHS})	0.75ns	75h
46-61	Reserved		00h
62	SPD revision	JEDEC 1	00h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	SimpleTech's ID	A8h
66-71			00h
72	Manufacturing location	SimpleTech USA	01h
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)	01h
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	ww
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
98		Serial number (bits 23-16)	ss
99-127	Manufacturer's specific data		xxh
128-255		Undefined	00h