About LVDS

As the bandwidth increases in Telecom / Datacom and even in consumer / commercial applications , the high speed, low power, noise, and cost of LVDS signal broaden the scope of its application beyond the traditional technologies such as ECL / PECL.

LVDS (Low Voltage Differential Signaling) are differential signals with typical 350 mV swing and a DC offset of 1.2V. When moving signals from box-to-box or board-to-board (i.e. flat panel display). LVDS is the right solution because it generates less noise, consumes less power and it is very cost effective. Figure 1 shows different voltage levels for different types of signals.

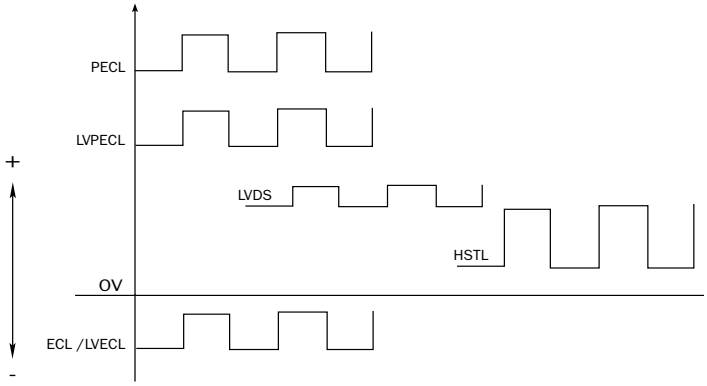

Figure 1: Relative differences among various I/O standards

Note:
HSTL (High-Speed Transceiver Logic) signals are used in computing design applications such as memory drivers and high-speed CPU-to-Memory interfacing.

Interfacing LVDS with PECL and LVPECL

Signal level translation between PECL / LVPECL to LVDS can be achieved using resistor divider network; however, when using discrete logic the signal voltage level would shift with respect to supply voltage and ambient temperature fluctuation. In turn, this will diminish the signal integrity and cause duty cycle distortion. To avoid such problems, Semtech has designed a fully integrated IC devices that translate PECL / LVPECL signal into LVDS and LVDS to PECL / LVPECL type signals. Refer to table 1 for a list of these devices. Semtech also offers a fully integrated receiver / driver device with true LVDS inputs and outputs (SK1303) in an 8-lead SOIC and MSOP packages.

LVDS signals can easily be terminated with a 100 Ω resistor across the differential LVDS outputs. Most devices with LVDS I / O provide the 100Ω resistor internally at its inputs to minimize component count (i.e. SK1301). Figure 2 is an example of LVDS output termination. For PECL / LVPECL output termination refer to application note AN1003.

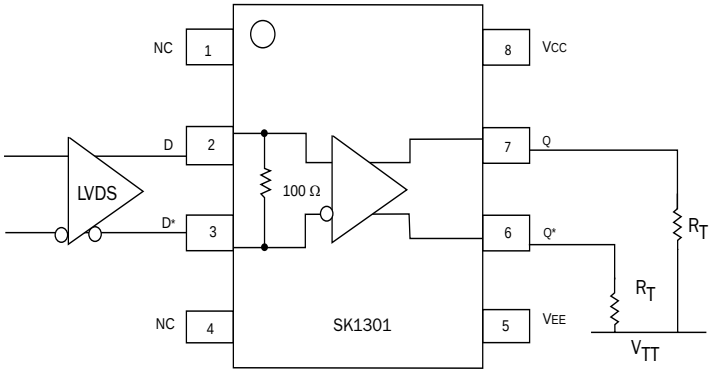

Figure 2: LVDS Termination

Interfacing LVDS with PECL and LVPECL *(con'd)*

Device	Function	Package Type	Operating Voltage
SK1300	PECL / LVPECL to LVDS Translator	8 PIN SOIC / MSOP	3.0V to 5.5V
SK1301	LVDS to PECL / LVPECL Translator	8 PIN SOIC / MSOP	3.0V to 5.5V

Table 1

LVDS with PECL / LVPECL Signal Distribution

Figure 3 is a good example showing how we can fan-out LVDS signal using PECL / LVPECL devices. SK10/100EL11W, a 1:2 fan-out buffer, is used as an example to fan-out the LVDS signal into either PECL or LVPECL signals. It is important to mention that SK100EL11W has PECL / LVPECL type inputs, but with its extended input common mode range it can accept LVDS type signal without having to go through any kind of signal translation. This kind of feature makes clock distribution or generation devices ideal to directly interface with LVDS signals and provide PECL / LVPECL type outputs. Table 2 depicts some of the devices that can directly accept LVDS signals.

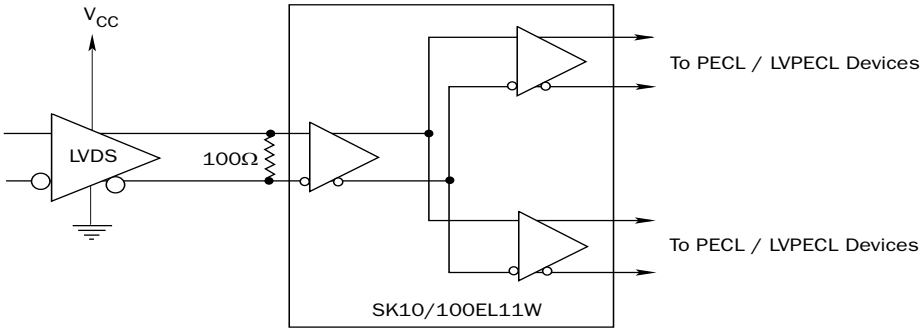

Figure 3: LVDS to PECL / LVPECL

LVDS with PECL / LVPECL Signal Distribution *(con'd)*

Device	Function	Package Type	Operating Voltage
SK10/100EL11W	1:2 Differential Fanout Buffer	8 PIN SOIC/MSOP	3.0V to 5.5V
SK10/100EL14W	1:5 Clock Distribution Chip	20 PIN SOIC	3.0V to 5.5V
SK10/100EL15W	1:4 Clock Distribution	16 PIN SOIC	3.0V to 5.5V
SK10/100EL38W	÷2, ÷4/6 Clock Generation Chip	20 PIN SOIC	3.0V to 5.5V
SK10/100EL39W	÷2/4, ÷4/6 Clock Generation Chip	20 PIN SOIC	3.0V to 5.5V
SK10/100EL57W	4:1 Differential Multiplexer	16 PIN SOIC	3.0V to 5.5V
SK10/100EL91W	Triple PECL to ECL / LVECL and LVPECL to ECL / LVECL Translator	20 PIN SOIC	-5.0V to -3.0V/ 3.0V to 5.5V
SK10/100LVEL111/E	1:9 Differential LVECL / LVPECL Clock Driver	20 PIN PLCC	3.0V to 3.8V
SK15XX	1:5 Signal Distribution	32 PIN TQFP	3.0V to 5.5V
SK19XX	1:9 Signal Distribution	32 PIN TQFP	3.3V to 5.2V
SK44XX	Quad Buffer/Receiver	32 PIN TQFP	3.3V to 5.2V

Table 2

Interfacing LVDS with ECL and LVECL

Since LVDS signals are in the positive region, they can interface with ECL / LVECL signal in two different ways. The first method is to simply use SK10 / 100EL91W, triple PECL to ECL / LVECL and LVPECL to ECL / LVECL translator, to convert the LVDS signal into ECL or LVECL type signal. The extended input common mode range of SK10 / 100EL91W will allow the LVDS signal to directly interface with the inputs of SK10 / 100EL91W. Figure 4 shows LVDS interface to ECL / LVECL using SK10 / 100EL91W, please note that for ECL / LVECL output termination refer to the application note AN1003.

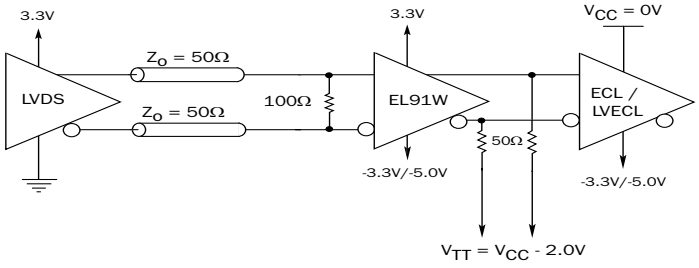

Figure 4: LVDS tp ECL/LVECL

The alternative method would be the capacitive coupling of the LVDS to ECL / LVECL signals. Figure 5 shows such interface with ECL devices that provide a VBB output. The 100 KΩ resistor is to prevent the outputs from oscillating during null state signal conditions. If the VBB output is not provided by the ECL device, Thevenin equivalent parallel termination scheme can be used to reset the threshold to the inputs of the ECL / LVECL device, as shown in Figure 6. In the board layout, both the capacitors and the resistors must be as close to the ECL / LVECL device as possible.

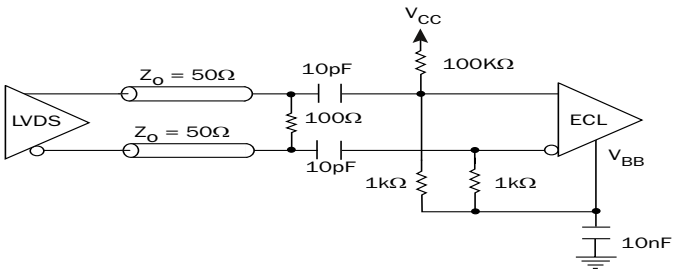

Figure 5: Cacapitive Coupling of LVDS to ECL

Interfacing LVDS with ECL and LVECL *(con'd)*

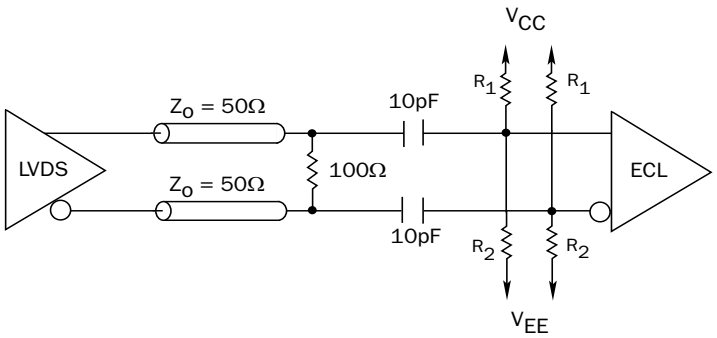

Figure 6: Capacitive Coupling of LDVS to ECL with Different Termination

Examples: VCC = GND, VEE = -5.0V: R1 = 1.2 KΩ and R2 = 3.4KΩ
VCC = GND, VEE = -3.3V: R1 = 680Ω and R2 = 1 KΩ

Interfacing ECL / LVECL with LVDS

The ECL / LVECL outputs are emitter follower outputs; therefore, they need a DC path to VEE. When capacitive coupled, the ECL outputs need pull-down resistors to VEE as shown in Figure 7. The Thevenin equivalent parallel termination resistors represent the termination of the transmission line Zo = R1 || R2 and generates a DC level of 1.2V (typical) which is the threshold of the LVDS signal.

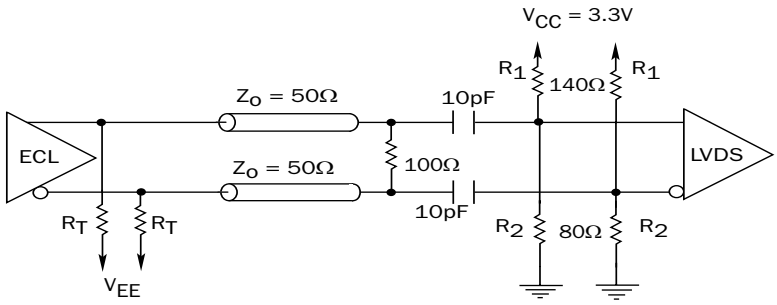

Figure 7: ECL / LVECL to LVDS

Note: R_T = 150Ω for a 3.3V system and
R_T = 270Ω for a 5.0V system.

Contact Information

Semtech Corporation
High-Performance Products Division

Division Headquarters
10021 Willow Creek Road
San Diego, CA 92131
Phone: (858) 695-1808
FAX: (858) 695-2633

Marketing Group
1111 Comstock Street
Santa Clara, CA 95054
Phone: (408) 566-8776
FAX: (408) 727-8994