SFC05C-1
ChipClamp™
Flip Chip Single Line TVS Diode

PROTECTION PRODUCTS

Description

The SFC05C-1 is a single line flip chip CSP TVS diode. It is a state-of-the-art device that utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. The SFC series TVS diodes are designed to protect sensitive semiconductor components from damage or latch-up due to electrostatic discharge (ESD) and other voltage induced transient events.

The SFC05C-1 is a 4-bump, 0.65mm pitch flip chip array with a 2x2 bump grid. It measures 1.0 x 0.5 x 0.60 mm. This small outline makes the SFC05C-1 especially well suited for portable applications. CSP TVS devices are compatible with current pick and place equipment and assembly methods.

Each device will protect one data or I/O line. The CSP design results in lower inductance, virtually eliminating voltage overshoot due to leads and interconnecting bond wires. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (15kV air, 8kV contact discharge).

Features

- 350 Watts peak pulse power (tp = 8/20µs)
- Transient protection for data lines to
  IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 24A (8/20µs)
- Small chip scale package requires less board space
- Low profile (< 0.60mm)
- No need for underfill material
- Bidirectional protection
- Low clamping voltage
- Working voltage: 5V
- Solid-state silicon-avalanche technology

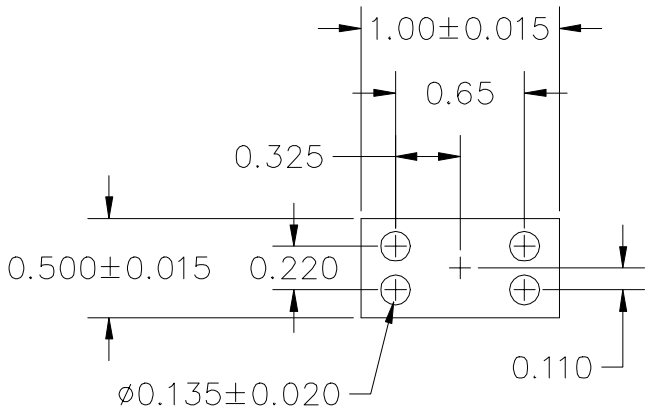
Mechanical Characteristics

- Marking : Marking Code
- Packaging : Tape and Reel

Applications

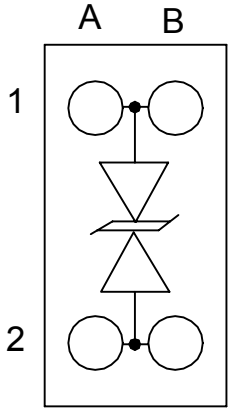
- Cell Phone Handsets and Accessories
- Personal Digital Assistants (PDA's)
- Notebook & Hand Held Computers
- Portable Instrumentation
- Pagers
- Smart Cards
- MP3 Players

Device Dimensions



SFC05C-1 Maximum Dimensions (mm)

Schematic & PIN Configuration



CSP TVS (Bottom View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	350	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	24	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	>25 >15	kV
Soldering Temperature	T_L	260 (10 seconds)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

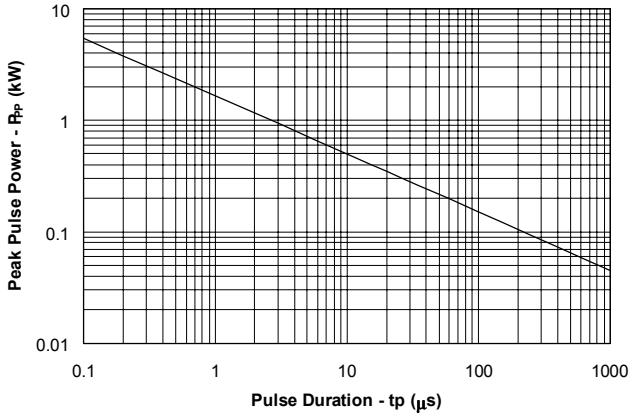
Electrical Characteristics

SFC05C-1 for 5V Bidirectional Line

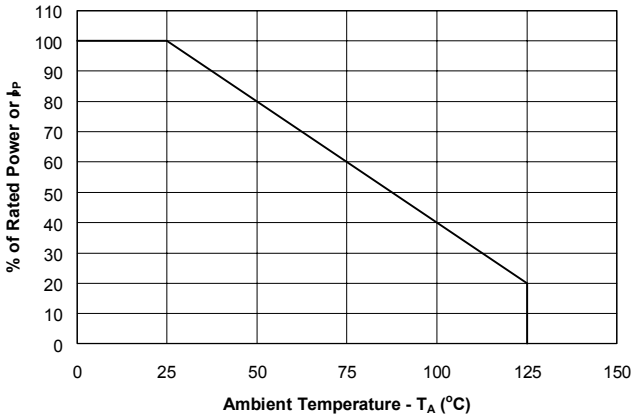
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C			10	µA
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs			9.8	V
Clamping Voltage	V_C	I_{PP} = 24A, tp = 8/20µs			14.5	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz		260	350	pF

Typical Characteristics

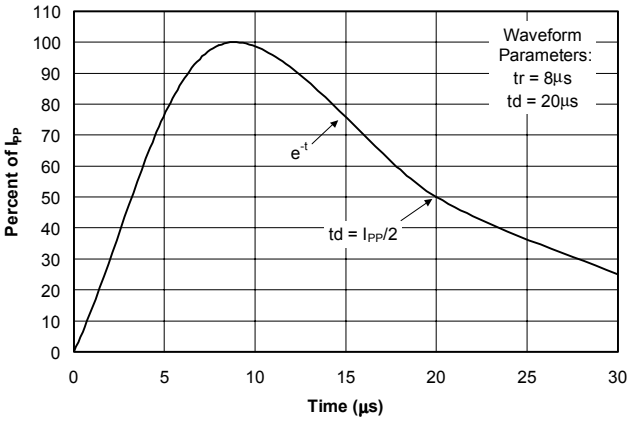
Non-Repetitive Peak Pulse Power vs. Pulse Time



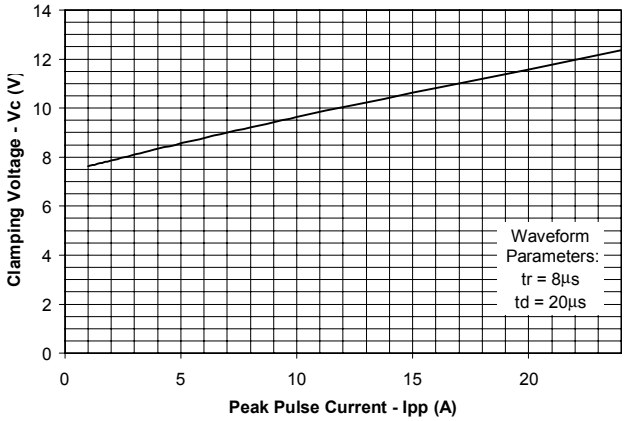
Power Derating Curve



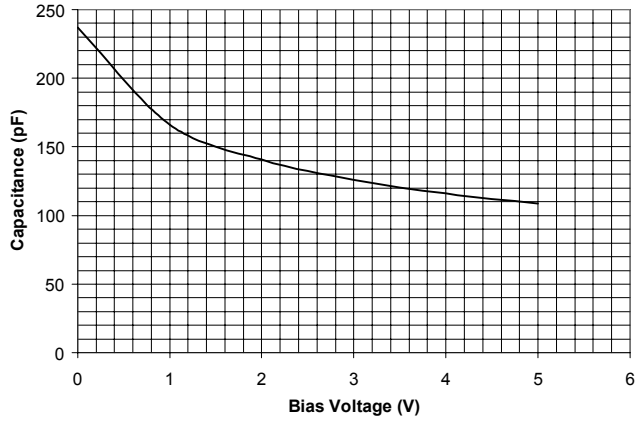
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



Capacitance vs. Reverse Voltage



Applications Information

Device Connection Options

The SFC05C-1 is symmetrical therefore no device orientation is necessary. The line that is to be protected is connected to one side of the device and the other side is connected to ground (common mode protection). All path lengths should be kept as short as possible.

Wafer Level CSP TVS

CSP TVS devices are wafer level chip scale packages. They eliminate external plastic packages and leads and thus result in a significant board space savings. Manufacturing costs are minimized since they do not require an intermediate level interconnect or interposer layer for reliable operation. Certain precautions and design considerations have to be observed however for maximum solder joint reliability. These include solder pad definition, board finish, and assembly parameters.

Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting the SFC05C-1. Solder mask defined (SMD) pads produce stress points near the solder mask on the PCB side that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is 0.370 x 0.200mm with a solder mask opening of 0.520 x 0.350mm.

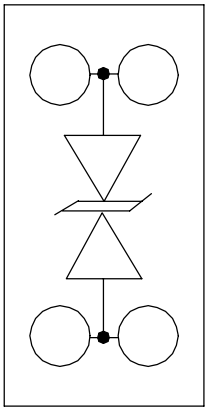
Printed Circuit Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided.

Reflow Profile

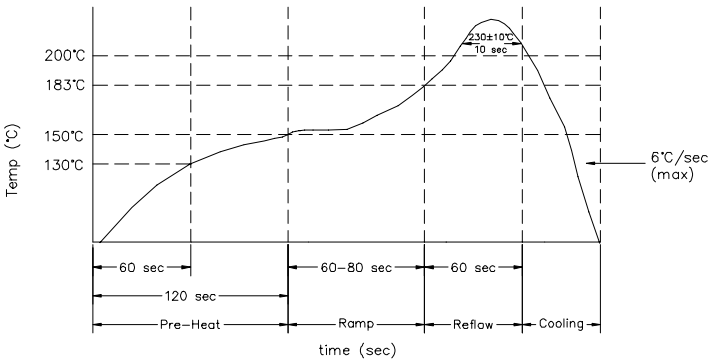
The flip chip TVS can be assembled using standard SMT reflow processes. As with any component, thermal profiles at specific board locations can vary & must be determined by the manufacturer. The flip chip TVS peak reflow temperature is 230 ± 10 °C, but the device can withstand up to 260 °C peak reflow temperature. Time above eutectic temperature (183 °C) should be 50 ± 10 seconds. During reflow, the component self-aligns itself on the pad.

Device Schematic & Pin Configuration



Bottom View

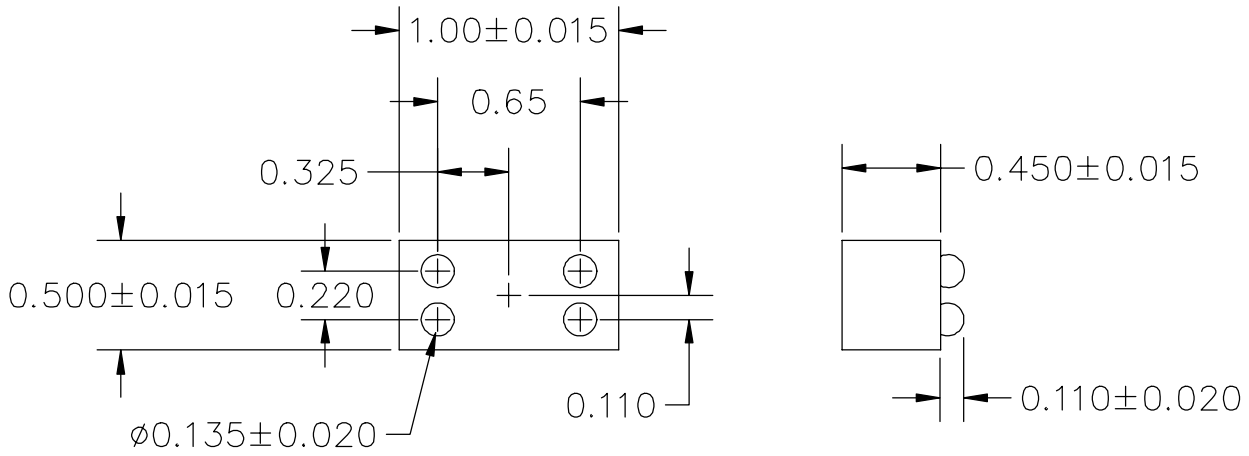
Reflow Profile



Typical solder reflow profile for OSP finish FR–4 bond.

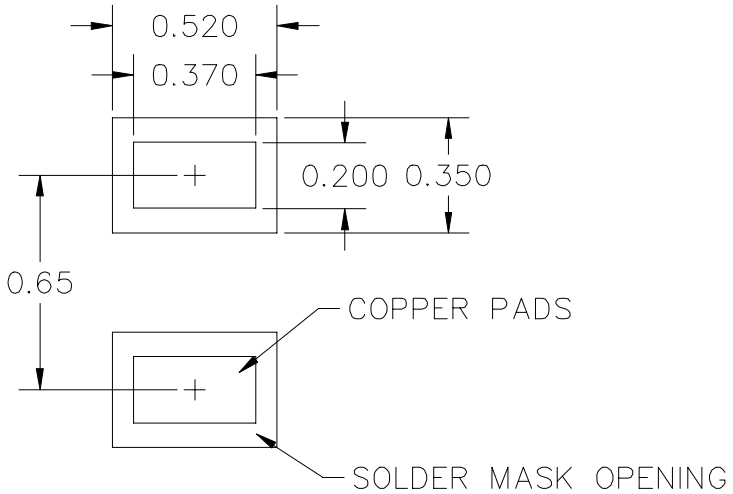
Pre–heat to 150°C	120 sec max
Time to eutectic (183°C)	60–80 sec
Time above eutectic	50±10 sec
Peak reflow temp	230±10°C
Time w/in 10°C of peak	10 seconds
Ramp down rate	6°C/sec max

Outline Drawing



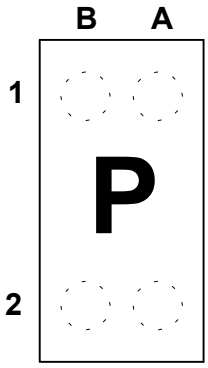
DIMENSIONS ARE IN MILLIMETERS

Land Pattern



Marking Codes

Part Number	Marking Code
SFC05C-1	P



2 x 2 Grid Flip, 0.65mm Pitch Chip TVS (Top View)

Ordering Information

Part Number	Working Voltage	Qty per Reel	Reel Size
SFC05C-1.TC	5V	3000	7 Inch

Contact Information

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