EPSON

Micro MINI S1C60N09

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- S1C6200B Core CPU
- Low Voltage and Low Power
- Built-in LCD Driver
- Low Cost Performance

■ DESCRIPTION

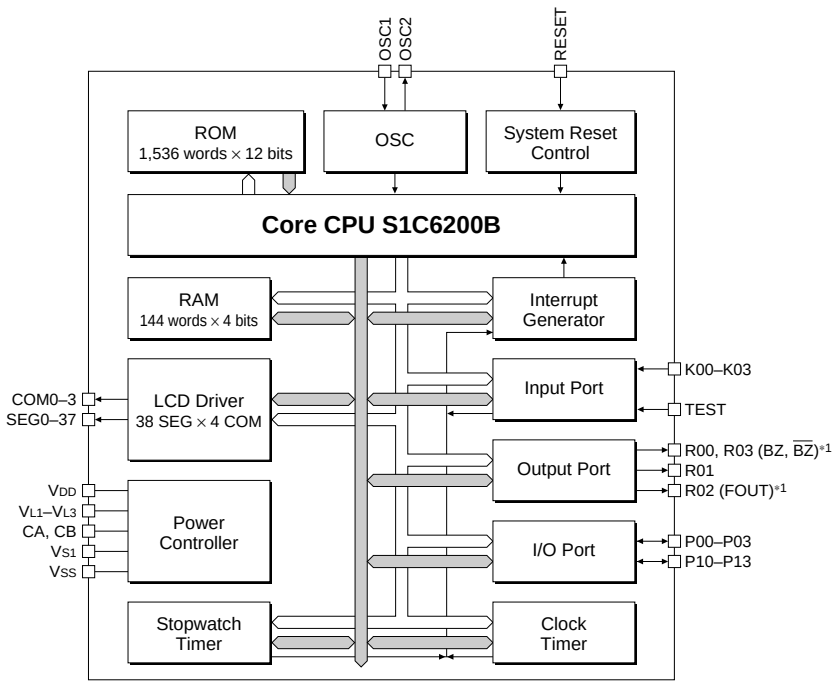
The S1C60N09 Series single-chip microcomputer features an S1C6200B CMOS 4-bit CPU as the core. It contains a 1,536 (words) × 12 (bits) ROM, 144 (words) × 4 (bits) RAM, LCD driver, 4-bit input port (K00–K03), 4-bit output port (R00–R03), 8-bit I/O port (P00–P03, P10–P13) and timers.
The S1C60N09 Series is configured as follows, depending on the supply voltage.

S1C60N09: 3.0 V (2.6 to 3.6 V)
S1C60L09: 1.5 V (1.2 to 1.8 V)

■ FEATURES

- Core CPU S1C6200B
- Built-in oscillation circuit ..... Crystal 32.768 kHz (Typ.) or CR oscillation circuit 65 kHz (Typ.)
- Instruction set ..... 100 instructions
- ROM capacity ..... 1,536 words × 12 bits
- RAM capacity ..... 144 words × 4 bits
- Input port ..... 4 bits (pull-down resistors are available by mask option)
- Output port ..... 4 bits (clock and buzzer outputs are selectable by mask option)
- I/O port ..... 8 bits
- LCD driver ..... 38 segments × 4, 3 or 2 commons
  (1/4, 1/3 or 1/2 duty are selectable by mask option)
- Time base counter ..... 2 systems (clock timer and stopwatch timer) built-in
- Interrupt ..... External: Input port interrupt 1 system
  Internal: Timer interrupt 2 systems
- Supply voltage ..... 1.5 V (1.2 to 1.8 V) S1C60L09
  3.0 V (2.6 to 3.6 V) S1C60N09
- Current consumption (Typ.) ..... During HALT: 1.0 µA (32 kHz crystal oscillation)
  During execution: 3.0 µA (32 kHz crystal oscillation)
- Supply form ..... Die form only

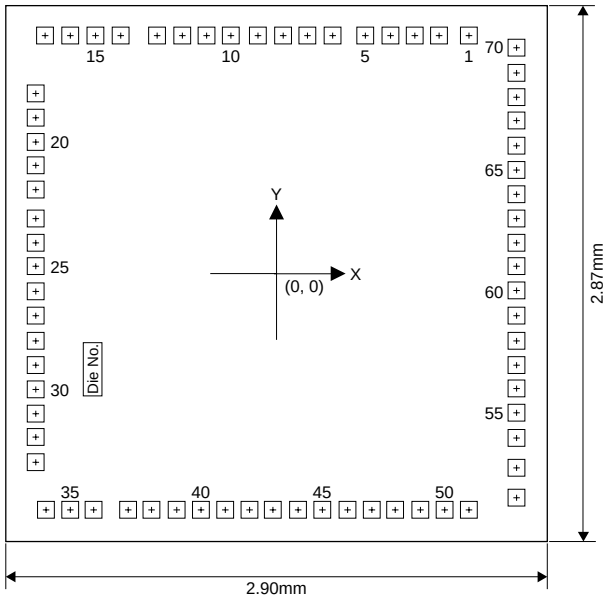
■ BLOCK DIAGRAM



*1: Terminal specifications can be selected by mask option.

■ PAD LAYOUT

Pad Layout Diagram



Chip thickness: 400µm
Pad opening: 95µm

Pad Coordinates (Unit: µm)

No.	Pad name	X	Y	No.	Pad name	X	Y
1	SEG37	1,020	1,268	36	SEG3	-977	-1,268
2	K03	861	1,268	37	SEG4	-795	-1,268
3	K02	731	1,268	38	SEG5	-665	-1,268
4	K01	601	1,268	39	SEG6	-535	-1,268
5	K00	471	1,268	40	SEG7	-405	-1,268
6	P13	297	1,268	41	SEG8	-275	-1,268
7	P12	167	1,268	42	SEG9	-145	-1,268
8	P11	37	1,268	43	SEG10	-15	-1,268
9	P10	-93	1,268	44	SEG11	115	-1,268
10	P03	-246	1,268	45	SEG12	245	-1,268
11	P02	-376	1,268	46	SEG13	375	-1,268
12	P01	-507	1,268	47	SEG14	505	-1,268
13	P00	-637	1,268	48	SEG15	635	-1,268
14	R02	-835	1,268	49	SEG16	765	-1,268
15	R01	-969	1,268	50	SEG17	895	-1,268
16	R00	-1,102	1,268	51	SEG18	1,025	-1,268
17	R03	-1,236	1,268	52	SEG19	1,284	-1,196
18	VSS	-1,284	965	53	TEST	1,284	-1,037
19	RESET	-1,284	835	54	SEG20	1,284	-879
20	VS1	-1,284	705	55	SEG21	1,284	-749
21	OSC2	-1,284	575	56	SEG22	1,284	-619
22	OSC1	-1,284	445	57	SEG23	1,284	-489
23	VDD	-1,284	286	58	SEG24	1,284	-359
24	VL3	-1,284	156	59	SEG25	1,284	-229
25	VL2	-1,284	26	60	SEG26	1,284	-99
26	VL1	-1,284	-104	61	SEG27	1,284	32
27	CB	-1,284	-234	62	SEG28	1,284	162
28	CA	-1,284	-364	63	SEG29	1,284	292
29	COM3	-1,284	-494	64	SEG30	1,284	422
30	COM2	-1,284	-624	65	SEG31	1,284	552
31	COM1	-1,284	-754	66	SEG32	1,284	682
32	COM0	-1,284	-884	67	SEG33	1,284	812
33	SEG0	-1,284	-1,014	68	SEG34	1,284	942
34	SEG1	-1,237	-1,268	69	SEG35	1,284	1,072
35	SEG2	-1,107	-1,268	70	SEG36	1,284	1,202

■ PAD DESCRIPTION

Pad name	Pad No.	I/O	Function
V_{DD}	23	(I)	Power supply terminal (+)
V_{SS}	18	(I)	Power supply terminal (-)
V_{S1}	20	–	Constant voltage output terminal
$V_{L1–3}$	26–24	–	Power source for LCD
CA, CB	28, 27	–	Booster capacitor connecting terminal
OSC1	22	I	Crystal or CR oscillation input terminal *
OSC2	21	O	Crystal or CR oscillation output terminal *
K00–03	5–2	I	Input port terminal
P00–03	13–10	I/O	I/O port terminal
P10–13	9–6	I/O	I/O port terminal
R00	16	O	Output port terminal (BZ output is selectable *)
R03	17	O	Output port terminal ($\overline{BZ}$ output is selectable *)
R01	15	O	Output port terminal
R02	14	O	Output port terminal (FOUT output is selectable *)
SEG0–37	33–52, 54–70, 1	O	LCD segment output (DC output is selectable *)
COM0–3	32–29	O	LCD common output terminal (1/4, 1/3 or 1/2 duty are selectable *)
RESET	19	I	Initial reset input terminal
TEST	53	I	Test input terminal

* Can be selected by mask option

■ OPTION LIST

1. DEVICE TYPE
   - ☐ 1. E0C6009 (S1C60N09) LCD 3 V
   - ☐ 2. E0C6009 (S1C60N09) LCD 4.5 V
   - ☐ 3. E0C60L09 (S1C60L09) LCD 3 V
   - ☐ 4. E0C60L09 (S1C60L09) LCD 4.5 V

2. OSC1 SYSTEM CLOCK
   - ☐ 1. Crystal
   - ☐ 2. CR

3. MULTIPLE KEY ENTRY RESET
   - • KEY COMBINATION ..... ☐ 1. Not Use
   - ☐ 2. Use K00, K01
   - ☐ 3. Use K00, K01, K02
   - ☐ 4. Use K00, K01, K02, K03

4. INTERRUPT NOISE REJECTOR K00–K03
   - ☐ 1. Use
   - ☐ 2. Not Use

5. INPUT PORT PULL DOWN RESISTOR
   - • K00 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - • K01 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - • K02 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - • K03 ..... ☐ 1. With Resistor ☐ 2. Gate Direct

6. R00 SPECIFICATION
   - • R00 OUTPUT SPECIFICATION .. ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - • R00 OUTPUT TYPE ..... ☐ 1. DC Output ☐ 2. Buzzer Output

7. R01 SPECIFICATION
   - • R01 OUTPUT SPECIFICATION .. ☐ 1. Complementary ☐ 2. Pch-OpenDrain

8. R02 SPECIFICATION
   - R02 OUTPUT SPECIFICATION .. ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - R02 OUTPUT TYPE ..... ☐ 1. DC Output
     ☐ 2. FOSC1
     ☐ 3. FOSC1/2
     ☐ 4. FOSC1/4
     ☐ 5. FOSC1/8
     ☐ 6. FOSC1/16
     ☐ 7. FOSC1/32
     ☐ 8. FOSC1/64
     ☐ 9. FOSC1/128

9. R03 SPECIFICATION
   - R03 OUTPUT SPECIFICATION .. ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - R03 OUTPUT TYPE ..... ☐ 1. DC Output
     ☐ 2. Buzzer Output (R00 control)
     ☐ 3. Buzzer Output (R03 control)

10. I/O PORT SPECIFICATION
   - P00 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - P01 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - P02 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - P03 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - P10 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - P11 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - P12 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain
   - P13 ..... ☐ 1. Complementary ☐ 2. Pch-OpenDrain

11. I/O PORT PULL DOWN RESISTOR
   - P00 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - P01 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - P02 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - P03 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - P10 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - P11 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - P12 ..... ☐ 1. With Resistor ☐ 2. Gate Direct
   - P13 ..... ☐ 1. With Resistor ☐ 2. Gate Direct

12. I/O PORT FUNCTION
   - P00 ..... ☐ 1. I/O Port ☐ 2. Output Port
   - P01 ..... ☐ 1. I/O Port ☐ 2. Output Port
   - P02 ..... ☐ 1. I/O Port ☐ 2. Output Port
   - P03 ..... ☐ 1. I/O Port ☐ 2. Output Port
   - P10 ..... ☐ 1. I/O Port ☐ 2. Output Port
   - P11 ..... ☐ 1. I/O Port ☐ 2. Output Port
   - P12 ..... ☐ 1. I/O Port ☐ 2. Output Port
   - P13 ..... ☐ 1. I/O Port ☐ 2. Output Port

13. LCD COMMON DUTY AND BIAS
     ☐ 1. 1/4 Duty, 1/3 Bias (when 4.5 V LCD is selected in Option 1)
     ☐ 2. 1/3 Duty, 1/3 Bias
     ☐ 3. 1/2 Duty, 1/3 Bias

     ☐ 1. 1/4 Duty, 1/2 Bias (when 3 V LCD is selected in Option 1)
     ☐ 2. 1/3 Duty, 1/2 Bias
     ☐ 3. 1/2 Duty, 1/2 Bias

14. SEGMENT MEMORY ADDRESS
     ☐ 1. 40H–6FH ☐ 2. C0H–EFH

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

S1C60N09

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-5.5 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–

S1C60L09

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-2.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–

● Recommended Operating Conditions

S1C60N09

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.6	-3.0	-2.6	V
Oscillation frequency	fosc	Crystal oscillation		32.768		kHz
		CR oscillation, R_{CR}=475kΩ		65	80	kHz
Booster capacitor	C_1		0.1			µF
Capacitor between V_{DD} and V_{S1}	C_3 or C_4*1		0.1			µF

*1: Depends on the LCD specification.

S1C60L09

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-1.8	-1.5	-1.2	V
Oscillation frequency	fosc	Crystal oscillation		32.768		kHz
		CR oscillation, R_{CR}=475kΩ		65	80	kHz
Booster capacitor	C_1		0.1			µF
Capacitor between V_{DD} and V_{S1}	C_3 or C_4*1		0.1			µF

*1: Depends on the LCD specification.

● DC Characteristics

S1C60N09

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, fosc=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03, P10–13	0.2·V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.1·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03, P10–13	V_{SS}		0.8·V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.9·V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V, No pull-down	K00–03, P00–03, P10–13	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V, Pull-down	K00–03	4		40	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V, Pull-down	P00–03, P10–13 RESET, TEST	50		200	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, P00–03, P10–13 RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R00, R03			-1.8	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	R01, R02, P00–03, P10–13			-0.9	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R00, R03	4.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	R01, R02, P00–03, P10–13	3.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–37			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1·V_{SS}	SEG0–37			-200	µA
	I_{OL5}	V_{OL5}=0.9·V_{SS}		200			µA

S1C60L09

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, fosc=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, P00–03, P10–13	0.2·V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.1·V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03, P00–03, P10–13	V_{SS}		0.8·V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.9·V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V, No pull-down	K00–03, P00–03, P10–13	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V, Pull-down	K00–03	2		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V, Pull-down	P00–03, P10–13 RESET, TEST	25		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–03, P00–03, P10–13 RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1·V_{SS}	R00, R03			-300	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1·V_{SS}	R01, R02, P00–03, P10–13			-150	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9·V_{SS}	R00, R03	1400			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9·V_{SS}	R01, R02, P00–03, P10–13	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–37			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1·V_{SS}	SEG0–37			-100	µA
	I_{OL5}	V_{OL5}=0.9·V_{SS}		100			µA

● Analog Circuit Characteristics and Current Consumption

S1C60N09 (Crystal Oscillation)

• 4.5 V LCD panel, 1/4, 1/3, 1/2 duty, 1/3 bias (V_{L2} is shorted to V_{SS} inside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.9	V
Current consumption	I_{OP}	During HALT	Without		1.0	2.5	µA
		During execution	panel load		2.5	5.0	µA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L2} - 0.1		1/2·V_{L2} ×0.85	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3/2·V_{L2} - 0.1		3/2·V_{L2} ×0.85	V
Current consumption	I_{OP}	During HALT	Without		2.0	5.5	µA
		During execution	panel load		5.5	10.0	µA

• 3 V LCD panel, 1/4, 1/3, 1/2 duty, 1/2 bias (V_{L3} is shorted to V_{SS} inside the IC and V_{L1} is shorted to V_{L2} outside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L3} - 0.1		1/2·V_{L3} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		1/2·V_{L3} - 0.1		1/2·V_{L3} ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)			V_{SS}		V
Current consumption	I_{OP}	During HALT	Without		1.0	2.5	µA
		During execution	panel load		2.5	5.0	µA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L3} - 0.1		1/2·V_{L3} ×0.85	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		1/2·V_{L3} - 0.1		1/2·V_{L3} ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)			V_{SS}		V
Current consumption	I_{OP}	During HALT	Without		2.0	5.5	µA
		During execution	panel load		5.5	10.0	µA

S1C60L09 (Crystal Oscillation)

• 4.5 V LCD panel, 1/4, 1/3, 1/2 duty, 1/3 bias (V_{L1} is shorted to V_{SS} inside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.9	V
Current consumption	I_{OP}	During HALT	Without		1.0	2.5	µA
		During execution	panel load		2.5	5.0	µA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.85	V
Current consumption	I_{OP}	During HALT	Without		2.0	5.5	µA
		During execution	panel load		5.5	10.0	µA

• 3 V LCD panel, 1/4, 1/3, 1/2 duty, 1/2 bias (V_{L1} is shorted to V_{SS} inside the IC and V_{L1} is shorted to V_{L2} outside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
Current consumption	I_{OP}	During HALT	Without panel load		1.0	2.5	µA
		During execution			2.5	5.0	µA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.85	V
Current consumption	I_{OP}	During HALT	Without panel load		2.0	5.5	µA
		During execution			5.5	10.0	µA

S1C60N09 (CR Oscillation)

• 4.5 V LCD panel, 1/4, 1/3, 1/2 duty, 1/3 bias (V_{L2} is shorted to V_{SS} inside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L2}$ - 0.1		$1/2 \cdot V_{L2}$ ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3/2 \cdot V_{L2}$ - 0.1		$3/2 \cdot V_{L2}$ ×0.9	V
Current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	µA
		During execution			15.0	20.0	µA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		$1/2 \cdot V_{L2}$ - 0.1		$1/2 \cdot V_{L2}$ ×0.85	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$3/2 \cdot V_{L2}$ - 0.1		$3/2 \cdot V_{L2}$ ×0.85	V
Current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	µA
		During execution			30.0	40.0	µA

• 3 V LCD panel, 1/4, 1/3, 1/2 duty, 1/2 bias (V_{L3} is shorted to V_{SS} inside the IC and V_{L1} is shorted to V_{L2} outside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L3} - 0.1		1/2·V_{L3} ×0.9	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		1/2·V_{L3} - 0.1		1/2·V_{L3} ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)			V_{SS}		V
Current consumption	I_{OP}	During HALT	Without		8.0	15.0	µA
		During execution	panel load		15.0	20.0	µA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)		1/2·V_{L3} - 0.1		1/2·V_{L3} ×0.85	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		1/2·V_{L3} - 0.1		1/2·V_{L3} ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)			V_{SS}		V
Current consumption	I_{OP}	During HALT	Without		16.0	30.0	µA
		During execution	panel load		30.0	40.0	µA

S1C60L09 (CR Oscillation)

• 4.5 V LCD panel, 1/4, 1/3, 1/2 duty, 1/3 bias (V_{L1} is shorted to V_{SS} inside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.9	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.9	V
Current consumption	I_{OP}	During HALT	Without		8.0	15.0	µA
		During execution	panel load		15.0	20.0	µA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_4=0.1µF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2·V_{L1} - 0.1		2·V_{L1} ×0.85	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3·V_{L1} - 0.1		3·V_{L1} ×0.85	V
Current consumption	I_{OP}	During HALT	Without		16.0	30.0	µA
		During execution	panel load		30.0	40.0	µA

• 3 V LCD panel, 1/4, 1/3, 1/2 duty, 1/2 bias (V_{L1} is shorted to V_{SS} inside the IC and V_{L1} is shorted to V_{L2} outside the IC)

<Normal mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.9	V
Current consumption	I_{OP}	During HALT	Without panel load		8.0	15.0	µA
		During execution			15.0	20.0	µA

<Heavy load protection mode>

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=65kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C_1–C_3=0.1µF, R_{CR}=475kΩ)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} (without panel load)			V_{SS}		V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} (without panel load)			V_{SS}		V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} (without panel load)		$2 \cdot V_{L1}$ - 0.1		$2 \cdot V_{L1}$ ×0.85	V
Current consumption	I_{OP}	During HALT	Without panel load		16.0	30.0	µA
		During execution			30.0	40.0	µA

● Oscillation Characteristics

Oscillation characteristics will vary according to different conditions (elements used, boad pattern). Use the following characteristics are as reference values.

S1C60N09 Crystal Oscillation

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC}=32.768kHz, Crystal: Q13MC146, C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-2.6			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-2.6			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.6 to -3.6V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-3.6	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

S1C60L09 Crystal Oscillation

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC}=32.768kHz, Crystal: Q13MC146, C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (V_{SS})	-1.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{SS})	-1.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the chip		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.2 to -1.8V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-1.8	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

S1C60N09 CR Oscillation

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=475kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC}		45.5	65	84.5	kHz
Oscillation start time	tsta	V_{SS}=-2.6 to -3.6V			3	mS

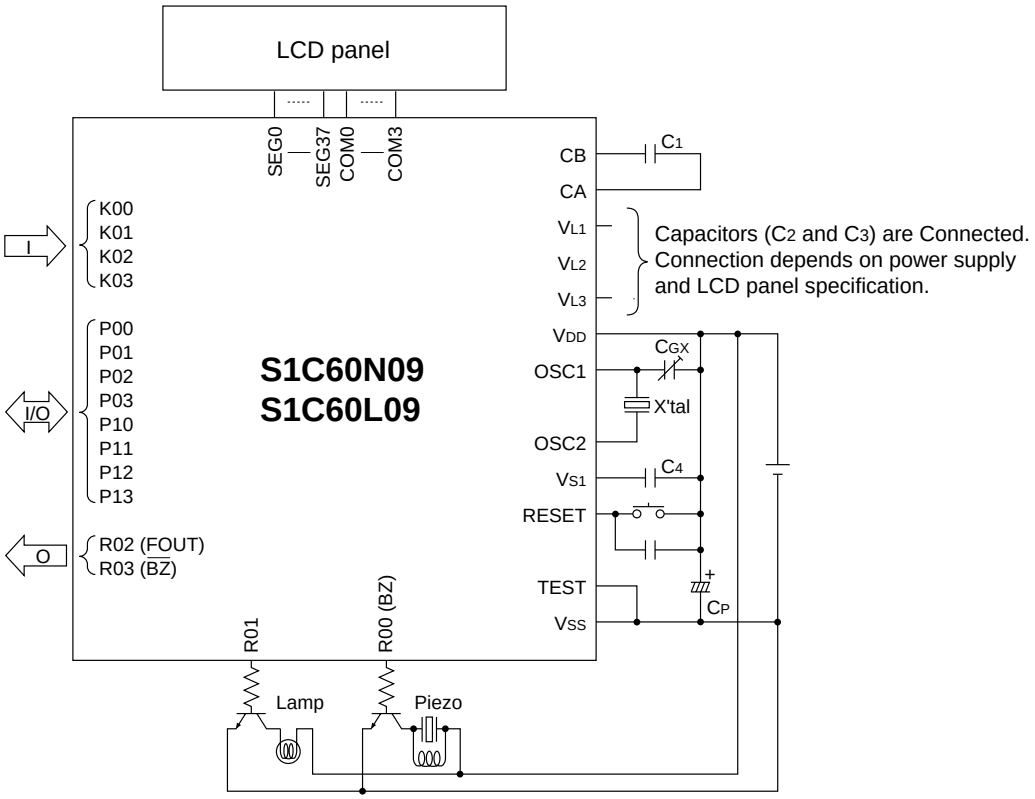
S1C60L09 CR Oscillation

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, R_{CR}=475kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC}		45.5	65	84.5	kHz
Oscillation start time	tsta	V_{SS}=-1.2 to -1.8V			3	mS

■ BASIC EXTERNAL CONNECTION DIAGRAM

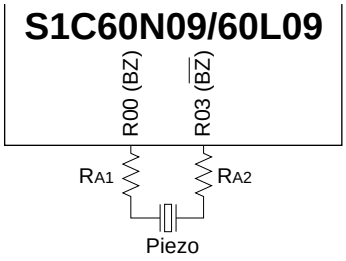
Piezo Buzzer Single Terminal Driving



X'tal	Crystal oscillator	32.768 kHz, C_I = 35 kΩ
C_{GX}	Trimmer capacitor	5–25 pF
C_1	Capacitor	0.1 µF
C_2	Capacitor	0.1 µF
C_3	Capacitor	0.1 µF
C_4	Capacitor	0.1 µF
C_P	Capacitor	3.3 µF

Note: The above table is simply an example, and is not guaranteed to work.

Piezo Buzzer Direct Driving



R_{A1}	Protection resistor	100 Ω
R_{A2}	Protection resistor	100 Ω

When driving the buzzer, set the IC into the heavy load protection mode since the supply voltage changes according to the buzzer frequency.

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