SH66L08

1K 4-bit Microcontroller with LCD Driver

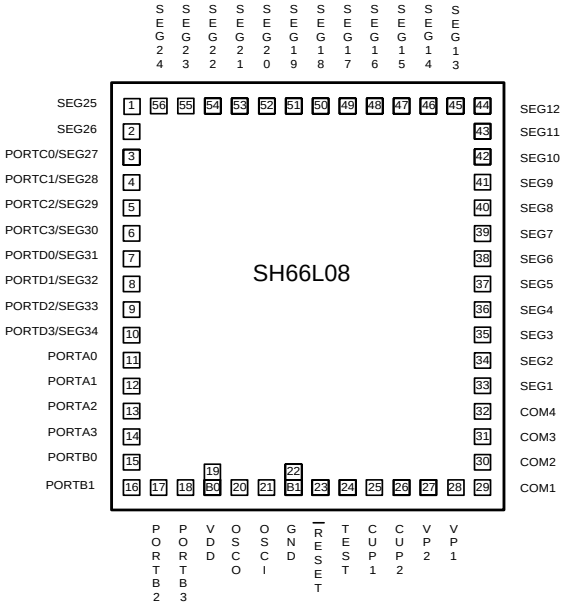
Features

- SH6610C-based single-chip 4-bit microcontroller with LCD driver
- ROM: 1024 X 16 bits
- RAM: 256 X 4 bits (data memory)
- Operation Voltage Range: 1.2V - 1.7V
- 16 CMOS I/O pins (PORTC, D can switch to segment)
- 4 level subroutine nesting (including interrupts)
- Two 8-bit timers with pre-divider circuit
- Oscillator warm-up timer
- 4 priority interrupt sources:
  - External interrupt (falling edge)
  - Timer0 interrupt
  - Timer1 interrupt
  - PortB & PortC interrupt (falling edge)
- Clock source: 32.768KHz crystal or 131K RC (type is selected by code option)
- Instruction cycle time:
  4/32.768KHz (≈ 122μs) for 32.768KHz crystal
  4/131KHz (≈ 31μs) for 131KHz RC
- LCD driver: 4 X 34 (1/4 duty, 1/3 bias or 1/3 duty, 1/2 bias, 8 segment shared with PORTC, D)
- Built-in voltage doubler and tripler charge pump circuit
- Built-in alarm generator (carrier frequency: 2KHz or 4KHz. Selected by code option)
- Two low power operation modes - HALT or STOP mode
- Low power consumption
- Bonding option for multi-code software
- Available in CHIP FORM

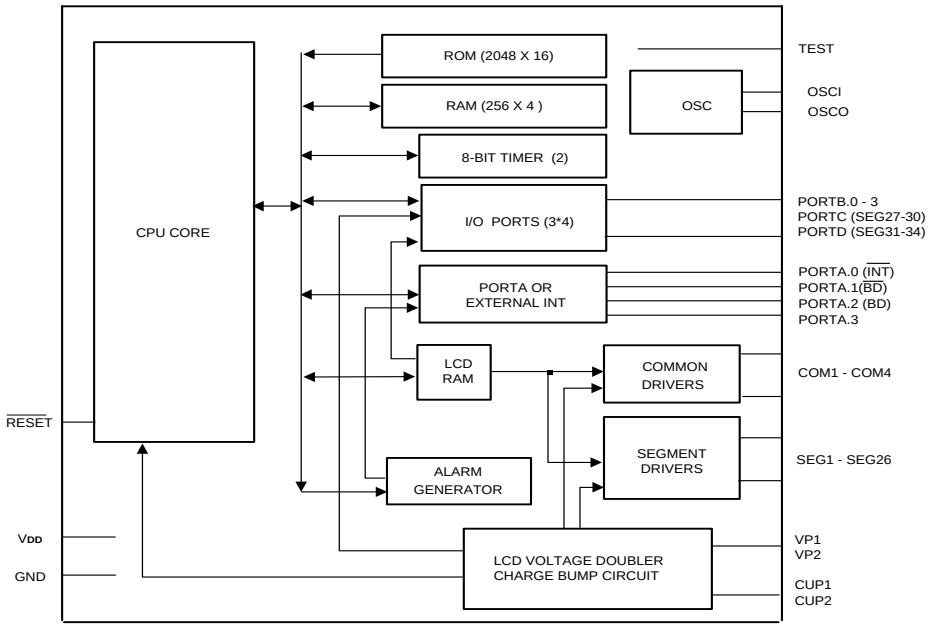
General Description

SH66L08 is a single-chip microcontroller integrated with an SH6610C CPU core, SRAM, timer, alarm generator, LCD driver, I/O port, voltage pump and program ROM.

Pad Configuration



Block Diagram



Pad Description (Total 58 pads for mask type)

Pad No.	Designation	I/O	Description
33 - 56,1 - 2	SEG1 - 26	O	Segment signal output for LCD display
29 - 32	COM1 - 4	O	Common signal output for LCD display
28, 27	VP1, VP2	P	Power supply pin for LCD driver
25, 26	CUP1 - 2	P	Connection for voltage doubler capacitor
24	TEST	I	Test pin internally pull-down. (No connect for user)
23	$\overline{\text{RESET}}$	I	Pad reset input
19	V_{DD}	P	Power supply pin for CPU
19	B0	I	Bonding option, internally pull-low
22	B1	I	Bonding option, internally pull-high
22	GND	P	Ground pin
20	OSCO	O	Oscillator output pin, connected to crystal oscillator
21	OSCI	I	Oscillator input pin, connected to crystal or external resistor
11 - 14	PORTA0 - 3	I/O	Bit programmable I/O, PA.0 could be external interrupt input ($\overline{\text{INT}}$) PA.1, PA.2 could be buzzer output PA.1 (BD), PA.2 ($\overline{\text{BD}}$)
15 - 18	PORTB0 - 3	I/O	Bit programmable I/O, vector interrupt (active falling edge)
3 - 6	PORTC0 - 3	I/O	Bit programmable I/O, Vector interrupt (active falling edge) Shared with SEG27 - 30
7 - 10	PORTD0 - 3	I/O	Bit programmable I/O. shared with SEG31 - 34

Functional Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and the Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 2K program ROM. It consists of 11-bits: the Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BNC),

(2) When executing a subroutine call instruction (CALL),

(3) When an interrupt occurs,

(4) When the chip is in the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)

Decision (BA0, BA1, BA2, BA3, BNZ, BNC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow which the arithmetic operation generates. During an interrupt servicing or call instruction, the carry flag is pushed into the stack and retrieved back from the stack by the RTNI instruction. It is unaffected by RTNW instruction.

1.3. Accumulator

The Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data transfer between the accumulator and system register or data memory can be performed.

1.4. Stack

A group of registers is used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt. It is organized into 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of the Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). The stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceed 4, and the bottom of the stack will be shifted out.

2. ROM

The ROM can address 1024 words X 16 bits of program area from $000 to $3FF.
There is an area from address $0 through $4 that is reserved for special interrupt service routines, such as starting at vector address.

Address	Instruction	Remarks
000H	JMP Instruction	Jump to RESET service routine
001H	JMP Instruction	Jump to External interrupt service routine
002H	JMP Instruction	Jump to TIMER0 service routine
003H	JMP Instruction	Jump to TIMER1 service routine
004H	JMP Instruction	Jump to PB service routine (PORTB)

*JMP instruction can be replaced by any instruction.

3. RAM

Built-in RAM contains of general-purpose data memory, LCD RAM, and system register.

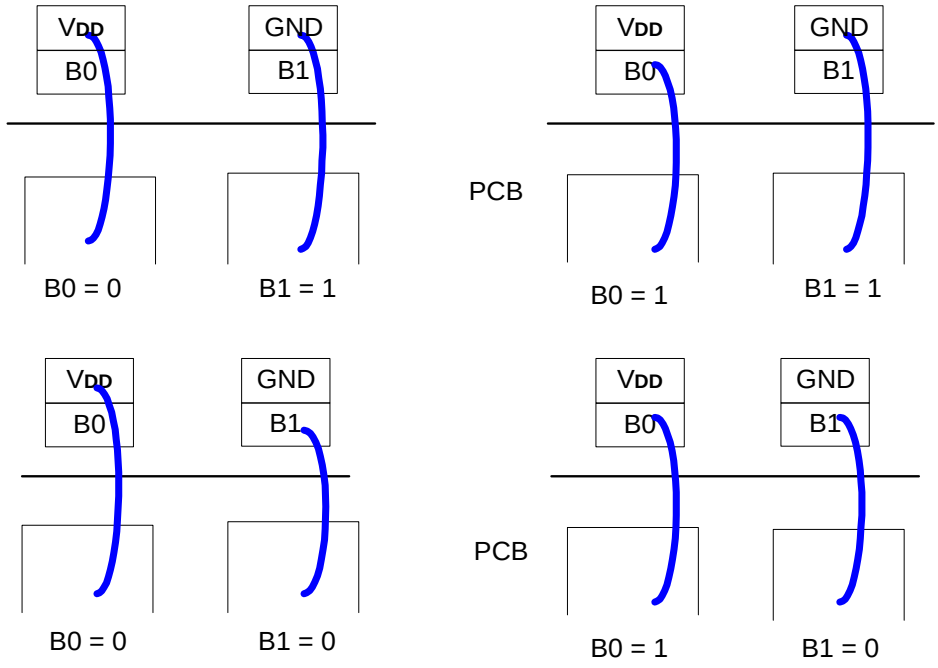
The following is the memory allocation map:
$000 - $01F: System register and I/O
$020 - $11F: Data memory (256 X 4 bits, divided into 2 banks)
$300 - $321: LCD RAM space (34 X 4 bits)

The Configuration of System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power on
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags	0000
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags	0000
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit0-2: Timer0 Mode register	000
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit0-2: Timer1 Mode register	000
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load / counter register low nibble	0000
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load / counter register high nibble	0000
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load / counter register low nibble	0000
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load / counter register high nibble	0000
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA	0000
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB	0000
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC	0000
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD	0000
$0C	-	-	-	-	-	Reserved	-
$0D	-	-	B1	B0	R	Bit0, 1: Bonding option	10
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register	-
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register	-
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble	-
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble	-
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble	-
$13	-	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as Alarm O/P Bit1: HEAVY LOAD Mode Bit2: LCD off	- 100
$14	AEC3	AEC2	AEC1	AEC0	R/W	Alarm Envelope Control	0000
$15	PPULL	O/S2	O/S1	-	R/W	Bit1: set PORTC as LCD segment output Bit2: set PORTD as LCD segment output Bit3: Port pull-up control	000 -
$16	-	-	-	-	-	Reserved	-
$17	-	-	-	-	-	Reserved	-
$18	-	-	-	-	-	Reserved	-
$19	-	-	-	-	-	Reserved	-
$1A	-	-	-	-	-	Reserved	-
$1B	PACR.3	PACR.2	PACR.1	PACR.0	R/W	Set PORTA to be output port	0000
$1C	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	Set PORTB to be output port	0000
$1D	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	Set PORTC to be output port	0000
$1E	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	Set PORTD to be output port	0000
$1F	-	-	-	-	-	Reserved	-

System Register 0DH

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power-on
$0DH	-	-	B1	B0	R	Bit0: Bonding option 0, internal weak drive Bit1: Bonding option 1, internal weak drive	Pull low Pull high
	X	X	1	0			Yes
	X	X	0	0		B1 bond to GND	
	X	X	1	1		B0 bond to VDD	
	X	X	0	1		B1 bond to GND & B0 bond to VDD	



SH66L08 Bonding Option

Up to 4 different bonding options are possible for the user's needs. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

System Register 13

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power on
$13	-	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as ALARM output Bit1: heavy load mode Bit2: LCD Power Control	100
	X	X	X	0		PORTA.1, PORTA.2 as I/O port	Yes
	X	X	X	1		PORTA.1, PORTA.2 as ALARM output	
	X	X	0	X		No heavy load	Yes
	X	X	1	X		HEAVY LOAD mode	
	X	0	X	X		LCD signal on, pump on	
	X	1	X	X		LCD signal off	Yes

HEAVY LOAD Mode (HLM): This mode is designed for the 32KHz crystal oscillator, so that the oscillation can be maintained in a noisy power environment. The power might drop suddenly when the ALARM is driving a speaker. The HLM is designed to control this power variation. The consumption of power will increase during the use of the HLM mode, but it will not affect the RC oscillator.

Notice:

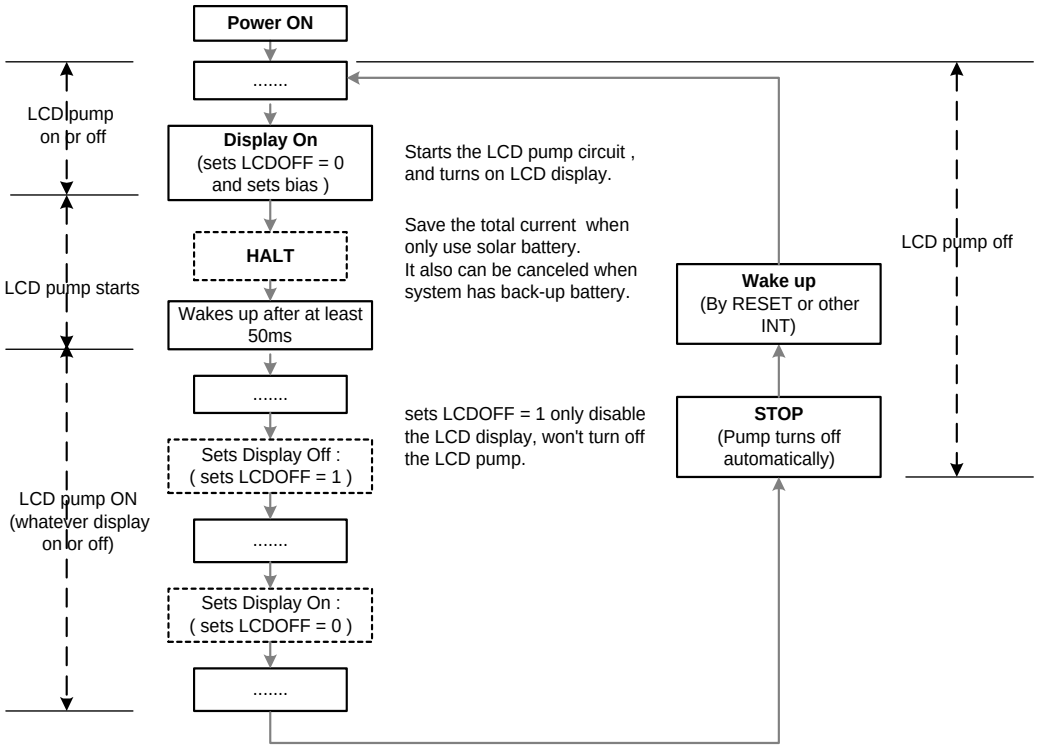
The LCDOFF (system register 13H bit2) will set to 1 when reset, and the LCD display will be disabled.

The LCD pump circuit may be on or off after power on reset. When LCDOFF (system register 13H bit2) is cleared to 1, the LCD pump circuit will turn on. It will turns off only after receiving a “STOP” instruction.

Set LCDOFF = 1 disables LCD display output only, and won’t turn off the LCD pump circuit.

When SH66L08 runs into STOP mode, the LCD pump circuit turns off automatically. The user should turn on the LCD pump (set LCDOFF = 0) after the next wake up.

Example:

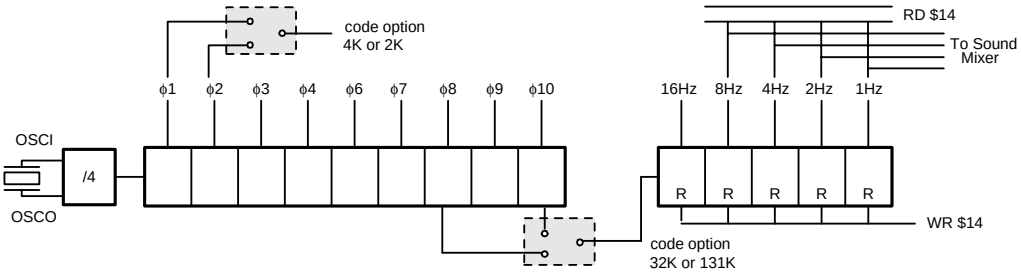


System Register 14:

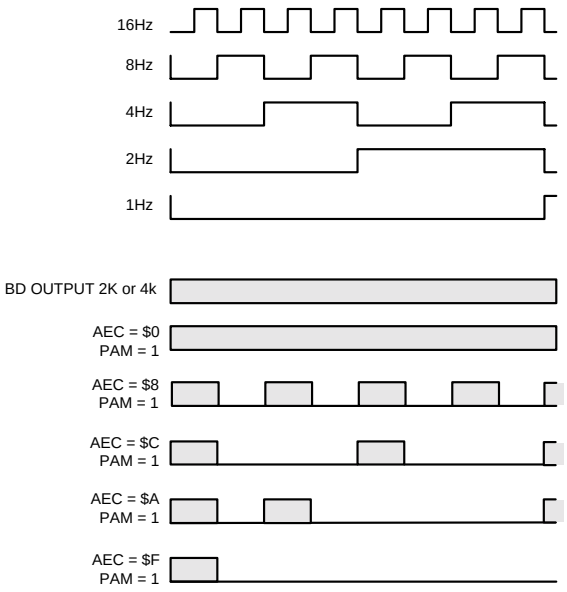
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power On
$14	AEC3	AEC2	AEC1	AEC0	R/W	ALARM envelope control	
	0	0	0	0		DC envelope	Yes
	X	X	X	1		1Hz envelope	
	X	X	1	X		2Hz envelope	
	X	1	X	X		4Hz envelope	
	1	X	X	X		8Hz envelope	

Default carrier frequency is 4KHz. Can be selected to 2KHz by code option.
WRITE mode: controls the envelope selection.
READ mode can read out current envelope waveforms.

Below is the ALARM functional block equivalent circuit diagram. To activate the ALARM function, first switch the PAM to ALARM OUTPUT mode. After setting PAM to 1, then set the proper envelope. When the data writes to AEC, the envelope counter will be synchronized. The programmer can read back the envelope from AEC register and make any pattern changes needed by programmer. The Read operation will not affect the alarm output waveform.



The programming alarm waveform is shown below:



System Register 15

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Description	Power on
$15	PPULL	O/S2	O/S1	-	R/W		0000
	X	X	0	-		PORTC as I/O port	Yes
	X	X	1	-		PORTC as LCD segment27 - 30	
	X	0	X	-		PORTD as I/O ports	Yes
	X	1	X	-		PORTD as LCD segment31 - 34	

4. LCD Driver

The LCD driver contains a controller, voltage generator, 4 common signal pins, and 34 segment driver pins. There are two different driving modes. One is 1/4 duty and 1/3 bias, the other is 1/3 duty and 1/2 bias (COM4 same as COM1). Driving mode is selected by code option, The controller consists of display data RAM and a duty generator. The LCD data RAM is a dual port RAM that transfers data to segment pins automatically without program control.

PORTC, PORTD can be used as LCD SEG27 - 34. It is selected by bit2 and bit1 of system register 15. When used as I/O ports, the data in LCD RAM does not affect the I/O input and output data. Also, when used as LCD output, the I/O RAM data won't affect LCD output. LCD RAM can be used as data memory if needed.

When the "STOP" instruction is executed, the LCD display output and LCD pump circuit are turned off, but the data of LCD RAM is the same as before executing the "STOP" instruction.

When LCD is off, both COMMON and SEGMENT output are low.

Configuration of LCD RAM Area: (Segments 1 - 34, 1/4 duty)

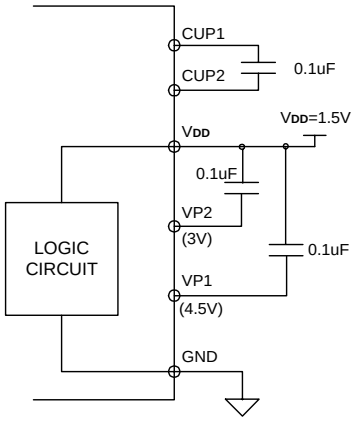
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1	311H	SEG18	SEG18	SEG18	SEG18
301H	SEG2	SEG2	SEG2	SEG2	312H	SEG19	SEG19	SEG19	SEG19
302H	SEG3	SEG3	SEG3	SEG3	313H	SEG20	SEG20	SEG20	SEG20
303H	SEG4	SEG4	SEG4	SEG4	314H	SEG21	SEG21	SEG21	SEG21
304H	SEG5	SEG5	SEG5	SEG5	315H	SEG22	SEG22	SEG22	SEG22
305H	SEG6	SEG6	SEG6	SEG6	316H	SEG23	SEG23	SEG23	SEG23
306H	SEG7	SEG7	SEG7	SEG7	317H	SEG24	SEG24	SEG24	SEG24
307H	SEG8	SEG8	SEG8	SEG8	318H	SEG25	SEG25	SEG25	SEG25
308H	SEG9	SEG9	SEG9	SEG9	319H	SEG26	SEG26	SEG26	SEG26
309H	SEG10	SEG10	SEG10	SEG10	31AH	SEG27	SEG27	SEG27	SEG27
30AH	SEG11	SEG11	SEG11	SEG11	31BH	SEG28	SEG28	SEG28	SEG28
30BH	SEG12	SEG12	SEG12	SEG12	31CH	SEG29	SEG29	SEG29	SEG29
30CH	SEG13	SEG13	SEG13	SEG13	31DH	SEG30	SEG30	SEG30	SEG30
30DH	SEG14	SEG14	SEG14	SEG14	31EH	SEG31	SEG31	SEG31	SEG31
30EH	SEG15	SEG15	SEG15	SEG15	31FH	SEG32	SEG32	SEG32	SEG32
30FH	SEG16	SEG16	SEG16	SEG16	320H	SEG33	SEG33	SEG33	SEG33
310H	SEG17	SEG17	SEG17	SEG17	321H	SEG34	SEG34	SEG34	SEG34

Configuration of LCD RAM Area: (Segments 1 - 34, 1/3 duty)

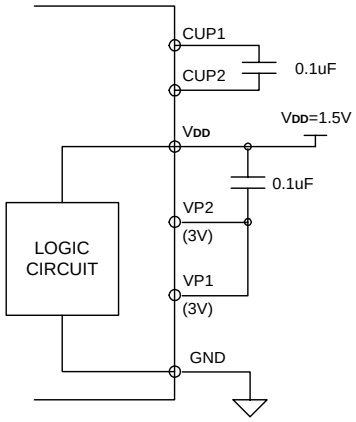
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	-	COM3	COM2	COM1		-	COM3	COM2	COM1
300H	-	SEG1	SEG1	SEG1	311H	-	SEG18	SEG18	SEG18
301H	-	SEG2	SEG2	SEG2	312H	-	SEG19	SEG19	SEG19
302H	-	SEG3	SEG3	SEG3	313H	-	SEG20	SEG20	SEG20
303H	-	SEG4	SEG4	SEG4	314H	-	SEG21	SEG21	SEG21
304H	-	SEG5	SEG5	SEG5	315H	-	SEG22	SEG22	SEG22
305H	-	SEG6	SEG6	SEG6	316H	-	SEG23	SEG23	SEG23
306H	-	SEG7	SEG7	SEG7	317H	-	SEG24	SEG24	SEG24
307H	-	SEG8	SEG8	SEG8	318H	-	SEG25	SEG25	SEG25
308H	-	SEG9	SEG9	SEG9	319H	-	SEG26	SEG26	SEG26
309H	-	SEG10	SEG10	SEG10	31AH	-	SEG27	SEG27	SEG27
30AH	-	SEG11	SEG11	SEG11	31BH	-	SEG28	SEG28	SEG28
30BH	-	SEG12	SEG12	SEG12	31CH	-	SEG29	SEG29	SEG29
30CH	-	SEG13	SEG13	SEG13	31DH	-	SEG30	SEG30	SEG30
30DH	-	SEG14	SEG14	SEG14	31EH	-	SEG31	SEG31	SEG31
30EH	-	SEG15	SEG15	SEG15	31FH	-	SEG32	SEG32	SEG32
30FH	-	SEG16	SEG16	SEG16	320H	-	SEG33	SEG33	SEG33
310H	-	SEG17	SEG17	SEG17	321H	-	SEG34	SEG34	SEG34

Connection Diagram

1. V_{DD}=1.5V, 4.5V LCD, 1/4 duty, 1/3bias



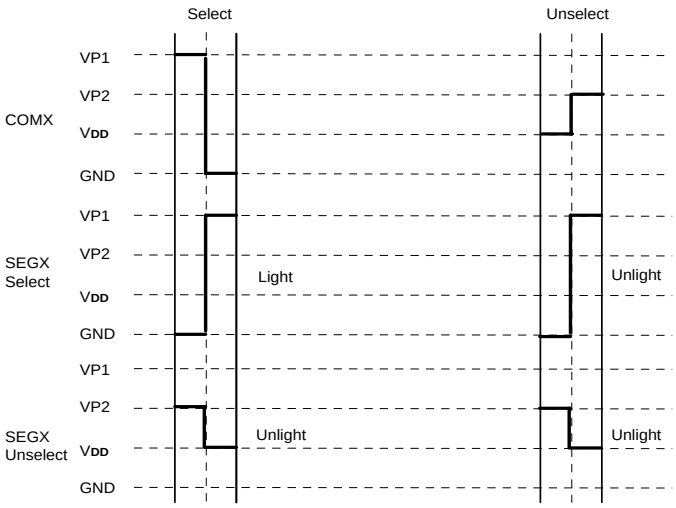
2. V_{DD}=1.5V, 3V LCD, 1/3 duty, 1/2bias

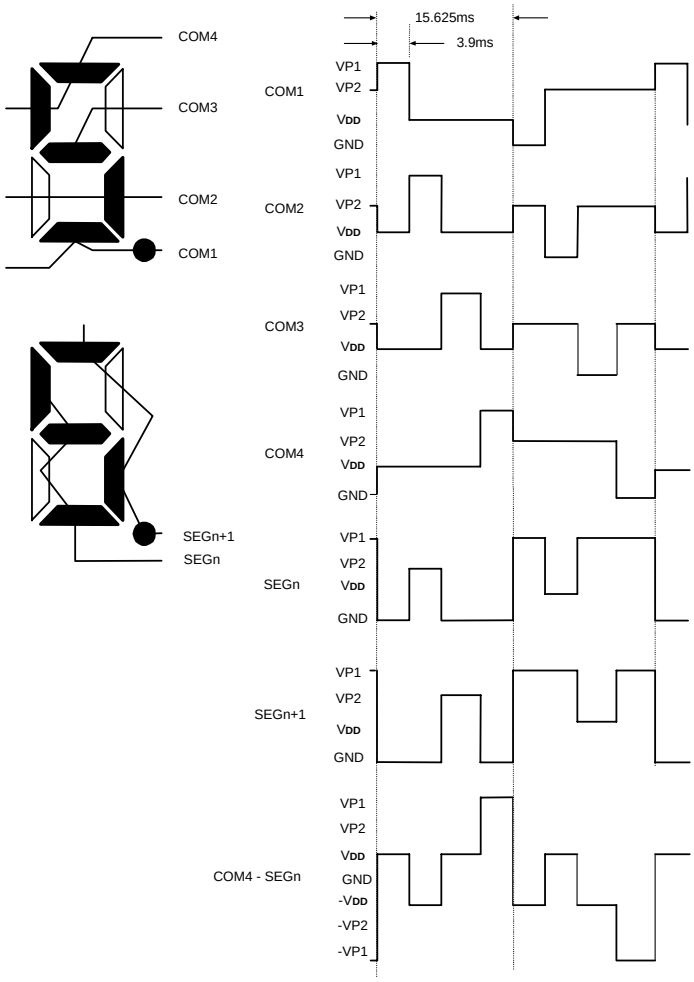


Notice:

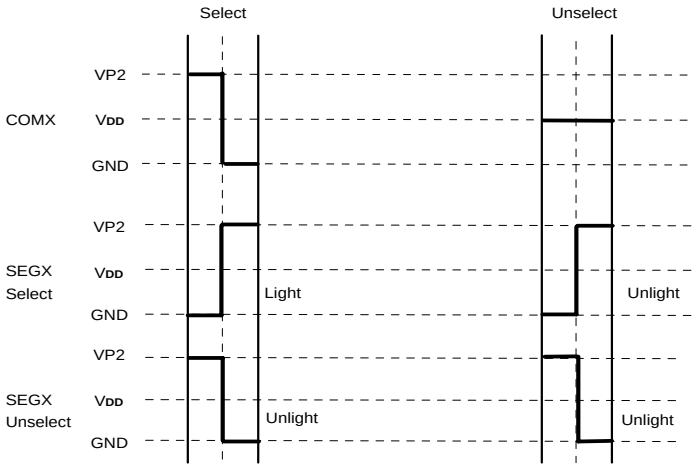
The pump circuit frequency can be 4KHz, or 2KHz (selected by code option). When using the small LCD panel, the user can select 2KHz pump frequency to save power. When using the large LCD panel, the user can select 4KHz pump frequency to have more power supply ability for LCD use. LCD duty and bias are selected by code option.

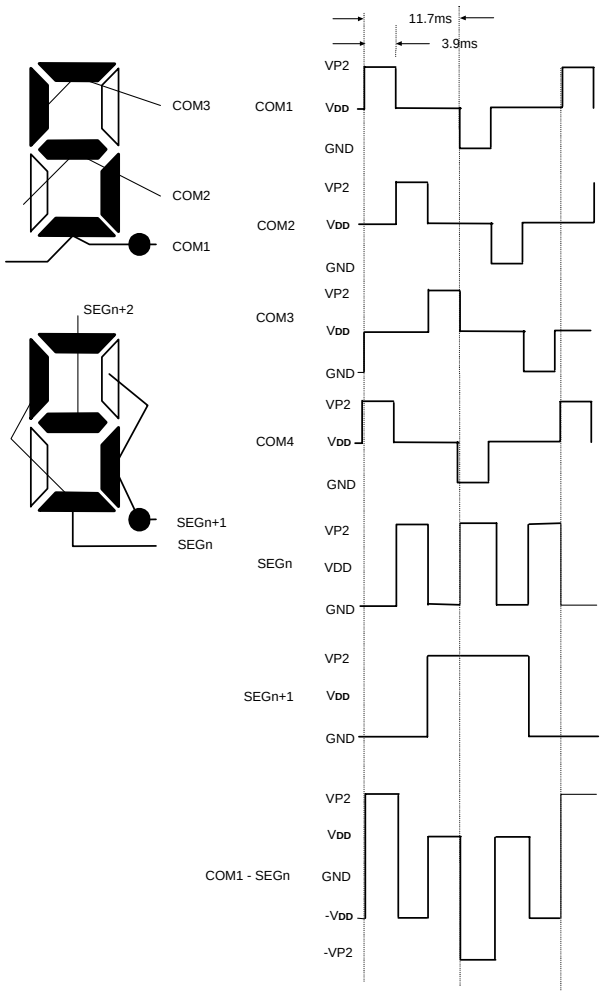
1/4 duty, 1/3 bias LCD Waveform (V_{DD} = 1.5V, V_{P1} = 4.5V, V_{P2} = 3V)





1/3 duty, 1/2 bias LCD Waveform (V_{DD} = 1.5V, V_{P1} = V_{P2} = 3V)

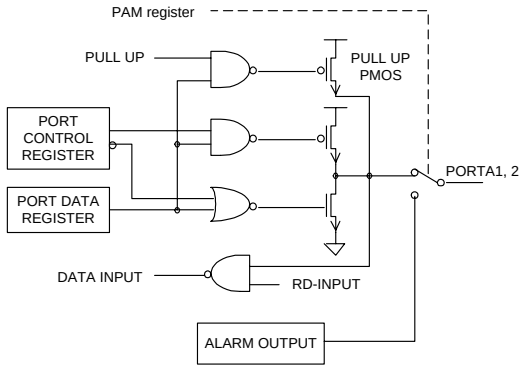




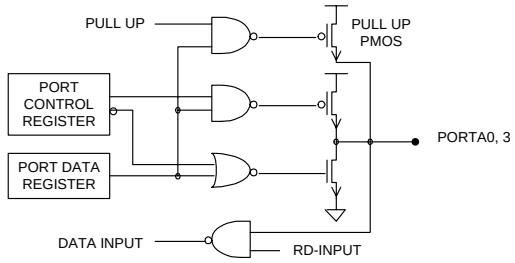
5. I/O Port

SH66L08 has 16 CMOS I/O ports: PORTA, PORTB, PORTC and PORTD. Each I/O pins contains pull-up MOS which is controlled by program. The PORT control register (PACR, PBCR, PCCR, and PDCR) controls the ON/OFF buffer of the output buffer. These I/O ports can be accessed through the read/write system register. The user can output any value to any I/O port at any time.

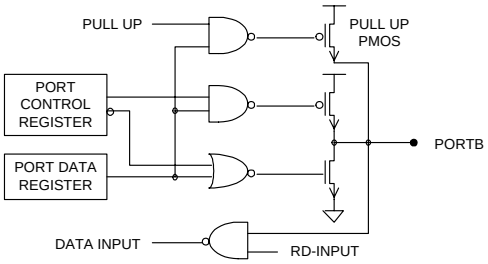
PORTA, B, C, D



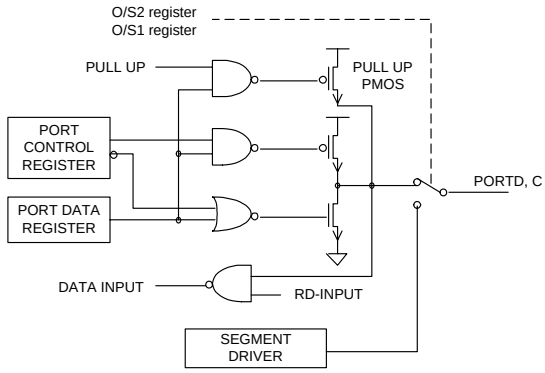
PORTA1, 2 (for reference only)



PORTA0, 3 (for reference only)



PORTB (for reference only)



PORTC, D (for reference only)

When PAM = 1 (system register 13H bit0), PA.1 & PA.2 are used as alarm output. When set O/S1 (system register 15H bit1) and O/S2 (system register 15H bit2) = 1, PORTC & PORTD are used as LCD SEGMENT outputs, and writing data to PC.X (system register 0AH), PD.X (system register 0BH) won't affect LCD output data.

Controlling the Pull-up MOS

These ports contain pull-up MOS controlled by program. System register 15 bit3 (PPULL) simultaneously controls ON/OFF of all pull-up MOS. Pull -up MOS is also controlled by the port data registers (PA, PB, PC, and PD) of each port. (Write 0 could turn off the pull-up MOS.) Thus the pull-up MOS can be turned ON/OFF individually.

Port Interrupt

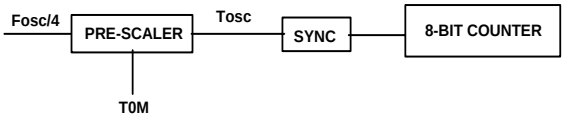
PORTB, PORTC interrupt (falling edge) is not controlled by Port I/O register. This means that if an interrupt request (IEx is set to 1, and one port bit from high to low) is been touched and that the condition is the other port bits are high level whenever the port bit is output or input. When PORTC are used as LCD outputs (O/S1 = 1), the PORTC interrupt is disabled.

External $\overline{\text{INT}}$

PortA.0 is shared by external interrupts (active low).

6. Timer

SH66L08 has two 8-bit timers. Their operation counts up. The timers consist of an 8-bit counter and an 8-bit preload register.



The timers provide the following functions:
- Programmable interval timer function.
- Reading counter value.

Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consists of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H), and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. The timer counter can be initialized by writing data into the timer load register (TL0L, TL0H; TL1L, TL1H).

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or count overflow occurs. The timer overflow will generate an interrupt if the interrupt enable flag is set.

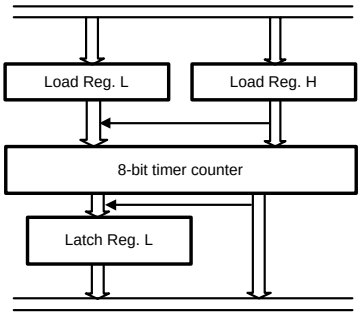
The timer can be programmed in several different system clock sources by setting the Timer Mode register (TM0,TM1).

Timer Load Register: Since the register H controls the physical READ and WRITE operations, please follow these steps:

Write Operation:
Low nibble first;
High nibble to update the counter

Read Operation:
High Nibble first;
Low nibble followed.

Timer Mode Register



The 8-bit counter counts prescaler overflow output pulses. The Timer Mode registers (TM0, TM1) are 4-bit registers used for timer control as shown in table1 and table 2. These mode registers set the input pulse sources into the timer.

Table 1: Timer0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	Fosc /4
0	0	1	$/2^{9}$	Fosc /4
0	1	0	$/2^{7}$	Fosc /4
0	1	1	$/2^{5}$	Fosc /4
1	0	0	$/2^{3}$	Fosc /4
1	0	1	$/2^{2}$	Fosc /4
1	1	0	$/2^{1}$	Fosc /4
1	1	1	$/2^{0}$	Fosc /4

Table 2: Timer1 Mode Register ($03)

TM1.2	TM1.1	TM1.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	Fosc /4
0	0	1	$/2^{9}$	Fosc /4
0	1	0	$/2^{7}$	Fosc /4
0	1	1	$/2^{5}$	Fosc /4
1	0	0	$/2^{3}$	Fosc /4
1	0	1	$/2^{2}$	Fosc /4
1	1	0	$/2^{1}$	Fosc /4
1	1	1	$/2^{0}$	Fosc /4

Interrupt

Four interrupt sources are available on SH66L08:

- External interrupt ($\overline{INT}$ share with PA.0)
- Timer0 interrupt
- Timer1 interrupt
- Port's falling edge detection interrupt ($\overline{PBC}$)

The Configuration of System Register $00:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags

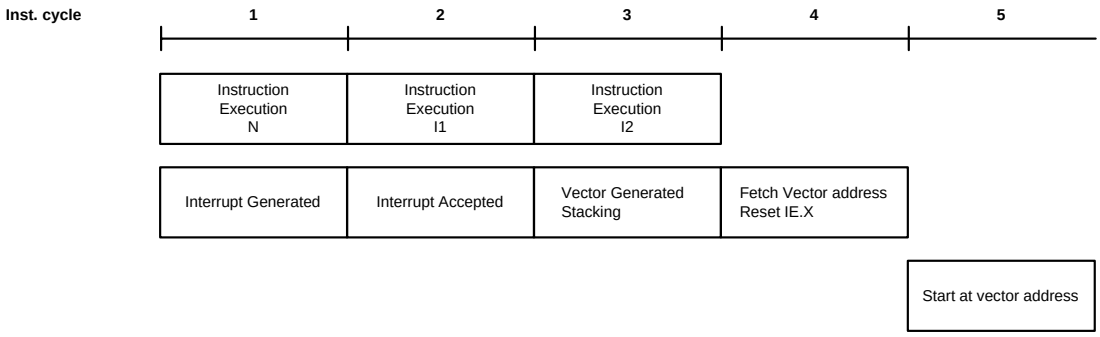
External Interrupt ($\overline{INT}$)

External interrupt is shared with the bit0 of PORTA. When bit3 of system register 0 (IEX) is set to 1, the external interrupt will be enabled, and a falling edge signal on PA.0 will generate an external interrupt. (Note: while external interrupt is enabled, writing a "0" to bit0 of PORTA will generate an external interrupt)

Timer0, Timer1 Interrupt, Port Interrupt and I/O Ports

The input clock of Timer0 and Timer1 are based on OSC clock. The programming of Timer interrupt, Port interrupts and I/O ports refer to SH6610C SPEC

● Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any INTERRUPT enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

System Clock

SH66L08 has one clock source. OSCI is 32.768KHz crystal or 131KHz RC determined by code option. The OSC generates the basic clock pulses that provide the system clock for CPU and on-chip peripherals (TIMER0, TIMER1, LCD).

Instructions

All instructions are one cycle and one-word instructions. Their characteristics are memory-oriented operation.
Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM memonic is EORI. However, EORI has the identical operation to EORIM. The same is true for ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC;Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC;Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	B (bbb)	RAM bank = 000
p	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +3.0V

Input Voltage. . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . -55°C to +125°C

***Comments**

Stresses at levels above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	
Operating Current	I_{OP}		3	6	μA	All output pins unload execute NOP instruction, exclude LCD & Alarm current
Standby Current	I_{SB1}		2	4	μA	All output pins unload (HALT mode), exclude LCD current. (Not heavy load mode)
Standby Current	I_{SB2}			0.5	μA	All output pins unload (STOP mode), LCD off
Input High Voltage	V_{IH1}	0.8 X V_{DD}		V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock)
Input High Voltage	V_{IH2}	0.85 X V_{DD}		V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST (schmitt trigger input)
Input Low Voltage	V_{IL1}	GND - 0.3		0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock)
Input Low Voltage	V_{IL2}	GND - 0.3		0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST (schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}			V	PORTB, C, D, PORTA.0, 3 (I_{OH} = -8μA)
Output Low Voltage	V_{OL1}			0.2 X V_{DD}	V	PORTB, C, D, PORTA.0, 3 (I_{OL}= 0.3mA)
Output High Voltage	V_{OH2}	0.8 X V_{DD}			V	BD/$\overline{BD}$ (PA.1, PA.2), I_{OH} = -0.3mA
Output Low Voltage	V_{OL2}			0.2 X V_{DD}	V	BD/$\overline{BD}$ (PA.1, PA.2), I_{OL} = 0.3mA
Output High Voltage	V_{OH4}	V_{P1} - 0.2			V	SEGx, I_{OH} = -3μA
Output Low Voltage	V_{OL4}			0.2	V	SEGx, I_{OL} = 3μA
Output High Voltage	V_{OH5}	V_{P1} - 0.2			V	COMx, I_{OH} = -8μA
Output Low Voltage	V_{OL5}			0.2	V	COMx, I_{OL} = 8μA
Pull-up Resistor	R_P		150		KΩ	PULL-UP resistor (V_{OH} = 0, I_{OH} = -10μA)
LCD Lighting	I_{LCD}			1	μA	No panel loaded. LCD pump frequency = 4K

DC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, Fosc = 131KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	
Operating Current	I_{OP}		10	15	μA	All output pins unload execute NOP instruction, exclude LCD & Alarm current
Standby Current	I_{SB1}		5	9	μA	All output pins unload (HALT mode) exclude LCD current. (Not heavy load mode)
Standby Current	I_{SB2}			0.5	μA	All output pins unload (STOP mode), LCD off, no current
Reset Current	I_{REST}			20	μA	Reset current
Input High Voltage	V_{IH1}	0.8 X V_{DD}		V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock)
Input High Voltage	V_{IH2}	0.85 X V_{DD}		V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST (schmitt trigger input)
Input Low Voltage	V_{IL1}	GND - 0.3		0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD, OSCI (Driven by external clock)
Input Low Voltage	V_{IL2}	GND - 0.3		0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST (schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}			V	PORTB, C, D, PORTA.0, 3 (I_{OH} = -8μA)
Output Low Voltage	V_{OL1}			0.2 X V_{DD}	V	PORTB, C, D, PORTA.0, 3 (I_{OL}= 0.3mA)
Output High Voltage	V_{OH2}	0.8 X V_{DD}			V	BD/$\overline{BD}$ (PA.1, PA.2), I_{OH} = -0.3mA
Output Low Voltage	V_{OL2}			0.2 X V_{DD}	V	BD/$\overline{BD}$ (PA.1, PA.2), I_{OL} = 0.3mA
Output High Voltage	V_{OH4}	V_{P1} - 0.2			V	SEGx, I_{OH} = -3μA
Output Low Voltage	V_{OL4}			0.2	V	SEGx, I_{OL} = 3μA
Output High Voltage	V_{OH5}	V_{P1} - 0.2			V	COMx, I_{OH} = -8μA
Output Low Voltage	V_{OL5}			0.2	V	COMx, I_{OL} = 8μA
Pull-up Resistor	R_P		150		KΩ	PULL-UP resistor (V_{OH} = 0, I_{OH} = -10μA)
LCD Lighting	I_{LCD}			1	μA	No panel loaded. LCD pump frequency = 4K

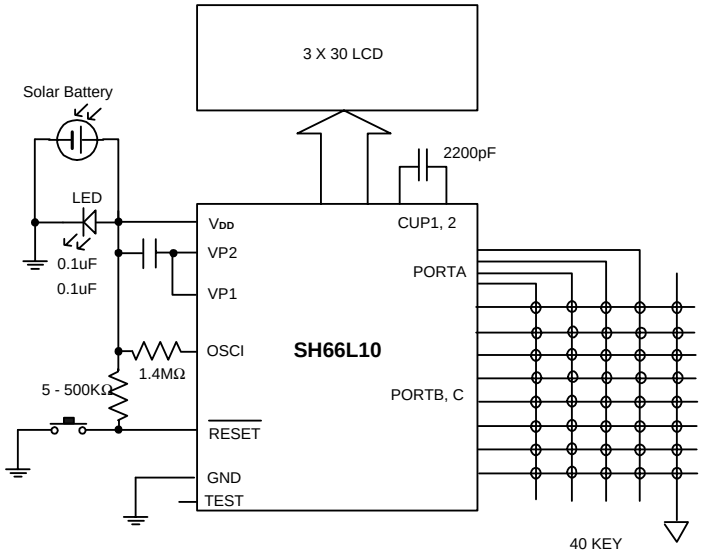
AC Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time (Crystal)	T_{STT}		1	2	s	F_{osc} = 32.768KHz
Frequency Variation(RC)	Δ F/F			±30	%	Include supply voltage and chip to chip variation OSC = 131K RC

Application Circuits (for reference only)

SH66L08 chip substrate connects to system ground.

AP1: V_{DD} = 1.5V
OSC: RC: 131K (code option)
LCD: 3V, 1/3 duty, 1/2 bias, PORTD used as segment.
PORTA - C: I/O



Code Option:

Addresses: $800
Body data: 0110 1010 0001 0000 (66L10)

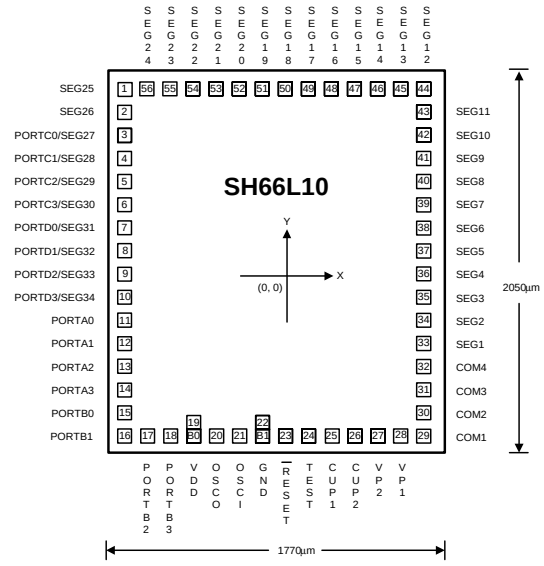
Addresses: $801
Data: CAPF 1D00 0000 0000
C (Clock source)
0 = 32768 Crystal (default)
1 = 131K RC

A (Alarm carrier frequency)
0 = 4KHz (default)
1 = 2KHz

PF (LCD Pump circuit frequency)
0, 1 = 2KHz
1, 0 = 4KHz (default)

D (Duty and bias option)
0 = 1/3 duty, 1/2 bias (default)
1 = 1/4 duty, 1/3 bias

Bonding Diagram



Substrate connects to GND
Bonding wire with 1.0mil diameter is recommended.

Pad Location

unit: µm

Pad No.	Designation	X	Y
1	SEG25	-760	900
2	SEG26	-760	757.5
3	PORTC0	-760	637.5
4	PORTC1	-760	517.5
5	PORTC2	-760	402.5
6	PORTC3	-760	287.5
7	PORTD0	-760	172.5
8	PORTD1	-760	57.5
9	PORTD2	-760	-57.5
10	PORTD3	-760	-172.5
11	PORTA0	-760	-287.5
12	PORTA1	-760	-402.5
13	PORTA2	-760	-517.5
14	PORTA3	-760	-637.5
15	PORTB0	-760	-757.5
16	PORTB1	-760	-900
17	PORTB2	-637.5	-900
18	PORTB3	-517.5	-900
19	V_{DD}	-402.5	-808
	B0	-402.5	-900
20	OSCO	-287.5	-900
21	OSCI	-172.5	-900
22	GND	-57.5	-808
	B1	-57.5	-900

Pad No.	Designation	X	Y
23	$\overline{\text{RESET}}$	57.5	-900
24	TEST	172.5	-900
25	CUP1	287.5	-900
26	CUP2	402.5	-900
27	VP2	517.5	-900
28	VP1	637.5	-900
29	COM1	760	-900
30	COM2	760	-757.5
31	COM3	760	-637.5
32	COM4	760	-517.5
33	SEG1	760	-402.5
34	SEG2	760	-287.5
35	SEG3	760	-172.5
36	SEG4	760	-57.5
37	SEG5	760	57.5
38	SEG6	760	172.5
39	SEG7	760	287.5
40	SEG8	760	402.5
41	SEG9	760	517.5
42	SEG10	760	637.5
43	SEG11	760	757.5
44	SEG12	760	900
45	SEG13	637.5	900
46	SEG14	517.5	900

Pad Location (continued)

Pad No.	Designation	X	Y
47	SEG15	402.5	900
48	SEG16	287.5	900
49	SEG17	172.5	900
50	SEG18	57.5	900
51	SEG19	-57.5	900
52	SEG20	-172.5	900

Pad No.	Designation	X	Y
53	SEG21	-287.5	900
54	SEG22	-402.5	900
55	SEG23	-517.5	900
56	SEG24	-637.5	900

Ordering Information

Part No.	Package
SH66L08H	CHIP FORM

SPEC Change History:

Ver 2.0

1. Change code option at $801 bit 11: cancel the OP invert selection for 32kHz-oscillator source. (Page 19)