SINO WEALTH

SH6636

Mask 4-bit Microcontroller with Remote control carrier synthesizer

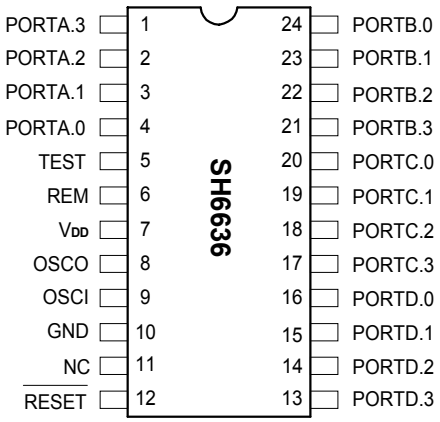
Features

- SH6610C-based single-chip 4-bit microcontroller
- ROM: 24K X 16 bits (bank switched)
- RAM: 128 X 4 bits (system control register & data memory)
- Operation voltage: 1.8V - 3.6V (Typically 3.0V)
- 16 CMOS bi-directional I/O pins
- 4-level subroutine nesting (including interrupts)
- One 8-bit automatic re-load timer/counter
- Powerful interrupt sources:
  - Timer0 interrupt
  - Port B & Port C interrupt (falling edge)
- Built-in remote control carrier synthesizer through software option
- Oscillator :
  - Ceramic resonator: 400K - 2MHz
- Instruction cycle time:
  - 4/455KHz (≈ 8.79μs) for 455KHz OSC clock
- Two low power operation modes: HALT and STOP
- Warm-up timer for power-on reset
- Low power detection by software option
- Pull-up resistor for reset pin

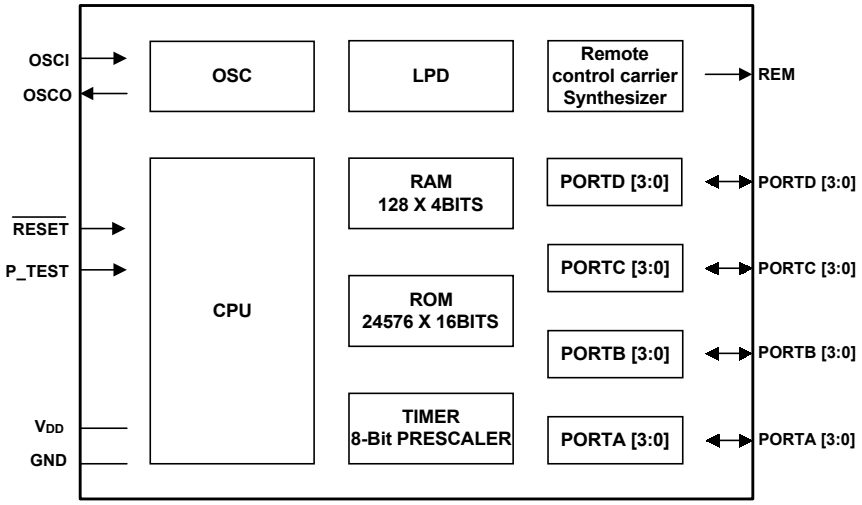
General Description

SH6636 is dedicated to infrared remote control transmitter applications. This chip integrates the SH6610C 4-bit CPU core with SRAM, program ROM, timer, and programmable input, output driving buffers, and carrier synthesizer. The standby function, which can be used to stop/start the ceramic resonator oscillation, facilitates the low power dissipation of the system.

Pin Configuration



Block Diagram



Pin Description

PIN No.	Symbol	I/O	Description
1 - 4	PORTA [3:0]	I/O	Bit programmable I/O pins
5	TEST	I	Test pin. Not connected for user
6	REM	O	Carrier synthesizer for infrared or RF output pin
7	V_{DD}	P	Power supply
8	OSCO	O	Oscillator output pin. Connected to ceramic oscillator
9	OSCI	I	Oscillator input pin. Connected to ceramic oscillator
10	GND	P	Ground pin
12	$\overline{\text{RESET}}$	I	Reset input. (Low active, internal pull up)
13 - 16	PORTD [3:0]	I/O	Bit programmable I/O pins
17 - 20	PORTC [3:0]	I/O I	Bit programmable I/O pins Vector port interrupt. (active falling edge)
21 - 24	PORTB [3:0]	I/O I	Bit programmable I/O pins Vector port interrupt. (active falling edge)
11	NC	-	Not connected

Total 24 pins.

Functional Description

1. CPU

The CPU core contains the following function blocks: Program Counter, ALU, Carry Flag, Accumulator, Table Branch Register (TBR), Data Pointer (INX, DPH, DPM and DPL), and Stack.

(a) PC (Program Counter)

The PC is used for ROM addressing consisting of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BAC);
(2) When executing a subroutine call instruction (CALL);
(3) When an interrupt occurs;
(4) When the chip is in the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can only address a 4K program ROM. To address a 24K program ROM, the bank switch must be used (Refer to the ROM description).

(b) ALU and CY (Carry Flag)

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

(c) Accumulator

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

(d) Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. It is organized into 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of the stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). The stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, where upon then the bottom of stack will be shifted out.

2. RAM

Built-in RAM consists of general-purpose data memory and a system register.

(a) RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing.

The following is the memory allocation map:
$000 - $01F: System register and I/O.
$020 - $07F: Data memory (96 X 4 bits).

(b) Data memory

Data memory is organized as 96 X 4 bits ($020 - $07F). Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

(c) Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPM (3-bits) and DPL (4-bits). The addressing range can have 128 locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9-bit0 comes from DPH, DPM and DPL.

(d) Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Description
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)
$03	-	-	-	-	-	Reserved
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit
$06	-	-	-	-	-	Reserved
$07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	-	-	-	Reserved
$0D	-	-	-	-	-	Reserved
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table branch register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	PPULL	CPS	CF1	CF0	W	Bit1-0: Carrier Frequency Control Bit2: Carrier OSC pre-divider Bit3: Port Pull-up MOS Control
$14	-	-	-	-	-	Reserved
$15	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control: 0101: LPD Enable (Default) 1010: LPD Disable
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA as output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB as output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC as output port
$19	PD3OUT	PD2OUT	PD1OUT	PD0OUT	W	Set PORTD as output port
$1A	-	-	-	-	-	Reserved
$1B	-	-	-	-	-	Reserved
$1C	-	-	-	-	-	Reserved
$1D	-	-	-	REMO	R/W	REM data output
$1E	-	-	-	-	-	Reserved
$1F	BNK3	BNK2	BNK1	BNK0	R/W	Bank register for ROM (BNK)

3. ROM

The SH6636 can address 24K X 16 bit words of program area from $0000 to $5FFF.

ROM SPACE in the system is 24576 X 16 bits.

(a) Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Function
$000H	JMP	Jump to RESET service routine
$001H	NOP	Reserved
$002H	JMP	Jump to TIMER0 service routine
$003H	NOP	Reserved
$004H	JMP	Jump to PBC service routine

(b) Table Data Reference

Table Data can be stored in the program memory and can be referenced by using the Table Branch (TJMP) and the Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, A)). The address is determined by RTNW to return look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

(c) Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM space. The bank switch technique is used to extend the CPU address space. The lower 2K of the CPU address space maps to the lower 2K of ROM space (BANK0). The upper 2K of the CPU address space maps to one of the fifteen banks (BNK 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A) of the upper 22K of ROM. (according to the Bank Register)

The bank switch mapping is as follows:

CPU Address	ROM Space, BNK = 0	ROM Space, BNK = 1	ROM Space, BNK = 2	ROM Space, BNK = 3	ROM Space, BNK = 4	ROM Space, BNK = 5	ROM Space, BNK = 6
000 - 7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
800 - FFF	0800 - 0FFF (BANK 1)	1000 - 17FF (BANK 2)	1800 - 1FFF (BANK 3)	2000 - 27FF (BANK 4)	2800 - 2FFF (BANK 5)	3000 - 37FF (BANK 6)	3800 - 3FFF (BANK 7)

CPU Address	ROM Space, BNK = 7	ROM Space, BNK = 8	ROM Space, BNK = 9	ROM Space, BNK = A
000 - 7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
800 - FFF	4000 - 47FF (BANK 8)	4800 - 4FFF (BANK 9)	5000 - 57FF (BANK 10)	5800 - 5FFF (BANK 11)

4. Timer

SH6636 has one 8-bit timer. The timer/counter has the following features:
. 8-bit up-counting timer/counter
. Automatically re-loads counter
. 8-bit pre-scaler
. Interrupt on overflow from $FF to $00

The following is a simplified timer block diagram.

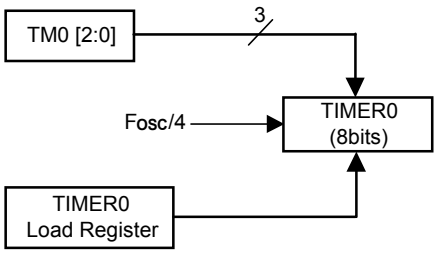


Figure 1. Timer block Diagram

(a) Configuration and Operation

Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

Load register programming: Write the low-order digit first and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FF to $00.

Timer Load Register: Since register H will control the physical READ and WRITE operations. Follow these steps:

Write Operation:
Low nibble first,
High nibble to update the counter

Read Operation:
High nibble first,
Followed by Low nibble.

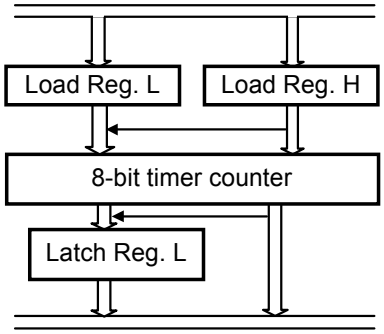


Figure 2. Timer Load register Configure

(b) Timer mode register

The timer can be programmed in several different prescaler ratios by setting the Timer Mode register (TM0).

The 8-bit counter prescaler overflow output pulses. The timer mode registers (TM0) are 3-bit registers used for timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Register

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^{9}$	512
0	1	0	$/2^{7}$	128
0	1	1	$/2^{5}$	32
1	0	0	$/2^{3}$	8
1	0	1	$/2^{2}$	4
1	1	0	$/2^{1}$	2
1	1	1	$/2^{0}$	1

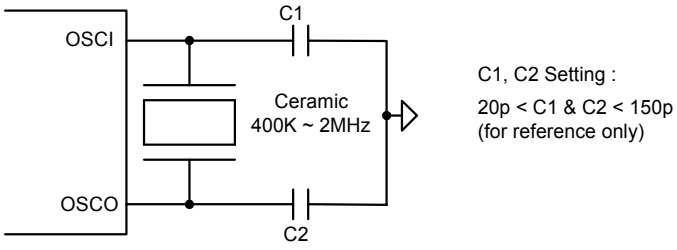
5. System Clock and Oscillator

System clock generator produces the basic clock pulses that provide the system clock for the CPU and peripherals.

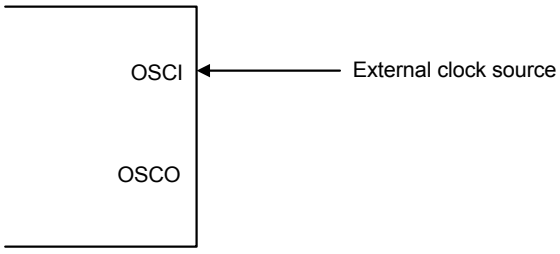
Instruction cycle time:
(1) 4/455KHz (≈ 8.79μs) for 455KHz system clock.

Oscillator

(1) Ceramic resonator: 400KHz - 2MHz.



(2) External input clock: 30KHz - 2MHz.



6. I/O PORT

The MCU provides 16 I/O pins.

Each I/O pin contains pull-up MOS controllable by the program. Bit3 of the PMOD register controls the On/Off status of all pull-up MOS simultaneously. Pull-up MOS is also controlled by the port data registers (PDR) of each port, so the pull-up MOS can be turned on and off individually.

The port control register (PCR) controls ON/OFF of the output buffer.

The following sections show the circuit configuration of the I/O ports.

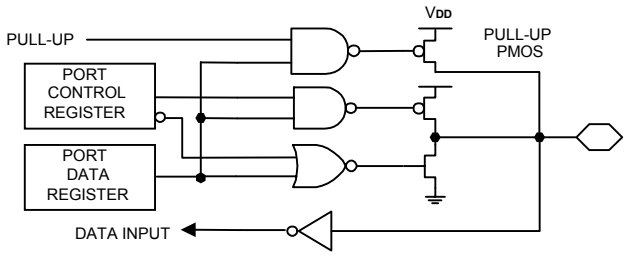


Figure 3. Port Configuration Function Block Diagram

Port I/O Data Register: (PDR)

Address	Bit3	Bit2	Bit1	Bit0
$08	PORT A.3	PORT A.2	PORT A.1	PORT A.0
$09	PORT B.3	PORT B.2	PORT B.1	PORT B.0
$0A	PORT C.3	PORT C.2	PORT C.1	PORT C.0
$0B	PORT D.3	PORT D.2	PORT D.1	PORT D.0

Port I/O Control Register: (PCR)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA as output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB as output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC as output port
$19	PD3OUT	PD2OUT	PD1OUT	PD0OUT	W	Set PORTD as output port

I/O control register: PAXOUT, PBXOUT, PCXOUT, PDXOUT (X = 0, 1, 2, 3)
0: Set I/O as an input buffer. (Power on initial)
1: Set I/O as an output buffer.

Port Function Control: (PMOD)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$13	PPULL	CPS	CF1	CF0	W	Bit3: Port Pull-up MOS Control

PPULL Port Pull-up MOS enables control
0: Disable PORT pull-up MOS (Power on initial)
1: Enable PORT pull-up MOS

7. Remote Control Synthesizer

SH6636 has a built in a carrier synthesizer for infrared or RF remote control circuits.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1D	-	-	-	REMO	R/W	Bit0: REM output data
$13	PPULL	CPS	CF1	CF0	W	Bit1-0: Carrier Frequency Control Bit2: Carrier OSC prescaler Bit3: Port Pull-up MOS Control

CPS: Oscillator range selection:

0: fx = System clock (default)
1: fx = System clock /8

CF1-0: Carrier Frequency control:

0, 0: No carrier (default)
0, 1: fx/8, 1/2 duty
1, 0: fx/12, 1/3 duty
1, 1: fx/12, 1/2 duty

REMO: REM output pin data control.

With these controls the SH6636 can transmit data with or without a carrier.
The functional block diagram is shown below:

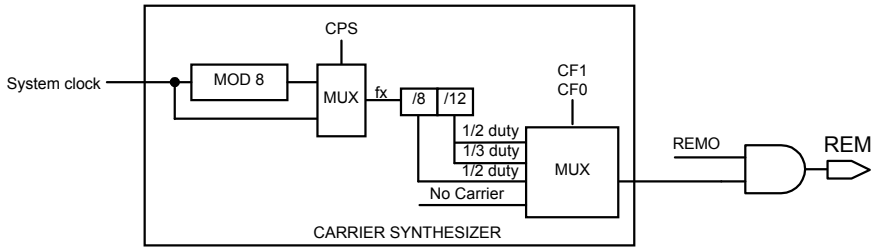


Figure 4. Remote Control Functional Block Diagram

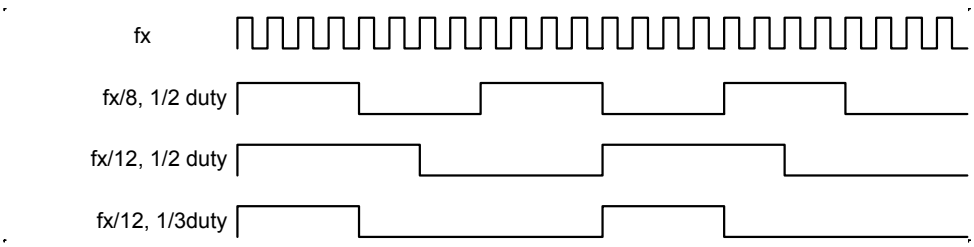


Figure 5. Remote Carrier Duty

8. Interrupt

Two interrupt sources are available on the SH6636:

- Timer0 overflow interrupt
- Port's falling edge detection interrupt ($\overline{PBC}$)

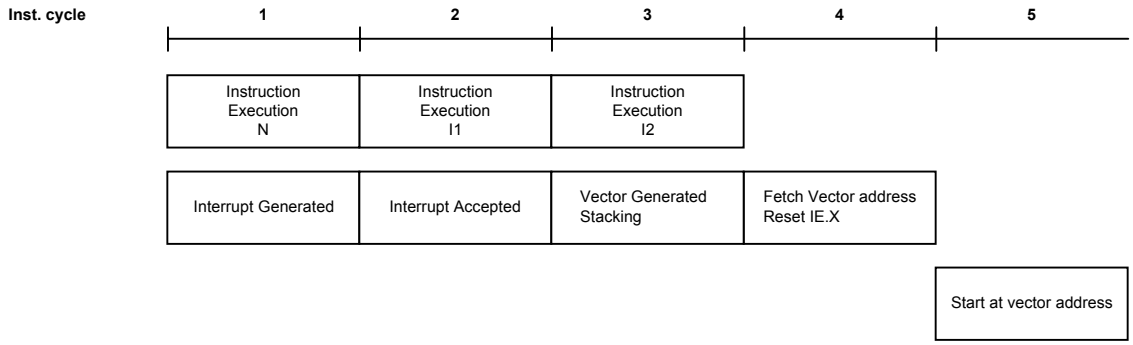
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

Address	Bit3	Bit2	Bit1	Bit0	Remarks
$00	-	IET0	-	IEP	Interrupt enable flags
$01	-	IRQT0	-	IRQP	Interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and a vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into the stack memory and jump to the interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and the vector address will be generated from the priority PLA corresponding to the interrupt sources.

Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution, N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

(a) Timer (Timer0) Interrupt

The timer overflow will generate an internal interrupt request, when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will start. This can also be used to wake the CPU from HALT mode.

(b) Port Interrupt ($\overline{PBC}$)

The PORTB and PORTC are used as port interrupt sources. Since PORT I/O is a bit programmable I/O, only the input port can generate an external interrupt. Any one of the PORTB and PORTC input pin transitions from V_{DD} to GND will generate an interrupt request. Further falling edge transition will not be able to make an interrupt request until all of the input pins have returned to V_{DD}. This can also be used to wake the CPU from STOP mode. The following is the port interrupt function block-diagram.

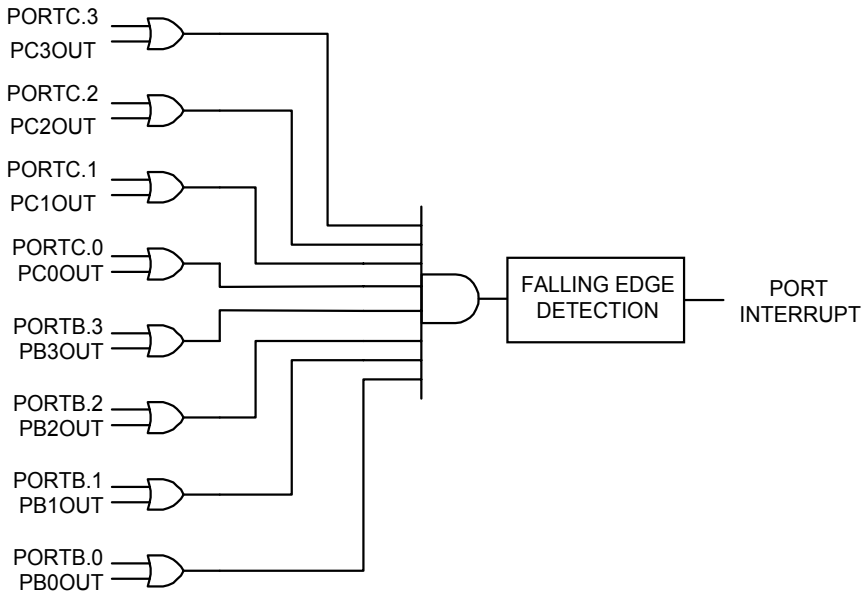


Figure 6. PORT Interrupt Block Diagram

9. HALT and STOP mode

After execution of the HALT instruction, SH6636 will enter HALT mode.
In HALT mode, the CPU will stop operating. But peripheral circuit (timer) will keep operating.
After the execution of the STOP instruction, SH6636 will enter STOP mode.
In STOP mode, the entire chip (including oscillator) will stop operating.
In HALT mode, SH6636 can be woken up if any interrupt occurs.
In STOP mode, SH6636 can be woken up if a port interrupt occurs.

10 Warm-up Timer

The SH6636 has a built in oscillator warm-up timer to eliminate an unstable state of initial oscillation when the oscillator starts oscillating under the following conditions:
(1) Power on reset
(2) Wake-up from stop mode

Warm-up time interval (Fosc/512 cycles of oscillator):

(1) Power on reset interval is as long as the initial oscillator's frequency mode warm-up timer interval.
When SH6636 operates in 455KHz frequency, the warm-up time interval is 1.13 ms.
(2) 2MHz ceramic oscillator wake-up:
When SH6636 operates in 2MHz frequency, the warm-up time interval is 256 μs.

11. Low Power Detection (LPD)

The LPD function is to monitor the supply voltage and applies an internal reset in the microcontroller at the time of battery replacement. If the applied circuit satisfies the following conditions, the LPD can be incorporated by the software control.

High reliability is not required.

Power supply voltage V_{DD} = 2.2 to 3.6 V

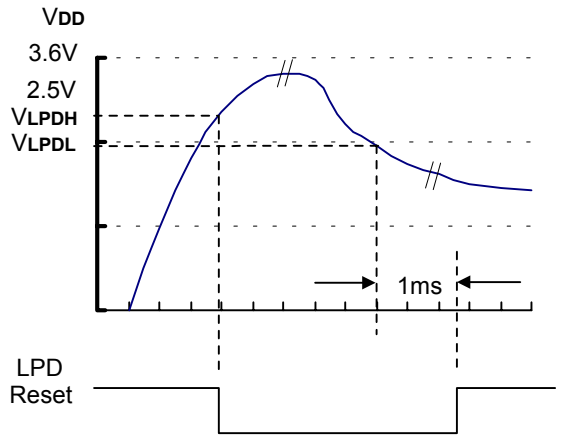
Operating ambient temperature T_A = -20°C to + 70°C

(a) Functions of the LPD Circuit:

The LPD circuit has the following functions:

Generates an internal reset signal when $V_{DD} \leq V_{LPDL}$.
Cancels the internal reset signal when $V_{DD} > V_{LPDH}$.
Stops the oscillator operation and forces the CPU to enter STOP mode when $V_{DD} \leq V_{LPDL}$.

Here, V_{DD}: power supply voltage, V_{LPDL}: POWER DOWN LPD-detect voltage, V_{LPDH}: Power rise LPD-detect voltage.



V_{LPDX} is always in range of CPU operating, so there is no malfunction existing when V_{LPDX} is reached. As $V_{DD} \leq V_{LPDL}$, the LPD reset will delay about 1ms to be triggered. If V_{DD} goes back to $V_{DD} > V_{LPDH}$, without any delay then cancel the LPD reset.

(b) LPD Control Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$15	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 - 0): 0101: LPD Enable (Power-on initial) 1010: LPD Disable

Initial State

There are 3 types of system resets:

1. Hardware reset input
2. Power on reset
3. Low Power Detection reset

Hardware	After Power-on Reset
Program Counter	$000
CY	Undefined
Data Memory	Undefined
System Register	Undefined
AC	Undefined
Timer Counter	Undefined
Timer Mode Register	0
Interrupt Enable Flags	0
Interrupt Request Flags	0
DPH, DPM, DPL	Undefined
TBR	Undefined
I/O ports	Input
REMO	0
PPULL	0
CPS	0
CF1, CF0	00
LPD [3:0]	0101B (LPD Enable)
BNK [3:0]	0000B

Instruction Set

All instructions are one cycle and one-word instructions. The characteristics are memory-oriented operation.

Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC [3]; AC[0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx v I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx ^ I	

* In the assembler ASM66 V1.0, EORIM mnemonic is EORI. However, EORI has the same operation identical with EORIM. It is true for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not include p)	
RTNW H;L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
P	ROM page		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Rating*

DC Supply Voltage . . . . . -0.3V to + 7.0V

Input Voltage . . . . . -0.3V to V_{DD}+ 0.3V

Operating Ambient Temperature . . . -10°C to + 60°C

Storage Temperature . . . . . .-55°C to + 125°C

***Comments**

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 455KHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	1.8	3.0	3.6	V	When LPD is inactive
V_{DD}	Operating Voltage	2.2	3.0	3.6	V	When LPD is active
I_{OP}	Operating Current by V_{DD}	-	0.3	1	mA	All output pins unload (Execute NOP instruction)
I_{SB1}	HALT Current	-	40	-	µA	OSC: 400K; CPU halt ALL output pins unload, LPD off
I_{SB2}	STOP Current	-	-	1	µA	OSC STOP ALL output pins unload, LPD off
I_{REM1}	REM Sink Current	0.3	-	-	mA	V_{REM} = 0.3V
I_{REM2}	REM Driving Current	-5	-9	-	mA	V_{REM} = 1V
V_{IL1}	Input Low Voltage	GND	-	V_{DD} X 0.2	V	I/O ports, pins tri-state
V_{IL2}	Input Low Voltage	GND	-	V_{DD} X 0.15	V	$\overline{\text{RESET}}$
V_{IL3}	Input Low Voltage	GND	-	V_{DD} X 0.3	V	OSCI (Driven with external clock)
V_{IH1}	Input High Voltage	V_{DD} X 0.7	-	V_{DD}	V	I/O Ports, pins tri-state
V_{IH2}	Input High Voltage	V_{DD} X 0.8	-	V_{DD}	V	$\overline{\text{RESET}}$
V_{IH3}	Input High Voltage	V_{DD} X 0.7	-	V_{DD}	V	OSCI (Driven with external clock)
I_{IH1}	High-level Input Current	-	-	0.2	µA	I/O ports; $V_{I/O}$ = V_{DD}
I_{IH2}	high-level Input Current	-	1	5	µA	$V_{\overline{RESET}}$ = V_{DD}
I_{IL1}	Low-level Input Current	-10	-	-30	µA	I/O ports with pull-up; $V_{I/O}$ = GND
I_{IL2}	Low-level Input Current	-	-	-1	µA	I/O ports with no pull-up; $V_{I/O}$ = GND
I_{IL3}	Low-level Input Current	-	-15	-30	µA	$V_{\overline{RESET}}$ = GND + 0.25V
V_{OH}	High-level Output Current	V_{DD} - 0.7	-	-	V	I/O ports, I_{OH} = -1.0 mA
V_{OL}	Low-level Output Current	-	-	GND + 0.6	V	I/O ports, I_{OL} = 5 mA

LPD Circuitry (GND = 0V, T_A = 25°C, F_{OSC} = 455KHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{LPD}	LPD-detected Voltage	-	1.9	-	V	(for reference only)
I_{LPD}	LPD circuit current	-	2.0	3.0	µA	V_{DD} = 3.0V. (for reference only)

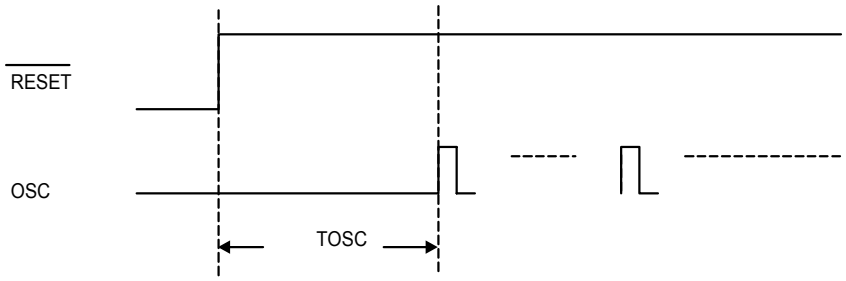
AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Tosc	Oscillator start time	-	-	35	ms	Ceramic Fosc = 400KHz. (for reference)
|ΔF|/F	Frequency stability	-	-	0.1	%	Ceramic FOSC = 2MHz, [F(3.0) - F(2.7)]/F(3.0)

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
TCY	Instruction Cycle Time	2	-	10	μs	Fosc = 400KHz - 2MHz

Timing Waveform

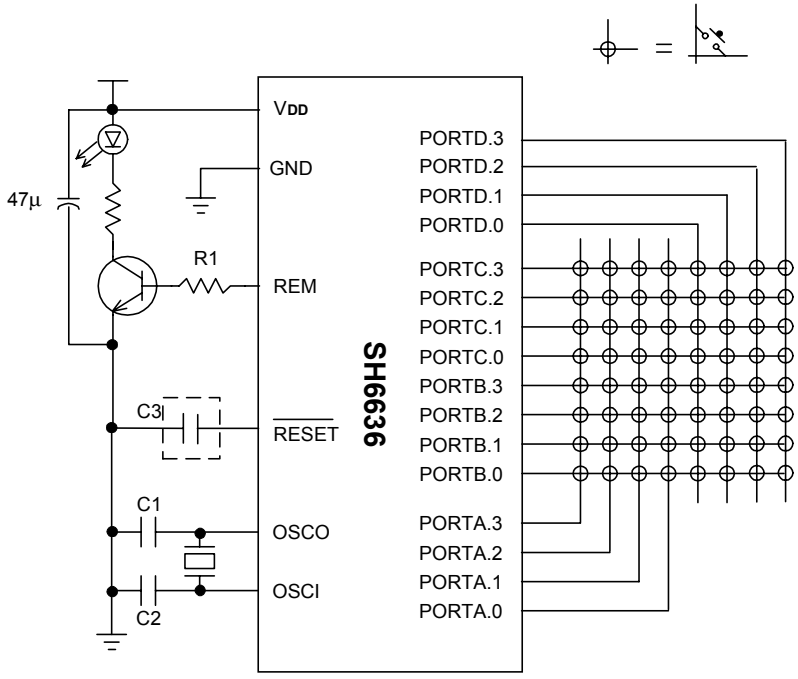


Application Circuit (for reference only)

AP1:

Remote Control (64 Keys)

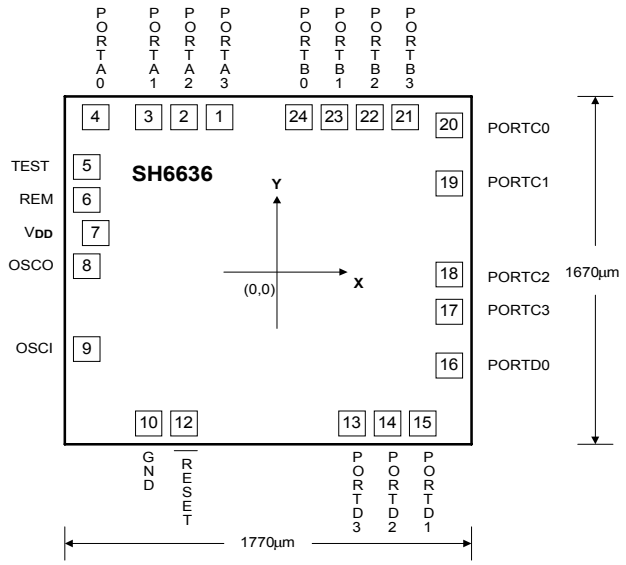
(1) Oscillator: Ceramic 400KHz - 2MHz
(2) C1 = C2 = 20P - 150P
(3) Port A and D: I/O Buffers
(4) Port B and C: Input Buffers
(5) C3 can be removed, but for increased reliability, C3 needs to be added
(6) R1 = 0 is possible, but the REM specification is revised to reduce power consumption
(7) I_{REM} = -5mA (V_{REM} = 1V).



Ordering Informations

Part No.	Packages
SH6636H	CHIP FORM
SH6636K	24L SKINNY
SH6636M	24L SOP

Bonding Diagram



* Substrate connects to GND.

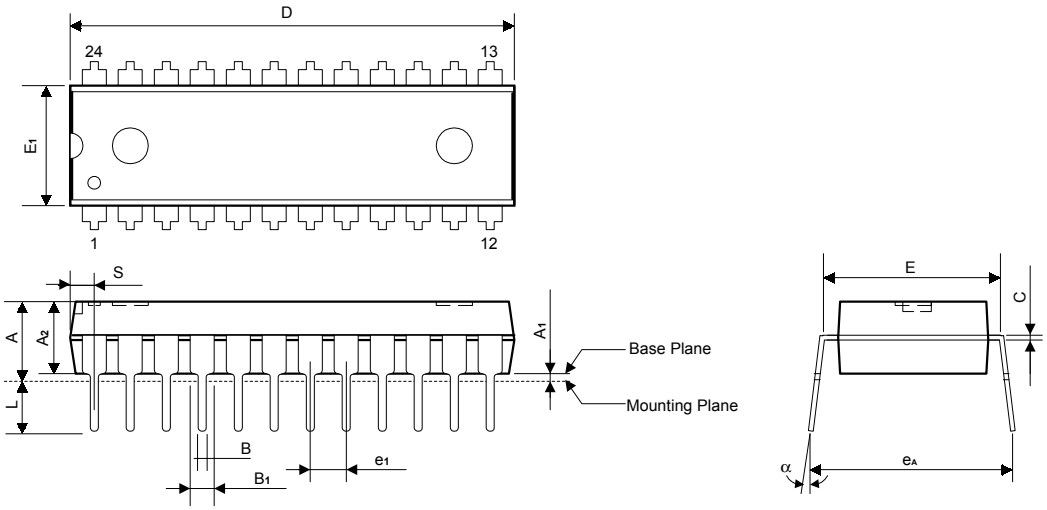
SH6636 unit: μm

Pad No	Designation	X	Y
1	PORTA3	-306.25	710.00
2	PORTA2	-426.25	710.00
3	PORTA1	-546.25	710.00
4	PORTA0	-738.20	710.00
5	TEST	-760.00	471.40
6	REM	-760.00	351.40
7	VDD	-748.40	231.40
8	OSCO	-760.00	67.50
9	OSCI	-760.00	-359.55
10	GND	-524.80	-710.00
11	NC		
12	$\overline{\text{RESET}}$	-404.80	-710.00
13	PORTD3	433.55	-710.00
14	PORTD2	553.55	-710.00
15	PORTD1	673.55	-710.00
16	PORTD0	758.20	-454.05
17	PORTC3	758.20	-116.70
18	PORTC2	758.20	31.70
19	PORTC1	758.20	391.80
20	PORTC0	758.20	662.45
21	PORTB3	608.35	710.00
22	PORTB2	476.35	710.00
23	PORTB1	356.35	710.00
24	PORTB0	236.35	710.00

Package Informations

SKINNY 24L Outline Dimensions

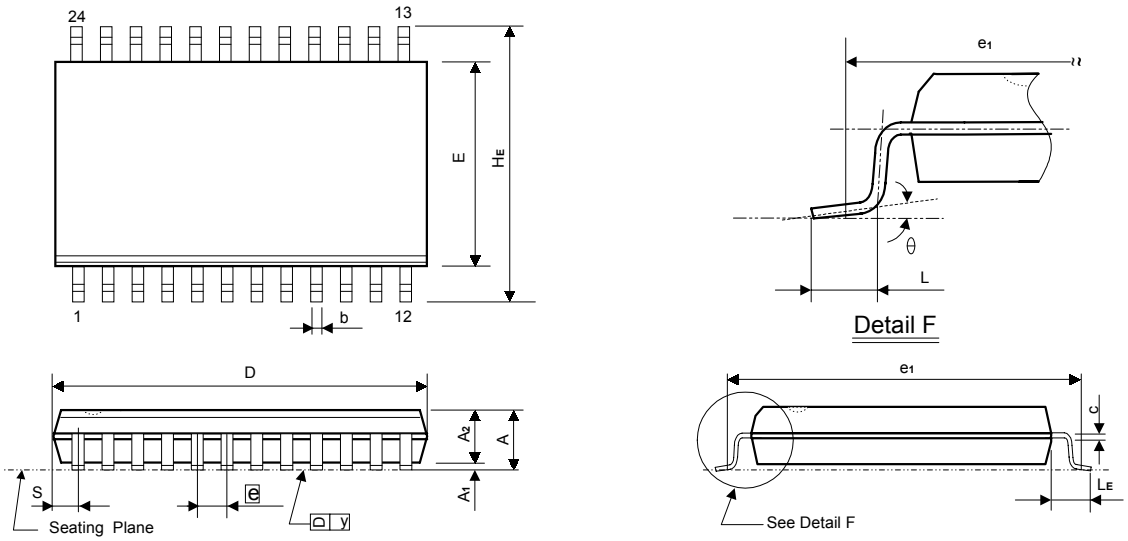
unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.010	3.30 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.258 Typ. (1.278 Max.)	31.95 Typ. (32.46 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.258 Typ. (0.270 Max.)	6.55 Typ. (6.86 Max.)
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.094 Max.	2.39 Max.

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

SOP (N.B.) 24L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.110 Max.	2.79 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.091 ± 0.005	2.31 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.006 +0.004 -0.002	0.15 +0.10 -0.05
D	0.606 ± 0.014	15.39 ± 0.36
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.370 NOM.	9.40 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.036 ± 0.008	0.91 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.040 Max.	1.02 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.