SINO WEALTH

SH6513

24K 4-Bit Microcontroller with Speech Synthesizer and LCD Driver

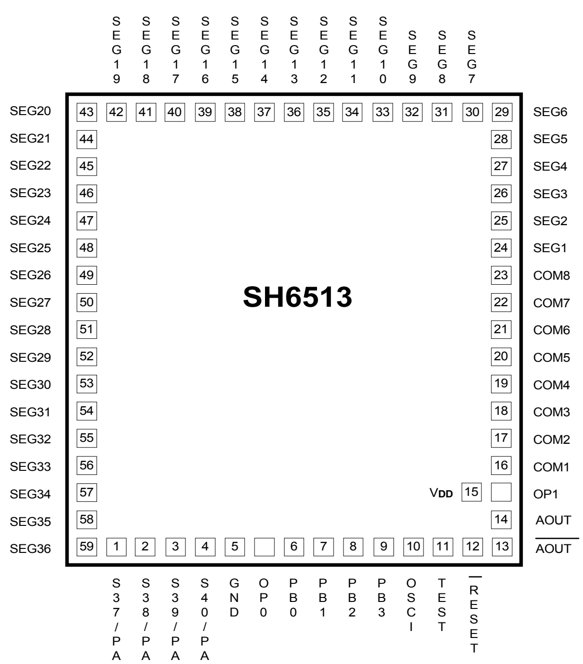
Features

- SH6610C-based single-chip 4-bit Microcontroller with LCD driver
- ROM: 24K X 16 bits (bank switched)
- RAM: 256 X 4 bits (system control register & data memory)
- Operating Voltage Range: 2.4V - 5.5V
- 8 CMOS I/O ports
- 4 level subroutine nesting including interrupts
- One 8-bit timer with pre-divider circuit
- Warm-up timer for power-on reset
- Powerful interrupt sources:
  - Speech end interrupt
  - Timer0 interrupt
  - Port B interrupt (falling edge)
- System clock: 4 MHz single-pad voltage-controlled oscillator
- Table Branch and Return Constant Instructions for Table Data Generation
- Data pointer with special system register control
- Two low power operating modes - HALT and STOP
- Instruction cycle time: 1 µs for 4 MHz voltage-controlled oscillator
- Built-in speech synthesizer and 2 channel tone generator
- Type B LCD drive circuit
- LCD driver: 40 X 8 (1/8 duty cycle, 1/4 bias)
- LCD off by programming LCDOFF register
- Available in CHIP FORM

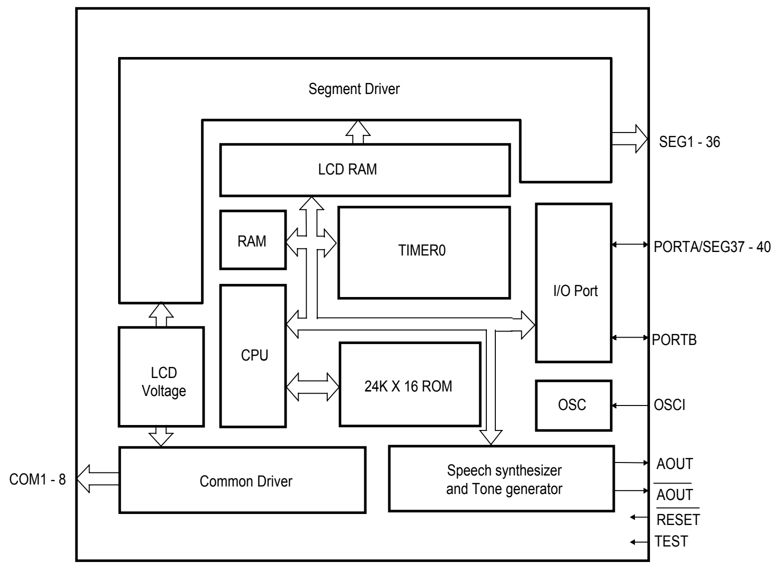
General Description

SH6513 is a single chip 4 bit µC dedicated chip for handheld games. This device integrates a SH6610C 4-bit CPU core with RAM, ROM, timer, speech synthesizer, tone generator and dot matrix LCD driver.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Symbol	I/O	Description
1 - 4	PA0 - PA3/ SEG37 - 40	I/O	Bit Programmable I/O, shared by LCD Seg37 - 40
5	GND	P	Ground
6 - 9	PB0 - PB3	I/O	Bit Programmable I/O, Vector Interrupt
10	OSCI	I	OSC Input
11	TEST	I	TEST (Internal pull low, no connection for user)
12	$\overline{\text{RESET}}$	I	Reset Input (Internal pull high, active low)
13	$\overline{\text{AOUT}}$	O	Audio Output
14	AOUT	O	Audio Output
15	V_{DD}	P	Power Supply
16 - 23	COM8 - 1	O	Common Signal Output for LCD Display
24 - 59	SEG36 - 1	O	Segment Signal Output for LCD Display, Seg31-36 shared by Output

Functional Description

1. CPU

The CPU core contains the following function blocks: Program Counter, ALU, Carry Flag, Accumulator, Table Branch Register (TBR), Data Pointer (INX, DPH, DPM and DPL), and the Stack.

(a) PC (Program Counter)

The PC is used for ROM addressing and consists of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10 - PC0).

The program counter normally increases by one (+1) with each execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BAC);

(2) When executing a subroutine call instruction (CALL);

(3) When an interrupt occurs;

(4) When the chip is at INITIAL RESET. The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The Program Counter can only address a 4K program ROM. To address a 24K program ROM, the user must use a bank switch (Refer to the ROM description in Section 3 for details).

(b) ALU and CY

ALU performs arithmetic and logic operations.

The ALU provides the following functions:

Binary addition/subtraction
(ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDI, EORI, ORI)
Decision (BA0, BA1, BA2, BA3, BAZ, BAC)
The Carry Flag (CY) holds the arithmetic operation ALU overflow.

During an interrupt or call instruction, the carry is pushed into the stack and restored from the stack by RTNI. It is unaffected by a RTNW instruction.

(c) Accumulator

The Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data transfers between the accumulator and system register, LCD RAM, or data memory can be performed.

(d) Stack

A group of registers used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt, it is organized into 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of the Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). The stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupt requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of the stack will be shifted out.

2. RAM

RAM consists of general-purpose data memory, LCD RAM, and system registers.

(a) RAM Addressing

Data memory and the system register can be accessed in one instruction by direct addressing. Following is the memory allocation map:

$000 - $01F: System register and I/O (32 X 4 bits)
$020 - $0FF: Data Memory (224 X 4 bits)
$100 - $2FF: Reserved
$300 - $34F: LCD RAM space (80 X 4 bits)

(b) Data Memory

Data memory is organized as 224 X 4 bits ($020 - $0FF). Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT mode.

(c) System Registers

The Configuration of the System Registers is as follows:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IES	IET0	-	IEP	R/W	Interrupt enable flags
$01	IRQSE	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 mode register (TM0)
$03	-	-	-	-	-	Reserved
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble
$06	SEG34	SEG33	SEG32	SEG31	W	Output port register
$07	-	-	SEG36	SEG35	W	Output port register
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA to be output
$0B	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB to be output
$0C	PPULL	LCDOFF	OP1	OP0	R W	OP1, OP0: Bonding Option LCDOFF: LCD Power control PPULL: Port pull-up control
$0D	O/S	PAS	SPS	LPS	W	SPS, LPS: Speech or LCD frequency control PAS: Set PORTA as LCD segment37 - 40 O/S: Set LCD segment 31 - 36 as output
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register (TBR)
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo Index Register (INX)
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data Pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data Pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data Pointer for INX high nibble
$13	TV1.3	TV1.2	TV1.1	TV1.0	W	Tone generator 1 volume low nibble
$14	PWMMD	-	-	-	W	PWM mode selection
$15	SEN/ TG1EN	SST/ TV1.6	SV1/ TV1.5	SV0/ TV1.4	R/W	Speech control bit or Tone generator 1 volume high nibble
$16	SA3/ TG1.3	SA2/ TG1.2	SA1/ TG1.1	SA0/ TG1.0	W	SA3 - 0: Speech data start address low nibble TG1.3 - 0: Tone generator 1 low nibble
$17	SA7/ TG1.7	SA6/ TG1.6	SA5/ TG1.5	SA4/ TG1.4	W	SA7 - 4: Speech data start address TG1.7 - 4: Tone generator 1 middle nibble
$18	SA11/ TG1.11	SA10/ TG1.10	SA9/ TG1.9	SA8/ TG1.8	W	SA11 - 8: Speech data start address TG1.11 - 8: Tone generator 1 high nibble

The Configuration of System Registers (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$19	STS	SA14	SA13	SA12	W	SA14 - 12: Speech data start address high nibble STS: Speech or tone generator selection bit
$1A	TV2.3	TV2.2	TV2.1	TV2.0	W	Tone generator 2 volume low nibble
$1B	TG2EN	TV2.6	TV2.5	TV2.4	R/W	Tone generator 2 volume high nibble TG2EN: Tone generator 2 enable
$1C	TG2.3	TG2.2	TG2.1	TG2.0	W	Tone generator 2 low nibble
$1D	TG2.7	TG2.6	TG2.5	TG2.4	W	Tone generator 2 middle nibble
$1E	TG2.11	TG2.10	TG2.9	TG2.8	W	Tone generator 2 high nibble
$1F	BNK3	BNK2	BNK1	BNK0	R/W	Bank Register for ROM (BNK)

(d) Data Pointer

Data memory can be indirectly addressed by the Data Pointer. The pointer address is located in the registers DPM (3-bits) and DPL (4-bits). The addressing range can have 128 locations. The pseudo index address (INX) is used to read or write Data memory and then the RAM address bit9-bit0 comes from DPH, DPM and DPL.

3. ROM

SH6513 can address up to 24K words of program area from $000 to $5FFF. The ROM can be defined as program ROM, speech data and melody wave table continuously without any limitation.

(a) Vector Address Area ($000 to $004)

The program is sequentially executed. An area from address $000 through $004 is reserved for any special interrupt service routines as starting execution of a vector address.

Address	Instruction	Remarks
$000	JMP	Jump to RESET
$001	JMP	Jump to Speech End
$002	JMP	Jump to TIMER0
	NOP	
$004	JMP	Jump to PB

JMP can be replaced by any other instruction.

(b) Table Data Reference

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) are placed by an offset address in the program ROM. TJMP instruction branches into address ((PC11 - PC8) X (2^8) + (TBR, A)). The address is determined by RTNW returning the look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

(c) Bank Switch Mapping

The Program Counter (PC11 - PC0) can only address 4K of ROM space. The bank switch technique is used to extend the CPU address space. The lower 2K of the CPU addressing space maps to the lower 2K of ROM space (BANK0). The upper 2K of the CPU addressing space maps to one of the fifteen banks (BANK 1 - 15) of the upper 30K of ROM. (according to the Bank Register)

The bank switch mapping is as follows:

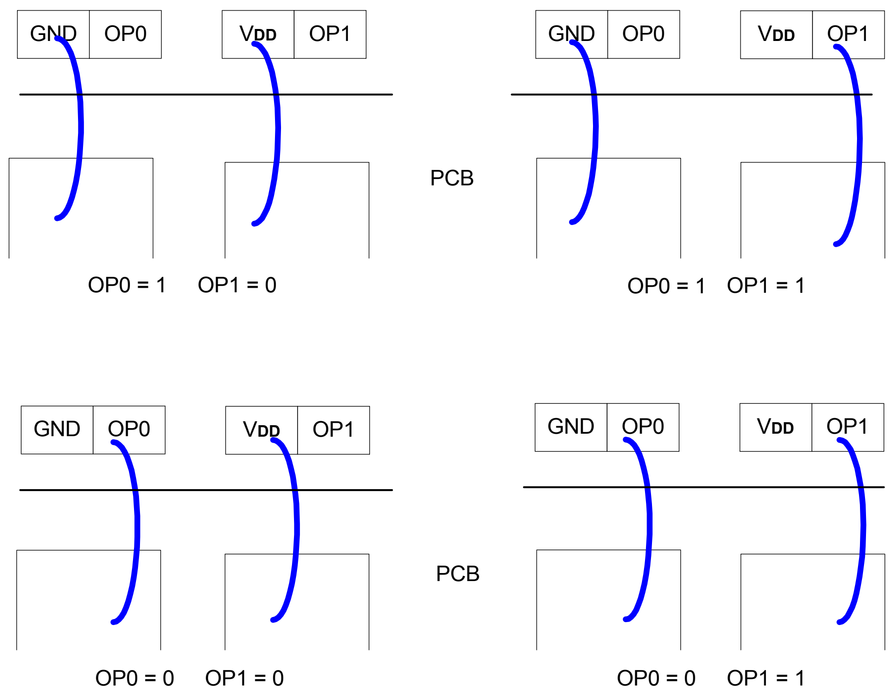
CPU Address	ROM Space BNK = 0	ROM Space BNK = 1	ROM Space BNK = 2	ROM Space BNK = 3	ROM Space BNK = 4	ROM Space BNK = 5
000 - 7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
800 - FFF	0800 - 0FFF (BANK 1)	1000 - 17FF (BANK 2)	1800 - 1FFF (BANK 3)	2000 - 27FF (BANK 4)	2800 - 2FFF (BANK 5)	3000 - 37FF (BANK 6)

CPU Address	ROM Space BNK = 6	ROM Space BNK = 7	ROM Space BNK = 8	ROM Space BNK = 9	ROM Space BNK = A
000 - 7FF	0000 - 07FF (BANK 0)	000 - 07FF (BANK 0)	000 - 07FF (BANK 0)	000 - 07FF (BANK 0)	000 - 07FF (BANK 0)
800 - FFF	3800 - 3FFF (BANK 7)	4000 - 47FF (BANK 8)	4800 - 4FFF (BANK 9)	5000 - 57FF (BANK 10)	5800 - 5FFF (BANK 11)

(d) System Register 0CH

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power-on
$0C	X	X	OP1	OP0	R	Bit0: Bonding option 0, internal weak drive Bit1: Bonding option 1, internal weak drive	Pull high Pull low
	X	X	0	1			Yes
	X	X	0	0		OP0 bond to GND	
	X	X	1	1		OP1 bond to VDD	
	X	X	1	0		OP0 bond to GND and OP1 bond to VDD	

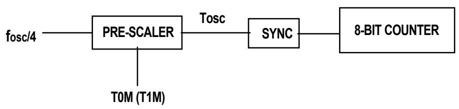
Up to 4 different bonding options are possible for the user's needs. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of OP1 and OP0 will differ depending on the bonding.



SH6513 Bonding Option

4. Timer

SH6513 has two 8-bit timers. Their operations are counting-up. The timers consist of an 8-bit counter and an 8-bit pre-load register.



Timer provides the following functions:

* Programmable interval timer
* Read counter value

(a) Timer0 Configuration and Operation:

The Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The timer counter can be initialized by writing data into the timer load register (TL0L, TL0H).

The low nibble should be written first, and then the high nibble. The timer counter is loaded with the contents of the load register automatically when the high nibble is written or a counter overflow happens. The timer overflow will generate an interrupt if the interrupt enable flag is set.

The timer can be programmed in several different system clock sources by setting the Timer Mode register (TM0).

(b) Timer Mode Register:

Timer Mode Register (TM0) is 4-bit register used for timer control as shown in Table 1. The Mode Register selects the input pulse sources to the timer.

Table 1. Timer 0 Mode Registers

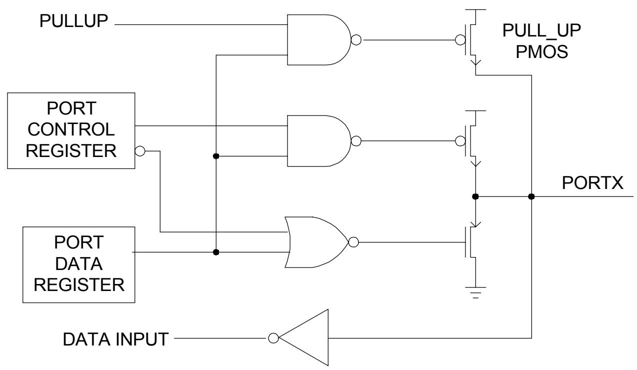
TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

5. I/O Ports

The MCU provides 8-bidirectional I/O pads. Each I/O pad contains pull-up MOS that is controlled by the program. The PORT control registers (PAOUT, PBOUT) control ON/OFF of the output buffer.

5.1. PORTA - B

These ports contain 8-bidirectional I/O ports.
The circuit configuration of PORTA - B as below.



I/O ports of SH6513 can be accessed by a read/write system register.

Memory map addresses are listed as follows:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA as output
$0B	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB as output
$0C	PPULL	LCDOFF	OP1	OP0	R W	OP1, OP0: Bonding Option LCDOFF: LCD Power control PPULL: Port pull-up control

5.2. Controlling the Pull-up MOS

These ports contain pull-up MOS controlled by the program. The register PPULL controls On/Off of all pull-up MOS simultaneously. Pull-up MOS is also controlled by the port data registers (PORTA, PORTB) of each port. So the pull-up MOS can be turned On/Off by writing data 1/0 to the port data register while the port is input.

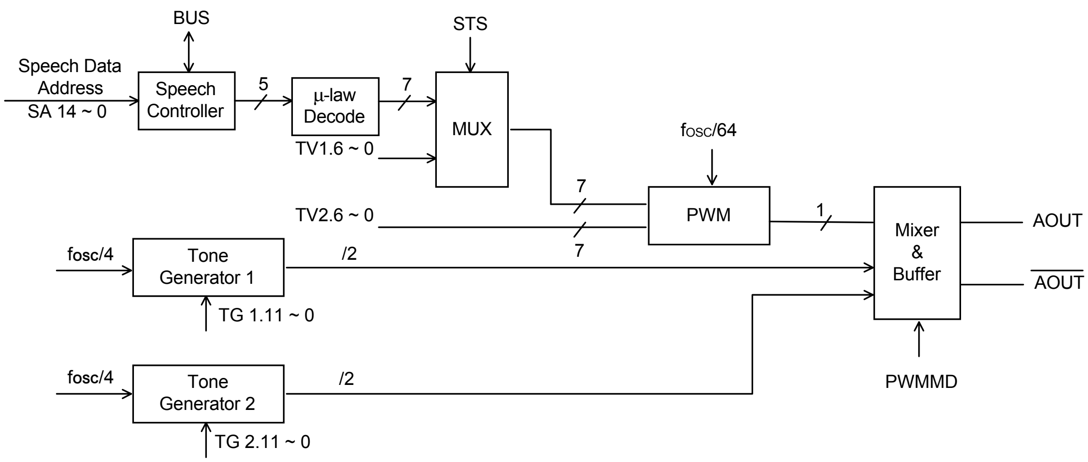
5.3. Port Interrupt

PORTB interrupt (falling edge) is not controlled by the Port I/O control register. This means that if an interrupt request (IEx is set to 1 & one port bit high go low) is been touched and that the condition is the other port bits are high level whenever the port bit is output or input.

6. Speech Synthesizer and Tone Generator

The built-in speech synthesizer uses 5-bit µ-Law PCM coding to synthesize speech. The speech ROM is shared with the program ROM, so the longest speech is about 10 seconds, depending on the sampling rate and the program ROM size.

(a) The Block Diagram of the Speech Synthesizer and Tone Generator



(b) The Speech ROM Mapping Control Register or Tone Generator ($16 - $19)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	SA3	SA2	SA1	SA0	W	SA3 - 0: Speech data start address low nibble
$17	SA7	SA6	SA5	SA4	W	SA7 - 4: Speech data start address
$18	SA11	SA10	SA9	SA8	W	SA11 - 8: Speech data start address
$19	STS	SA14	SA13	SA12	W	SA14 - 12: Speech data start address high nibble STS: Speech or tone generator selection bit

STS: Speech or tone generator 1 selection bit

0: Tone generator 1 (default) 1: Speech synthesizer

Speech addressing

Bit SA14 - SA0	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROM address	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

The format of speech data

Address	Speech Data			
	D15	D14 - D10	D9 - D5	D4 - D0
N (Start address)	0	SD2	SD1	SD0
N + 1	0	SD5	SD4	SD3
……	0	……	……	……
N + m (End address)	1	X	11111	SD (3m)

(c) Speech Control Register ($15)

$15	SEN	SST	SV1	SV0	W	Speech control bit or Tone generator 1 volume high nibble

SEN: Speech synthesizer enable flag

0: Speech synthesizer disable (default)   1: Speech synthesizer enable

SST: Speech synthesizer status flag

0: Speech synthesizer is idle   1: Speech synthesizer is playing

The control bit SST can be read by the CPU to check whether the speech is playing. While SST wrote to “ 1 ”, the rising edge triggers the speech to start playing, and the SST will reset to “ 0 ” when the speech ends and it will cause a speech end interrupt request simultaneously.

SV1, SV0: Speech synthesizer volume control

SV1	SV0	Volume Level
0	0	0
1	0	1
0	1	2
1	1	4

(d) Speech Synthesizer Sampling Rate Adjustment

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$0D	-	-	SPS	-	W	SPS: Speech frequency control

SPS: Speech synthesizer sampling rate adjustment

0: Speech playback sampling rate is 8KHz @4MHz oscillator

1: Speech playback sampling rate is 8KHz @2MHz oscillator

(e) Tone Generator Control Register

SH6513 has two 12-bit tone generators with the tone generator 1 being shared with the speech synthesizer. The tone generators generate the specific frequency of tone with square wave.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	TG1.3	TG1.2	TG1.1	TG1.0	W	Tone generator 1 low nibble
$17	TG1.7	TG1.6	TG1.5	TG1.4	W	Tone generator 1 middle nibble
$18	TG1.11	TG1.10	TG1.9	TG1.8	W	Tone generator 1 high nibble
$1C	TG2.3	TG2.2	TG2.1	TG2.0	W	Tone generator 2 low nibble
$1D	TG2.7	TG2.6	TG2.5	TG2.4	W	Tone generator 2 middle nibble
$1E	TG2.11	TG2.10	TG2.9	TG2.8	W	Tone generator 2 high nibble

(f) Tone Generator Volume Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	TV1.3	TV1.2	TV1.1	TV1.0	W	Tone generator 1 volume low nibble
$15	TG1EN	TV1.6	TV1.5	TV1.4	R/W	Tone generator 1 volume high nibble TG1EN: Tone generator 1 enable
$1A	TV2.3	TV2.2	TV2.1	TV2.0	W	Tone generator 2 volume low nibble
$1B	TG2EN	TV2.6	TV2.5	TV2.4	R/W	Tone generator 2 volume high nibble TG2EN: Tone generator 2 enable

The volume control register is 7-bit register used to control the output level of the tone generator.

TGxEN: Tone generator X enable

0: Tone generator X disable (default)   1: Tone generator X enable

Note: x = 1 or 2

(g) PWM mode selection

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$14	PWMMD	-	-	-	W	PWM mode selection

PWMMD: PWM mode selection

0: Single Ended (default), where the speech is output only to AOUT and $\overline{\text{AOUT}}$ outputs high impedance

1: Double Ended, where the speech is output to AOUT and $\overline{\text{AOUT}}$

Note: The AOUT and $\overline{\text{AOUT}}$ will output high impedance when both the speech synthesizer and the tone generator are not enabled.

(h) Programming notice

Never execute the "HALT" or "STOP" instruction while the Speech or Tone Generator are playing.

Music Table 1.

Following is the music scale reference table for the Tone Generator channel 1(or channel 2) under OSX = 4MHz.

Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%	Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%
B2	123.47	4050	02E	123.46	-0.01	**#F5**	739.99	676	D5C	739.64	-0.05
C3	130.81	3822	112	130.82	0.01	**G5**	783.99	638	D82	783.70	-0.04
#C3	138.59	3608	1E8	138.58	-0.01	**#G5**	830.61	602	DA6	830.56	-0.01
D3	146.83	3405	2B3	146.84	0.01	**A5**	880.00	568	DC8	880.28	0.03
#D3	155.56	3214	372	155.57	0.00	**#A5**	932.33	536	DE8	932.84	0.06
E3	164.81	3034	426	164.80	-0.01	**B5**	987.77	506	E06	988.14	0.04
F3	174.61	2863	4D1	174.64	0.02	**C6**	1046.5	478	E22	1046.0	-0.05
#F3	185.00	2703	571	184.98	-0.01	**#C6**	1108.7	451	E3D	1108.7	-0.01
G3	196.00	2551	609	196.00	0.00	**D6**	1174.7	426	E56	1173.7	-0.08
#G3	207.65	2408	698	207.64	-0.01	**#D6**	1244.5	402	E6E	1243.8	-0.06
A3	220.00	2273	71F	219.97	-0.01	**E6**	1318.5	379	E85	1319.3	0.06
#A3	233.08	2145	79F	233.10	0.01	**F6**	1396.9	358	E9A	1396.7	-0.02
B3	246.94	2025	817	246.91	-0.01	**#F6**	1480.0	338	EAE	1479.3	-0.05
C4	261.63	1911	889	261.64	0.01	**G6**	1568.0	319	EC1	1567.4	-0.04
#C4	277.18	1804	8F4	277.16	-0.01	**#G6**	1661.2	301	ED3	1661.1	-0.01
D4	293.66	1703	959	293.60	-0.02	**A6**	1760.0	284	EE4	1760.6	0.03
#D4	311.13	1607	9B9	311.14	0.00	**#A6**	1864.7	268	EF4	1865.7	0.05
E4	329.63	1517	A13	329.60	-0.01	**B6**	1975.5	253	F03	1976.3	0.04
F4	349.23	1432	A68	349.16	-0.02	**C7**	2093.0	239	F11	2092.1	-0.05
#F4	369.99	1351	AB9	370.10	0.03	**#C7**	2217.5	225	F1F	2222.2	0.22
G4	392.00	1276	B04	391.85	-0.04	**D7**	2349.3	213	F2B	2347.4	-0.08
#G4	415.30	1204	B4C	415.28	-0.01	**#D7**	2489.0	201	F37	2487.6	-0.06
A4	440.00	1136	B90	440.14	0.03	**E7**	2637.0	190	F42	2631.6	-0.21
#A4	466.16	1073	BCF	465.98	-0.04	**F7**	2793.8	179	F4D	2793.3	-0.02
B4	493.88	1012	C0C	494.07	0.04	**#F7**	2960.0	169	F57	2958.6	-0.05
C5	523.25	956	C44	523.01	-0.05	**G7**	3136.0	159	F61	3144.7	0.28
#C5	554.37	902	C7A	554.32	-0.01	**#G7**	3322.4	150	F6A	3333.3	0.33
D5	587.33	851	CAD	587.54	0.04	**A7**	3520.0	142	F72	3521.1	0.03
#D5	622.25	804	CDC	621.89	-0.06	**#A7**	3729.3	134	F7A	3731.3	0.05
E5	659.26	758	D0A	659.63	0.06	**B7**	3951.1	127	F81	3937.0	-0.36
F5	698.46	716	D34	698.32	-0.02	**C8**	4186.0	119	F89	4201.7	0.37

Music Table 2.

Following is the music scale reference table for the Tone Generator channel 1(or channel 2) under OSX =2MHz.

Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%	Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%
B1	61.73	4050	2E	61.73	0.00	**C5**	523.25	478	E22	523.01	-0.05
C2	65.10	3840	100	65.10	0.00	**#C5**	554.37	451	E3D	554.32	-0.01
#C2	69.29	3608	1E8	69.29	0.00	**D5**	587.33	426	E56	586.85	-0.08
D2	73.42	3405	2B3	73.42	0.00	**#D5**	622.25	402	E6E	621.89	-0.06
#D2	77.78	3214	372	77.78	0.00	**E5**	659.26	379	E85	659.63	0.06
E2	82.41	3034	426	82.40	-0.01	**F5**	698.46	358	E9A	698.32	-0.02
F2	87.31	2863	4D1	87.32	0.01	**#F5**	739.99	338	EAE	739.64	-0.05
#F2	92.50	2703	571	92.49	-0.01	**G5**	783.99	319	EC1	783.70	-0.04
G2	98.00	2551	609	98.00	0.00	**#G5**	830.61	301	ED3	830.56	-0.01
#G2	103.82	2408	698	103.82	0.00	**A5**	880.00	284	EE4	880.28	0.03
A2	110.00	2273	71F	109.99	-0.01	**#A5**	932.33	268	EF4	932.84	0.06
#A2	116.54	2145	79F	116.55	0.01	**B5**	987.77	253	F03	988.14	0.04
B2	123.47	2025	817	123.46	-0.01	**C6**	1046.5	239	F11	1046.0	-0.05
C3	130.81	1911	889	130.82	0.01	**#C6**	1108.7	225	F1F	1111.1	0.22
#C3	138.59	1804	8F4	138.58	-0.01	**D6**	1174.7	213	F2B	1173.7	-0.08
D3	146.83	1703	959	146.80	-0.02	**#D6**	1244.5	201	F37	1243.8	-0.06
#D3	155.56	1607	9B9	155.57	0.00	**E6**	1318.5	190	F42	1315.8	-0.21
E3	164.81	1517	A13	164.80	-0.01	**F6**	1396.9	179	F4D	1396.7	-0.02
F3	174.61	1432	A68	174.58	-0.02	**#F6**	1480.0	169	F57	1479.3	-0.05
#F3	185.00	1351	AB9	185.05	0.03	**G6**	1568.0	159	F61	1572.3	0.28
G3	196.00	1276	B04	195.92	-0.04	**#G6**	1661.2	150	F6A	1666.7	0.33
#G3	207.65	1204	B4C	207.64	-0.01	**A6**	1760.0	142	F72	1760.6	0.03
A3	220.00	1136	B90	220.07	0.03	**#A6**	1864.7	134	F7A	1865.7	0.05
#A3	233.08	1073	BCF	232.99	-0.04	**B6**	1975.5	127	F81	1968.5	-0.36
B3	246.94	1012	C0C	247.04	0.04	**C7**	2093.0	119	F89	2100.8	0.37
C4	261.63	956	C44	261.51	-0.04	**#C7**	2217.5	113	F8F	2212.4	-0.23
#C4	277.18	902	C7A	277.16	-0.01	**D7**	2349.3	106	F96	2358.5	0.39
D4	293.66	851	CAD	293.77	0.04	**#D7**	2489.0	100	F9C	2500.0	0.44
#D4	311.13	804	CDC	310.95	-0.06	**E7**	2637.0	95	FA1	2631.6	-0.21
E4	329.63	758	D0A	329.82	0.06	**F7**	2793.8	89	FA7	2809.0	0.54
F4	349.23	716	D34	349.16	-0.02	**#F7**	2960.0	84	FAC	2976.2	0.55
#F4	369.99	676	D5C	369.82	-0.05	**G7**	3136.0	80	FB0	3125.0	-0.35
G4	392.00	638	D82	391.85	-0.04	**#G7**	3322.4	75	FB5	3333.3	0.33
#G4	415.30	602	DA6	415.28	-0.01	**A7**	3520.0	71	FB9	3521.1	0.03
A4	440.00	568	DC8	440.14	0.03	**#A7**	3729.3	67	FBD	3731.3	0.05
#A4	466.16	536	DE8	466.42	0.06	**B7**	3951.1	63	FC1	3968.3	0.44
B4	493.88	506	E06	494.07	0.04	**C8**	4186.0	60	FC4	4166.7	-0.46

7. LCD

The LCD has 8 common signal pads, one controller, one LCD voltage generator, and 40 segment driver pads. The controller consists of display data RAM and a duty generator. The LCD is 1/8 duty, and 1/4 bias. The LCD data RAM is a dual port RAM that automatically transfers data to the segment. The LCD can be turned off with the internal LCDOFF register.

When the "STOP" instruction is executed, the LCD will be turned off, but the data of the LCD RAM remains the same as before executing the "STOP" instruction.

(a) LCD Control Register ($0C)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0C	- PPULL	- LCDOFF	OP1 -	OP0 -	R W	OP1, OP0: Bonding Option LCDOFF: LCD Power control PPULL: Port pull-up control

LCDOFF: LCD Power control

0: LCD on (default) 1: LCD off

When the LCD off, the COMx and SEGx are pulled low.

(b) LCD Frequency Control and Shared Output Control

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0D	O/S	PAS	SPS	LPS	W	SPS, LPS: Speech or LCD frequency control PAS: Set PORTA as LCD segment37 - 40 O/S: Set LCD segment 31 - 36 as output

O/S: Set LCD segments 31 - 3 6 as output

0: SEG 31 - 36 as LCD segment (default) 1: SEG 31 - 36 as outputs

PAS: Set PORTA as LCD segment37 - 40

0: SEG 37 - 40 as PORTA (default) 1: SEG 37 - 40 as LCD segments

LPS: LCD frequency control

LPS	LCD frame frequency	
	fosc = 4 MHz	fosc = 2 MHz
0 (default)	61 Hz	30 Hz
1	122 Hz	61 Hz

(c) LCD Voltage Generator

LCD voltages V1, V2, V3 are obtained using the resistor divider network. The LCD can be turned off with the LCDOFF register.

(d) LCD RAM Area Configuration:

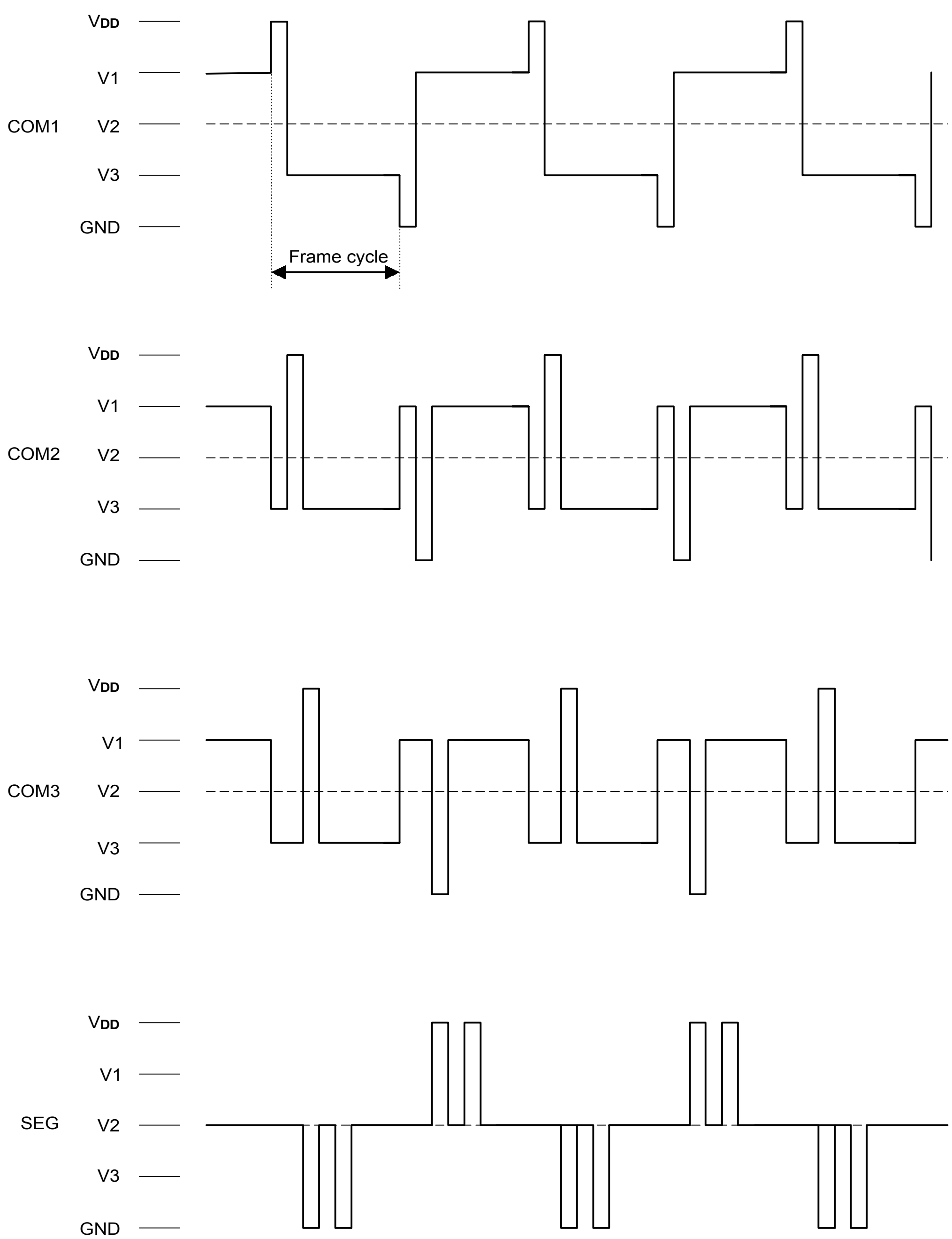
Address	Bit3	Bit2	Bit1	Bit0
$300	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32
$320	SEG33	SEG33	SEG33	SEG33
$321	SEG34	SEG34	SEG34	SEG34
$322	SEG35	SEG35	SEG35	SEG35
$323	SEG36	SEG36	SEG36	SEG36
$324	SEG37	SEG37	SEG37	SEG37
$325	SEG38	SEG38	SEG38	SEG38
$326	SEG39	SEG39	SEG39	SEG39
$327	SEG40	SEG40	SEG40	SEG40
Duty	**COM4**	**COM3**	**COM2**	**COM1**

LCD RAM Area Configuration (continued):

Address	Bit 3	Bit 2	Bit 1	Bit 0
$328	SEG1	SEG1	SEG1	SEG1
$329	SEG2	SEG2	SEG2	SEG2
$32A	SEG3	SEG3	SEG3	SEG3
$32B	SEG4	SEG4	SEG4	SEG4
$32C	SEG5	SEG5	SEG5	SEG5
$32D	SEG6	SEG6	SEG6	SEG6
$32E	SEG7	SEG7	SEG7	SEG7
$32F	SEG8	SEG8	SEG8	SEG8
$330	SEG9	SEG9	SEG9	SEG9
$331	SEG10	SEG10	SEG10	SEG10
$332	SEG11	SEG11	SEG11	SEG11
$333	SEG12	SEG12	SEG12	SEG12
$334	SEG13	SEG13	SEG13	SEG13
$335	SEG14	SEG14	SEG14	SEG14
$336	SEG15	SEG15	SEG15	SEG15
$337	SEG16	SEG16	SEG16	SEG16
$338	SEG17	SEG17	SEG17	SEG17
$339	SEG18	SEG18	SEG18	SEG18
$33A	SEG19	SEG19	SEG19	SEG19
$33B	SEG20	SEG20	SEG20	SEG20
$33C	SEG21	SEG21	SEG21	SEG21
$33D	SEG22	SEG22	SEG22	SEG22
$33E	SEG23	SEG23	SEG23	SEG23
$33F	SEG24	SEG24	SEG24	SEG24
$340	SEG25	SEG25	SEG25	SEG25
$341	SEG26	SEG26	SEG26	SEG26
$342	SEG27	SEG27	SEG27	SEG27
$343	SEG28	SEG28	SEG28	SEG28
$344	SEG29	SEG29	SEG29	SEG29
$345	SEG30	SEG30	SEG30	SEG30
$346	SEG31	SEG31	SEG31	SEG31
$347	SEG32	SEG32	SEG32	SEG32
$348	SEG33	SEG33	SEG33	SEG33
$349	SEG34	SEG34	SEG34	SEG34
$34A	SEG35	SEG35	SEG35	SEG35
$34B	SEG36	SEG36	SEG36	SEG36
$34C	SEG37	SEG37	SEG37	SEG37
$34D	SEG38	SEG38	SEG38	SEG38
$34E	SEG39	SEG39	SEG39	SEG39
$34F	SEG40	SEG40	SEG40	SEG40
Duty	**COM8**	**COM7**	**COM6**	**COM5**

(e) LCD Waveform

The output waveform of 1/8 duty and 1/4 bias is shown below.



8. Interrupt

Three interrupt sources are available on the SH6513:

- Speech End interrupt (SE)
- Timer0 interrupt (TMR0)
- PortB falling edge detection interrupt ($\overline{PB}$)

(a) Interrupt Control Bits and Interrupt Service:

- Interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. These flags are cleared to 0 at initialization.

Address	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
$00	IES	IET0	-	IEP	Interrupt enable flags
$01	IRQSE	IRQT0	-	IRQP	Interrupt request flags

- An interrupt request begins when IRQx is set to 1 and IEx is 1. At this time, the interrupt will activate and the vector address will follow from the priority PLA corresponding to the interrupt source. When an interrupt occurs, the PC and CY flags will be saved in the stack memory and jump to an interrupt service vector address. After an interrupt occurs, all interrupt enable flags (IEx) are automatically reset to 0, so that any interrupt is disabled. The IRQx, which caused the interrupt, must be reset by software in the interrupt service routine. When IEx is set to 1 again, SH6513 can service multi-level interrupts.

(b) Vector Address and Interrupt Priority

Priority	Interrupt source
1 (Most)	RESET
2	Speech end
3	Timer0
4 (Least)	PB

9. System Clock and Oscillation Circuit

The system clock generator produces clock pulses supplied to the CPU and to on-chip peripherals.

- Instruction cycle time

  1 μs for 4 MHz clock

10. HALT or STOP

- After execution of HALT, SH6513 will enter HALT. In HALT, the CPU will stop operating, but the peripheral circuit (timer) will operate.

- After execution of STOP, SH6513 will enter STOP. In STOP, the entire chip (including oscillator) will stop operating, and the LCD automatically powers-off.

- In HALT, SH6513 will wake up if an interrupt occurs.
- In STOP, SH6513 will wake up if a port interrupt occurs.

11. Warm-up Timer

The warm-up timer eliminates an initial oscillation instability in the following two cases:

(1) Power-on reset

(2) Wake-up from STOP

The warm-up time interval is 32 clock cycles.

12. System Reset

- Hardware reset input
- Warm-up timer for power-on reset

(a) Initial State

Hardware	After Power-on Reset
Program Counter	$000
CY	Undefined
Data Memory	Undefined
AC	Undefined
Timer 0 Counter	Undefined
Timer 0 Load Register	Undefined
Timer 0 mode Register	$0
Interrupt Enable Flags	0
Interrupt Request Flags	0
DPH, DPM, DPL	Undefined
TBR	Undefined
LCD driver output	0 (active)
LCD frequency control (LPS)	0
Speech sampling rate control (SPS)	0
Set PORTA as LCD segment 37 - 40 (PAS)	0 (PORTA)
Set LCD segment 31 - 36 as output (O/S)	0 (segment 31 - 36)
PAOUT	$0 (input)
PBOUT	$0 (input
PPULL	0 (disable)
Tone generator enable	0 (disable)
Tone generator volume	$0
STS	0 (Tone generator selected)
Speech volume	$0
Speech data address	Undefined
PWM mode (PWMMD)	0 (Single ended)
Speech enable (SEN)	0 (Disable)
Bank register	$0

13. Instruction Set

All instructions are one cycle and one-word instructions. The characteristics are memory-oriented operation.
Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I + 1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx I I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, the EORIM mnemonic is EORI. However, EORI has the identical operation as EORIM. The same is true for the ORIM with respect to ORI, and the ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X,I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not include p)	
RTNW H; L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where

PC	Program counter	l	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank = 000
P	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Ratings*

DC Supply Voltage . . . . -0.3V to + 7V

Input Voltage . . . .-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . .-10°C to + 60°C

Storage Temperature . . . . -55°C to + 125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

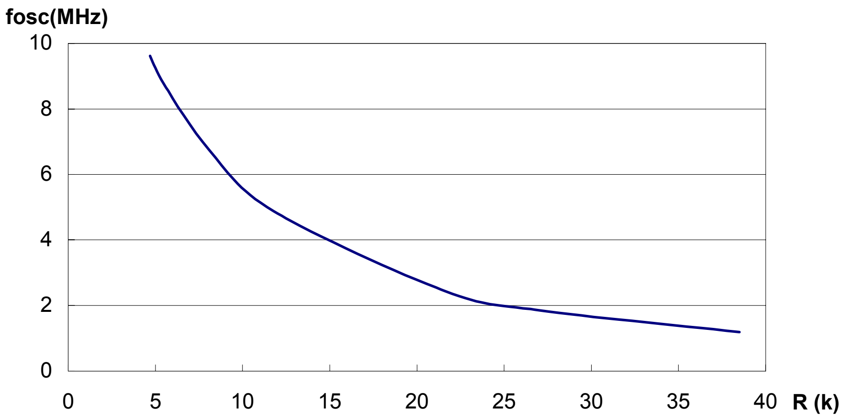
DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 4 MHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	2.4	3.0	5.5	V	
I_{OP}	Operating Current	-	0.8	1.5	mA	All output unload
I_{SB}	Standby Current (Stop)	-	-	1	μA	All output unload
I_{IL}	Input Current	-1	-	1	μA	V(input) = 3.0V
V_{IH1}	Input High Voltage	0.7 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB
V_{IL1}	Input Low Voltage	-0.3	-	0.3 X V_{DD}	V	PORTB, PORTB
V_{IH2}	Input High Voltage	0.8 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{\text{RESET}}$, TEST
V_{IL2}	Input Low Voltage	-0.3	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, TEST
V_{OH1}	Output high voltage	V_{DD} - 0.7	-	-	V	PORTA, PORTB, AOUT and $\overline{\text{AOUT}}$, I_{OH1} = -2mA
V_{OL1}	Output low voltage	-	-	0.6	V	PORTA, PORTB, AOUT and $\overline{\text{AOUT}}$, I_{OL1} = 2mA
V_{OH2}	Output high voltage	V_{DD} - 0.7	-	-	V	SEG31 - 36 set to output port, I_{OH2} = -1mA
V_{OL2}	Output low voltage	-	-	0.6	V	SEG31 - 36 set to output port, I_{OL2} = 1mA
R_{PU}	Pull-up Resistance	-	130	200	KΩ	PORTA and PORTB, $V_{I/O}$ = 0V
I_{LCD}	LCD lighting current	-	30	-	μA	Exclude CPU operation current

AC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 4 MHz, unless otherwise specified)

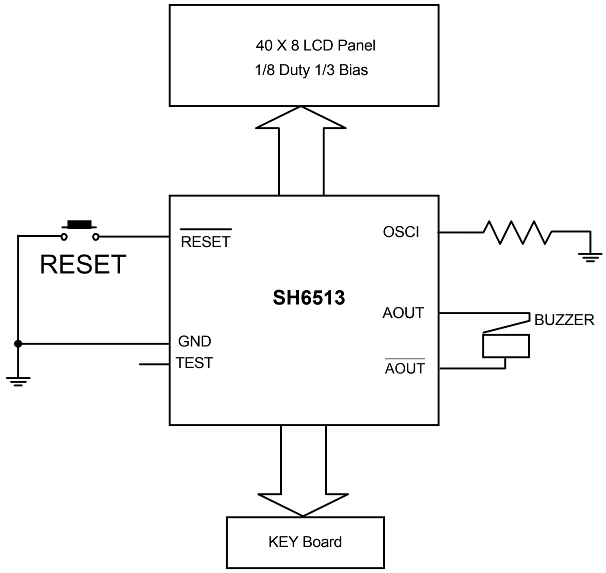
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
|ΔF|/F	Frequency Stability	-	6	9	%	[F(3.0) - F(2.5)] / F(3.0)
|ΔF|/F	Frequency Variation	-	-	10	%	[F(MAX) - F(TYP)] / F(TYP)

Typical RC oscillator R-F curve: (for reference only)

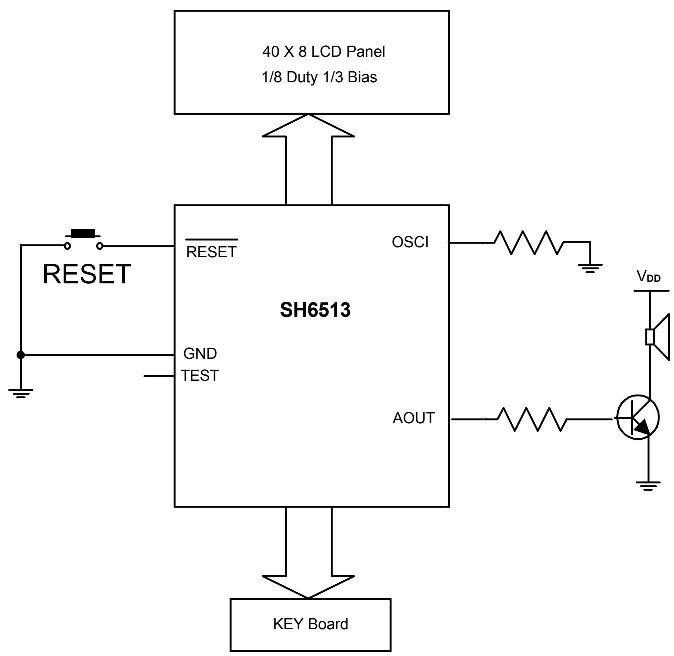


Application Circuit (for reference only):

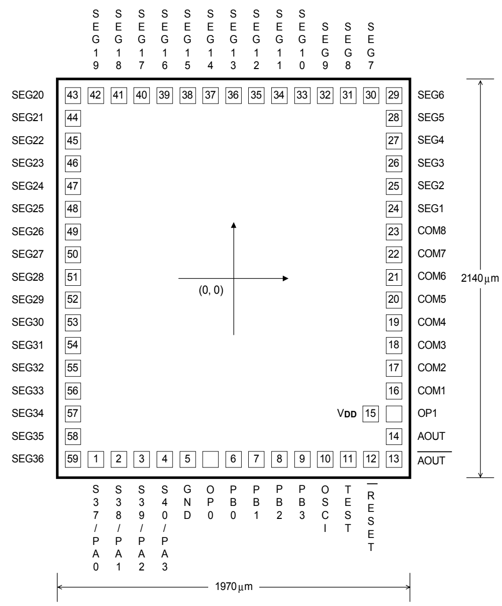
AP1:



AP2:



Bonding Diagram



❖Substrate connects to GND.

Pad No	Designation	X	Y
1	SEG37	-707.5	-944.5
2	SEG38	-587.5	-944.5
3	SEG39	-467.5	-944.5
4	SEG40	-347.5	-944.5
5	GND	-227	-944.5
6	PB0	0	-944.5
7	PB1	118	-944.5
8	PB2	238	-944.5
9	PB3	358	-944.5
10	OSCI	478	-944.5
11	TEST	598	-944.5
12	$\overline{\text{RESET}}$	718	-944.5
13	$\overline{\text{AOUT}}$	864	-944.5
14	AOUT	864	-819.5
15	VDD	763.95	-691.5
16	COM1	864	-576.5
17	COM2	864	-461.5
18	COM3	864	-346.5
19	COM4	864	-231.5
20	COM5	864	-116.5

Pad No	Designation	X	Y
21	COM6	864	-1.5
22	COM7	864	113.5
23	COM8	864	228.5
24	SEG1	864	343.5
25	SEG2	864	458.5
26	SEG3	864	573.5
27	SEG4	864	688.5
28	SEG5	864	808.5
29	SEG6	864	946.2
30	SEG7	708	946.15
31	SEG8	588	946.15
32	SEG9	463	946.15
33	SEG10	343	946.15
34	SEG11	223	946.15
35	SEG12	108	946.15
36	SEG13	-7	946.15
37	SEG14	-122	946.15
38	SEG15	-237	946.15
39	SEG16	-352	946.15
40	SEG17	-467	946.15

Pad No	Designation	X	Y
41	SEG18	-582.65	946.15
42	SEG19	-702.65	946.15
43	SEG20	-860.3	946.15
44	SEG21	-860.3	808.5
45	SEG22	-860.3	688.5
46	SEG23	-860.3	573.5
47	SEG24	-860.3	458.5
48	SEG25	-860.3	343.5
49	SEG26	-860.3	228.5
50	SEG27	-860.3	113.5
51	SEG28	-860.3	-1.5
52	SEG29	-860.3	-116.5
53	SEG30	-860.3	-231.5
54	SEG31	-860.3	-346.5
55	SEG32	-860.3	-461.5
56	SEG33	-860.3	-576.5
57	SEG34	-860.3	-691.5
58	SEG35	-860.3	-811.5
59	SEG36	-860.3	-944.5

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BONDING OPTION:				
	OP0	-127	-944.5	for GND
	OP1	864	-691.5	for VDD

Ordering Information

Part No.	Package
SH6513H	Chip Form