SINO WEALTH

SH6603

PRELIMINARY

Mask 4-Bit Microcontroller with LCD Driver

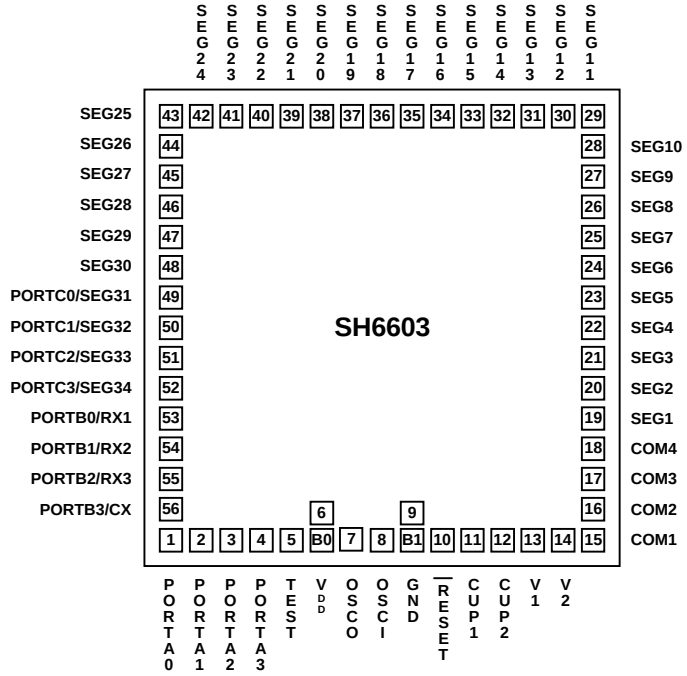
Features

- SH6610C-based single-chip 4-bit microcontroller with LCD driver
- ROM: 2048 X 16 bits
- RAM: 128 X 4 bits (data memory)
- Operation Voltage Range: 2.2V - 3.6V (typical 3.0V)
- 12 CMOS bi-directional I/O pins
- 4 level subroutine nesting (including interrupts)
- Two 8-bit timers with pre-divider circuit
- Built-in watch dog timer
- 4 priority interrupt sources:
  - External interrupt (rising edge)
  - Timer0 interrupt
  - Timer1 interrupt
  - PortB PortC interrupt (rising edge)
- Clock source: 32.768KHz crystal or 131K RC (type is selected by mask option)
- Instruction cycle time:
  - 4/32.768KHz (≈ 122μs) for 32.768KHz crystal
  - 4/131KHz (≈ 31μs) for 131KHz RC
- LCD driver: 4 X 34 (1/4,1/3, 1/2 duty, 1/3,1/2 bias)
- Built-in EL-light driver
- Built-in Resistor to Frequency converter circuit
- Built-in voltage charge pump circuit
- Built-in one channel PSG
- Two low power operation modes: HALT or STOP
- Low power consumption (I_{SB} < 2μA, 32.768KHz, 3V)
- Bonding option for multi-code software
- Available in CHIP FORM

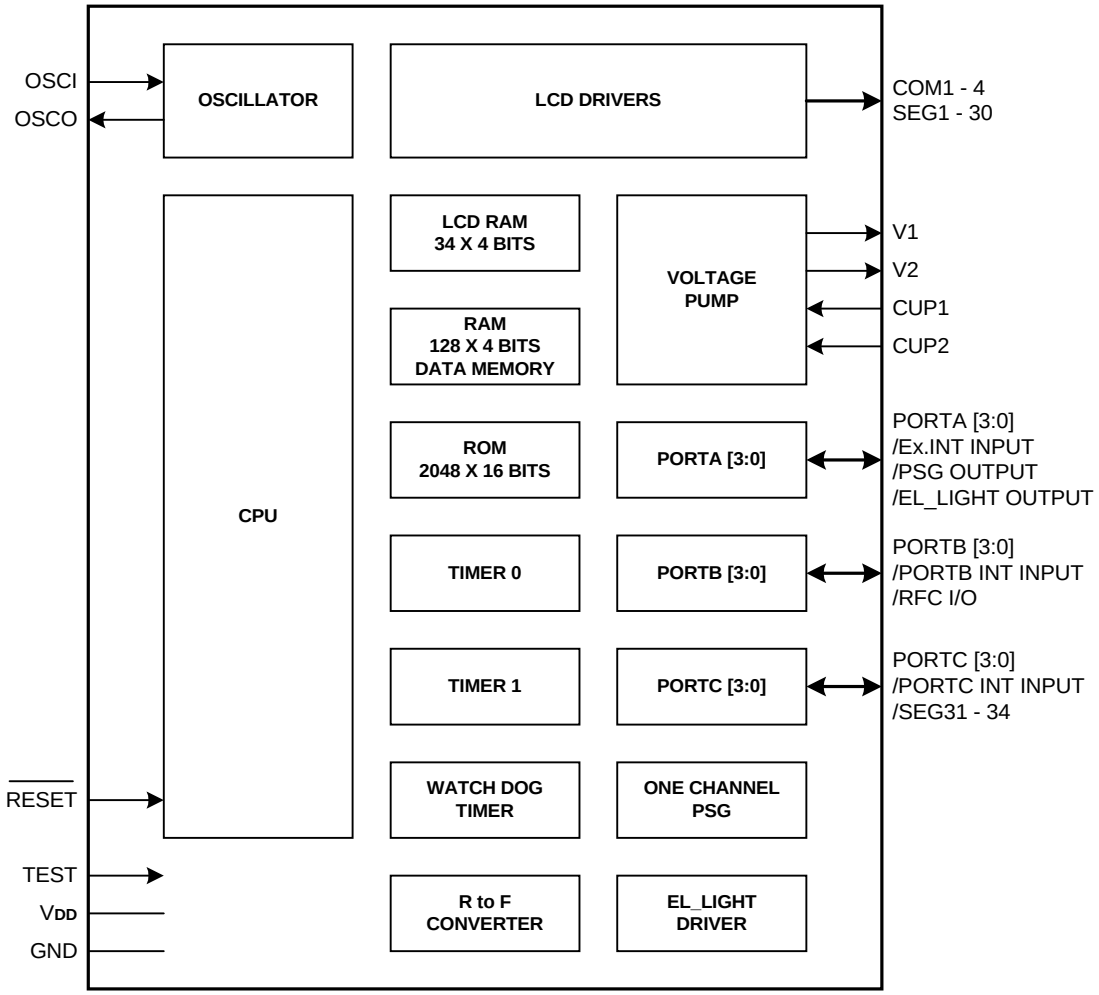
General Description

SH6603 is a single-chip microcontroller integrated with an SH6610C CPU core, SRAM, program ROM, programmable I/O driving buffers, 8-bit timer, PSG generator, LCD driver, EL-light driver, Resistor to Frequency converter circuit and watch dog timer.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Designation	I/O	Description
1	PORTA0	I/O I O	Bit programmable I/O Vector external interrupt. (active rising edge) Shared with PSG output $\overline{BD}$
2	PORTA1	I/O O	Bit programmable I/O pins Shared with PSG output BD
3, 4	PORTA [2:3]	I/O O	Bit programmable I/O pins Shared with EL-light output ELC (PA2), ELP (PA3)
5	TEST	I	Test pad input. (High active with test mode, internal pull down) No connect for user
6	V_{DD} B0	P I	Power supply 2.2 - 3.6V for SH6603 Bonding option, internally pull-low
7	OSCO	O	Oscillator output pad, connect to crystal oscillator
8	OSCI	I	Oscillator input pad, connect to crystal or external resistor
9	GND B1	P I	Ground pad Bonding option, internally pull-high
10	$\overline{RESET}$	I	Pad reset input. (Low active, internal pull up)
11	CUP1	I	Connect to voltage booster capacitor (-)
12	CUP2	I	Connect to voltage booster capacitor (+)
13, 14	V1, V2	O	Power supply pad for LCD driver
15 - 18	COM1 - 4	O	Common signal output for LCD display
29 - 48	SEG1 - 30	O	Segment signal output for LCD display
49 - 52	PORTC [0:3]	I/O I O	Bit programmable I/O pins.(Direct drive analog movement) Vector port interrupt. (active rising edge) Shared with SEG31 - 34
53 - 56	PORTB [0:3]	I/O I O I	Bit programmable I/O pins Vector port interrupt. (active rising edge) PB.0 - 2 shared with RX1 - 3 PB.3 shared with CX.(RFC counter input pin)

Total 56 pads

Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stacks.

2. ROM

The ROM can address 2048 words X 16 bits of program area from $0000H to $07FFH.

(a) Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
000H	JMP instruction	Jump to RESET service routine
001H	JMP instruction	Jump to External interrupt service routine
002H	JMP instruction	Jump to TIMER0 service routine
003H	JMP instruction	Jump to TIMER1 service routine
004H	JMP instruction	Jump to PBC service routine

*JMP instruction can be replaced by any instruction.

(b) Table Data Reference

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) is placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, A)). The address is determined by RTNW to return look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

3. RAM

Built-in RAM contains of general-purpose data memory, LCD RAM and system register.

(a) RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

$000 - $01F: System register and I/O

$020 - $09F: Data memory (128 X 4 bits, divided into 2 banks).

$300 - $321: LCD RAM space (34 X 4 bits).

(b) Data Memory

Data memory is organized as 128 X 4 bits ($020 - $09F). Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

(c) Data Pointer

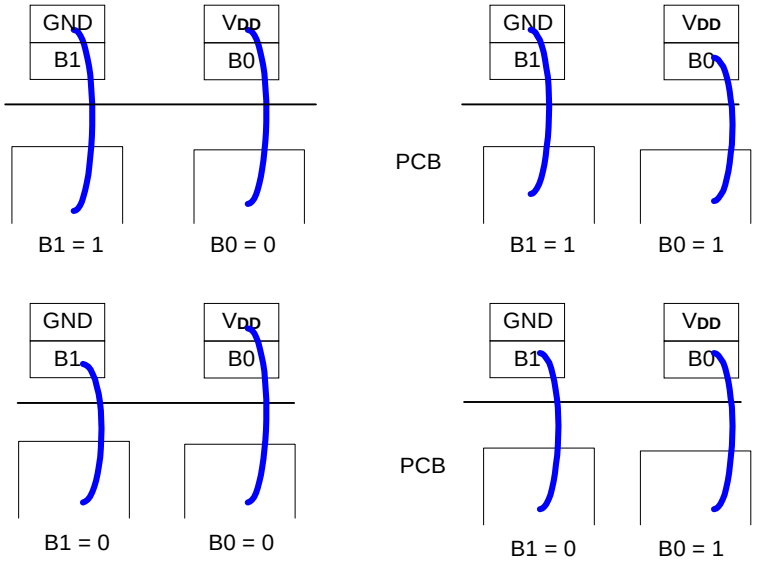
The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 comes from DPH, DPM and DPL.

(d) Configuration of System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit0 - 2: Timer0 Mode register
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit0 - 2: Timer1 Mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load / counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load / counter register high nibble
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load / counter register low nibble
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load / counter register high nibble
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	RF/P	EL/P	S/P	PAM	R/W	PAM: Set PORTA1 - 0 as PSG output S/P: Set PORTC as segment output EL/P: Set PORTA3 - 2 as EL light output RF/P: Set PORTB as R-F converter
$0C	ENX	RX3EN	RX2EN	RX1EN	R/W	RX1, 2, 3EN: Enables the RC oscillation of RX1, 2, 3 ENX: RFC counter on
$0D	ELON	ELF	ELPF	OSCS	R/W	ELON: EL-LIGHT on/off control ELPF: EL-LIGHT driver charge frequency select ELF: EL-LIGHT driver discharge frequency select OSCS: OSC type selection
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	LPS1	LPS0	B1	B0	R R/W	B1, B0: Bonding option LPS1 - 0: LCD frequency control
$14	LCDOFF	BIAS	DUTY 1	DUTY0	R/W	DUTY1 - 0: Set LCD duty BIAS: Set LCD bias LCDOFF: LCD on / off control
$15	PPULL	PS1	PS0	PSGEN	R/W	PSGEN: PSG enable PS1 - 0: PSG Prescaler PPULL: Port pull-down control
$16	C1.3	C1.2	C1.1	C1.0	W	C1.0 - 1.3: PSG low nibble
$17	-	C1.6	C1.5	C1.4	W	C1.6 - 1.4: PSG high nibble
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	RFL.3	RFL.2	RFL.1	RFL.0	R/W	RFC counter register low nibble
$1C	RFML.3	RFM.2	RFML.1	RFML.0	R/W	RFC counter register middle_low nibble
$1D	RFMH.3	RFMH.2	RFMH.1	RFMH.0	R/W	RFC counter register middle_high nibble
$1E	RFH.3	RFH.2	RFH.1	RFH.0	R/W	RFC counter register high nibble
$1F	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit0 - 2: Watch dog timer control WD: Watchdog timer overflow flag. (Read only)

System Register $13: (Bonding option)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$13	LPS1	LPS0	B1	B0	R R/W	B1, B0: Bonding option LPS1 - 0: LCD frequency control	00XX
	X	X	1	0		Default bonding option	
	X	X	0	0		B1 bond to GND	
	X	X	1	1		B0 bond to V_{DD}	
	X	X	0	1		B1 bond to GND & B0 bond to V_{DD}	



SH6603 Bonding Option

Up to 4 different bonding options is possible for the user's needs. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

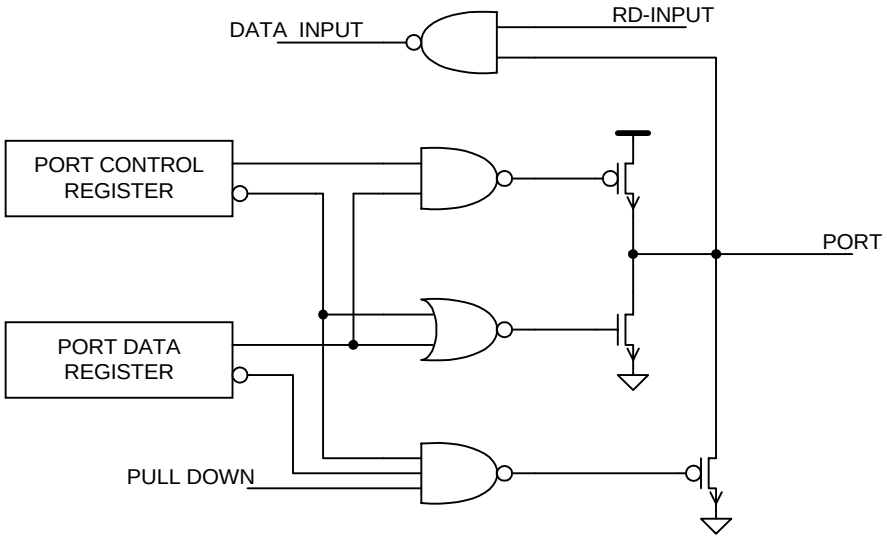
4. I/O Port

The MCU provides 12 I/O ports. Each I/O port contains pull-down MOS controllable by the program. Bit3 of the PMOD register controls On/Off of all pull-downs MOS simultaneously. Pull-down MOS is controlled by the port data registers (PDR) of each port also (Write “1” could turn off the pull-down MOS). So the pull-down MOS can be turned on and off individually. The port control register (PCR) controls ON/OFF of the output buffer.

PortA.0 can be shared with PSG output $\overline{BD}$, PortA.1 can be shared with PSG output BD, and PortA.2&3 can be shared with EL light output. PortB.0-3 can be shared with Resistor to Frequency converter circuit I/O. PortC.0-3 can be shared with segment output.

System Register $0B:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$0B	RF/P	EL/P	S/P	PAM	R/W	PAM: Set PORTA1 - 0 as PSG output S/P: Set PORTC as segment output EL/P: Set PORTA3 - 2 as EL light output RF/P: Set PORTB as R-F converter	0000
	X	X	X	0		PORTA0-1 as I/O port	Yes
	X	X	X	1		PORTA0-1 as PSG output	
	X	X	0	X		PORTC as I/O port	Yes
	X	X	1	X		PORTC as segment output	
	X	0	X	X		PORTA3 - 2 as I/O port	Yes
	X	1	X	X		PORTA3 - 2 as EL light output	
	0	X	X	X		PORTB as I/O port	Yes
	1	X	X	X		PORTB as RFC I/O port	



Port I/O Data Register: (PDR)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA	XXXX
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB	XXXX
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC	XXXX

Port I/O Control Register: (PCR)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	System Reset
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control	0000

I/O control register:

PACR.X, PBCR.X, PCCR.X (X = 0, 1, 2, 3)

0: Set I/O as an input buffer.

1: Set I/O as an output buffer.

Port Function Control: (PMOD)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark	System Reset
$15	PPULL	PS1	PS0	PSGEN	R/W	PSGEN: PSG enable PS1 - 0: PSG Prescaler PPULL: Port pull-down control	0000

PPULL Port Pull-down MOS enables control

0: Disable PORT pull-down MOS

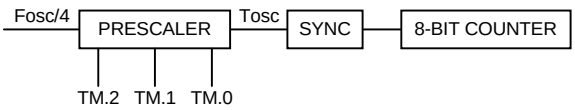
1: Enable PORT pull-down MOS

5. Timer

SH6603 has two 8-bit timers. The timer / counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-bit prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

(a) Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

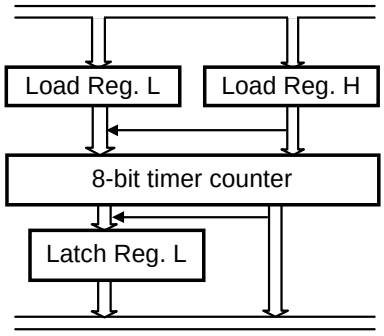
Low nibble first;

High nibble to update the counter

Read Operation:

High Nibble first;

Low nibble followed.



(b) Timer Mode Register

The timer can be programmed in several different prescaler ratios by setting Timer Mode register (TM0, TM1).

The 8-bit counter prescaler overflow output pulses. The Timer Mode registers (TM0, TM1) are 3-bit registers used for the timer control as shown in Table1 and Table 2. These mode registers select the input pulse sources into the timer.

Table 1: Timer0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

Table 2: Timer1 Mode Register ($03)

TM1.2	TM1.1	TM1.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

6. System Clock

SH6603 has one clock source. OSC is 32.768KHz crystal or 131KHz RC determined by mask option. The OSC generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals (TIMER0, TIMER1, LCD, PSG, Watchdog timer). System clock = Fosc/4.

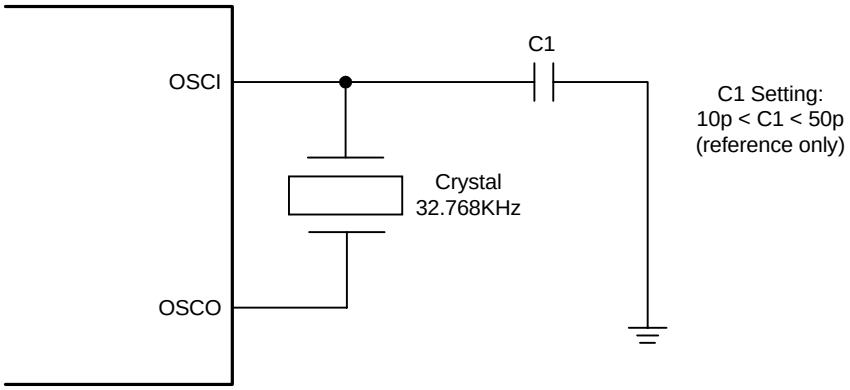
(a) Instruction cycle time:

(1) 4/32.768KHz (≈ 122μs) for 32.768KHz oscillator.

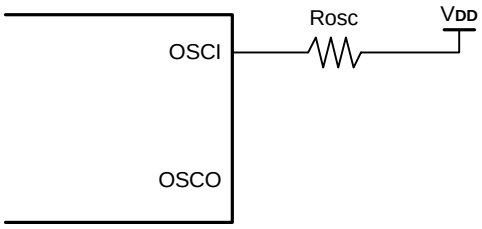
(2) 4/131KHz (≈ 31μs) for 131KHz oscillator.

(b) Oscillator

(1) 32.768KHz crystal:



(2) 131K RC:



System Register $0D (Bit0): Oscillator type select register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$0D	ELON	ELF	ELPF	OSCS	R/W	ELON: EL-LIGHT on/off control ELPF: EL-LIGHT driver charge frequency select ELF: EL-LIGHT driver discharge frequency select OSCS: OSC type selection	0000
	X	X	X	0		131KHz RC Oscillator	Yes
	X	X	X	1		32.768KHz crystal Oscillator	

8. PSG

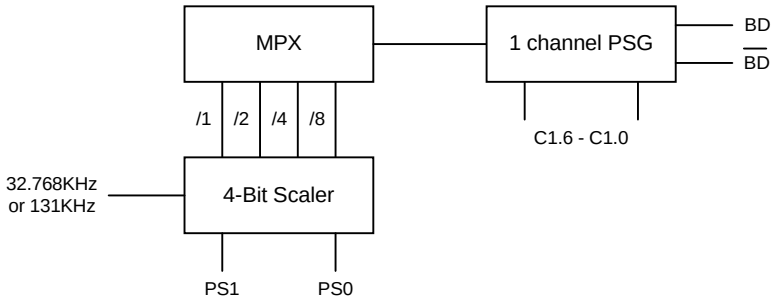
One Channel PSG is provided. It is a 7-bit pseudo random counter. To reduce power consumption, disable the sound effect generator during both STOP and HALT.

PSG control register $15 – 17:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$15	PPULL	PS1	PS0	PSGEN	R/W	PSGEN: PSG enable PS1 - 0: PSG Prescaler PPULL: Port pull-down control	0000
$16	C1.3	C1.2	C1.1	C1.0	W	PSG low nibble	0000
$17	-	C1.6	C1.5	C1.4	W	PSG high nibble	0000

PSGEN: 0 = PSG disable, the "BD" output low
1 = PSG enable

PS1	PS0	Prescaler Ratio	Clock source	Actual Clock
0	0	/1	32KHz or 131 KHz	32 KHz or 131KHz
0	1	/2	32KHz or 131 KHz	16 KHz or 65.5KHz
1	0	/4	32KHz or 131 KHz	8 KHz or 32KHz
1	1	/8	32KHz or 131 KHz	4 KHz or 16KHz



PSG actual clock can be selected by changing register $15H, as PSG - CLK is selected, the only way to get different tone is changing the value of N. The value of N is created by a group of counters (LSFR). Different initial data written to these counters, different N is created.

$$PSG\ output\ frequency = \frac{Actual\ Clock}{2 \times N}$$

The Value of N is corresponding to the Register $16H and $17H (C1.6 - C1.0) as shown in the following table

LSFR (C1.6 - C1.0)	N	LSFR (C1.6 - C1.0)	N	LSFR (C1.6 - C1.0)	N	LSFR (C1.6 - C1.0)	N
01	127	16	95	12	63	4B	31
02	126	2C	94	24	62	17	30
04	125	59	93	49	61	2E	29
08	124	33	92	13	60	5D	28
10	123	67	91	26	59	3B	27
20	122	4E	90	4D	58	77	26
41	121	1D	89	1B	57	6E	25
03	120	3A	88	36	56	5C	24
06	119	75	87	6D	55	39	23
0C	118	6A	86	5A	54	73	22
18	117	54	85	35	53	66	21
30	116	29	84	6B	52	4C	20
61	115	53	83	56	51	19	19
42	114	27	82	2D	50	32	18
05	113	4F	81	5B	49	65	17
0A	112	1F	80	37	48	4A	16
14	111	3E	79	6F	47	15	15
28	110	7D	78	5E	46	2A	14
51	109	7A	77	3D	45	55	13
23	108	74	76	7B	44	2B	12
47	107	68	75	76	43	57	11
0F	106	50	74	6C	42	2F	10
1E	105	21	73	58	41	5F	9
3C	104	43	72	31	40	3F	8
79	103	07	71	63	39	7F	7
72	102	0E	70	46	38	7E	6
64	101	1C	69	0D	37	7C	5
48	100	38	68	1A	36	78	4
11	99	71	67	34	35	70	3
22	98	62	66	69	34	60	2
45	97	44	65	52	33	40	1
0B	96	09	64	25	32		

9. LCD Driver

The LCD driver contains a controller, voltage generator, 4 common signal pads, and 34 segment driver pads. There are two bias modes (1/3 and 1/2 bias) and three duty mode (1/4, 1/3 and 1/2 duty) that are programmable, The LCD data RAM is a dual port RAM that transfers data to segment pads automatically without a program control.

PORTC can be set as LCD SEG31 - 34. It's selected by S/P the bit1 of system register $0B. When use as I/O ports, the data in LCD RAM won't effect the I/O input and output data. Also, when use as LCD output, the data of I/O RAM won't effect LCD output. LCD RAM can be used as data memory if needed.

When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM is the same before execution the "STOP" instruction.

When LCD off, both COMMON and SEGMENT output 0V.

(a) LCD Control Register

LCD Control Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$13	LPS1	LPS0	B1	B0	R R/W	B1, B0: Bonding option LPS1 - 0: LCD frequency control	00XX
	0	0	X	X		LCD clock frequency = f**osc**/128	Yes
	0	1	X	X		LCD clock frequency = f**osc**/256	
	1	0	X	X		LCD clock frequency = f**osc**/512	
	1	1	X	X		LCD clock frequency = f**osc**/1024	

Frame frequency f_{FRM} = LCDCLK/8 @1/4 duty or 1/2 duty

Frame frequency f_{FRM} = LCDCLK/6 @1/3 duty

LCD Control Register $14:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$14	LCDOFF	BIAS	DUTY 1	DUTY0	R/W	DUTY1 - 0: Set LCD duty BIAS: Set LCD bias LCDOFF: LCD on / off control	0000
	X	X	0	X		1/4 duty	Yes
	X	X	1	0		1/3 duty	
	X	X	1	1		1/2 duty	
	X	0	X	X		1/3 bias	Yes
	X	1	X	X		1/2 bias	
	0	X	X	X		LCD on	Yes
	1	X	X	X		LCD off	

Note: When LCD off the LCD voltage converts circuit is used.

(b) Configuration of LCD RAM Area

Segments 1 - 34, 1/4duty

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1	311H	SEG18	SEG18	SEG18	SEG18
301H	SEG2	SEG2	SEG2	SEG2	312H	SEG19	SEG19	SEG19	SEG19
302H	SEG3	SEG3	SEG3	SEG3	313H	SEG20	SEG20	SEG20	SEG20
303H	SEG4	SEG4	SEG4	SEG4	314H	SEG21	SEG21	SEG21	SEG21
304H	SEG5	SEG5	SEG5	SEG5	315H	SEG22	SEG22	SEG22	SEG22
305H	SEG6	SEG6	SEG6	SEG6	316H	SEG23	SEG23	SEG23	SEG23
306H	SEG7	SEG7	SEG7	SEG7	317H	SEG24	SEG24	SEG24	SEG24
307H	SEG8	SEG8	SEG8	SEG8	318H	SEG25	SEG25	SEG25	SEG25
308H	SEG9	SEG9	SEG9	SEG9	319H	SEG26	SEG26	SEG26	SEG26
309H	SEG10	SEG10	SEG10	SEG10	31AH	SEG27	SEG27	SEG27	SEG27
30AH	SEG11	SEG11	SEG11	SEG11	31BH	SEG28	SEG28	SEG28	SEG28
30BH	SEG12	SEG12	SEG12	SEG12	31CH	SEG29	SEG29	SEG29	SEG29
30CH	SEG13	SEG13	SEG13	SEG13	31DH	SEG30	SEG30	SEG30	SEG30
30DH	SEG14	SEG14	SEG14	SEG14	31EH	SEG31	SEG31	SEG31	SEG31
30EH	SEG15	SEG15	SEG15	SEG15	31FH	SEG32	SEG32	SEG32	SEG32
30FH	SEG16	SEG16	SEG16	SEG16	320H	SEG33	SEG33	SEG33	SEG33
310H	SEG17	SEG17	SEG17	SEG17	321H	SEG34	SEG34	SEG34	SEG34

Segments 1 - 34, 1/3duty

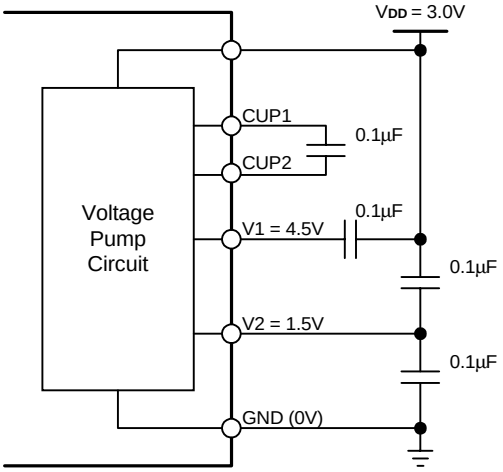
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	-	COM3	COM2	COM1		-	COM3	COM2	COM1
300H	-	SEG1	SEG1	SEG1	311H	-	SEG18	SEG18	SEG18
301H	-	SEG2	SEG2	SEG2	312H	-	SEG19	SEG19	SEG19
302H	-	SEG3	SEG3	SEG3	313H	-	SEG20	SEG20	SEG20
303H	-	SEG4	SEG4	SEG4	314H	-	SEG21	SEG21	SEG21
304H	-	SEG5	SEG5	SEG5	315H	-	SEG22	SEG22	SEG22
305H	-	SEG6	SEG6	SEG6	316H	-	SEG23	SEG23	SEG23
306H	-	SEG7	SEG7	SEG7	317H	-	SEG24	SEG24	SEG24
307H	-	SEG8	SEG8	SEG8	318H	-	SEG25	SEG25	SEG25
308H	-	SEG9	SEG9	SEG9	319H	-	SEG26	SEG26	SEG26
309H	-	SEG10	SEG10	SEG10	31AH	-	SEG27	SEG27	SEG27
30AH	-	SEG11	SEG11	SEG11	31BH	-	SEG28	SEG28	SEG28
30BH	-	SEG12	SEG12	SEG12	31CH	-	SEG29	SEG29	SEG29
30CH	-	SEG13	SEG13	SEG13	31DH	-	SEG30	SEG30	SEG30
30DH	-	SEG14	SEG14	SEG14	31EH	-	SEG31	SEG31	SEG31
30EH	-	SEG15	SEG15	SEG15	31FH	-	SEG32	SEG32	SEG32
30FH	-	SEG16	SEG16	SEG16	320H	-	SEG33	SEG33	SEG33
310H	-	SEG17	SEG17	SEG17	321H	-	SEG34	SEG34	SEG34

Segments 1 - 34, 1/2duty

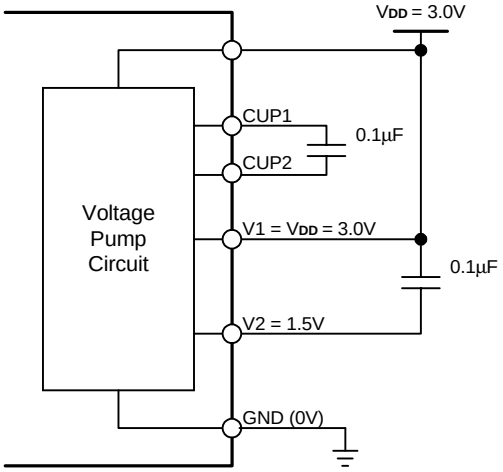
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	-	-	COM2	COM1		-	-	COM2	COM1
300H	-	-	SEG1	SEG1	311H	-	-	SEG18	SEG18
301H	-	-	SEG2	SEG2	312H	-	-	SEG19	SEG19
302H	-	-	SEG3	SEG3	313H	-	-	SEG20	SEG20
303H	-	-	SEG4	SEG4	314H	-	-	SEG21	SEG21
304H	-	-	SEG5	SEG5	315H	-	-	SEG22	SEG22
305H	-	-	SEG6	SEG6	316H	-	-	SEG23	SEG23
306H	-	-	SEG7	SEG7	317H	-	-	SEG24	SEG24
307H	-	-	SEG8	SEG8	318H	-	-	SEG25	SEG25
308H	-	-	SEG9	SEG9	319H	-	-	SEG26	SEG26
309H	-	-	SEG10	SEG10	31AH	-	-	SEG27	SEG27
30AH	-	-	SEG11	SEG11	31BH	-	-	SEG28	SEG28
30BH	-	-	SEG12	SEG12	31CH	-	-	SEG29	SEG29
30CH	-	-	SEG13	SEG13	31DH	-	-	SEG30	SEG30
30DH	-	-	SEG14	SEG14	31EH	-	-	SEG31	SEG31
30EH	-	-	SEG15	SEG15	31FH	-	-	SEG32	SEG32
30FH	-	-	SEG16	SEG16	320H	-	-	SEG33	SEG33
310H	-	-	SEG17	SEG17	321H	-	-	SEG34	SEG34

(c) Connection Diagram

V_{DD} = 3.0V, 4.5VLCD, 1/3Bias



V_{DD} = 3.0V, 3.0VLCD, 1/2Bias

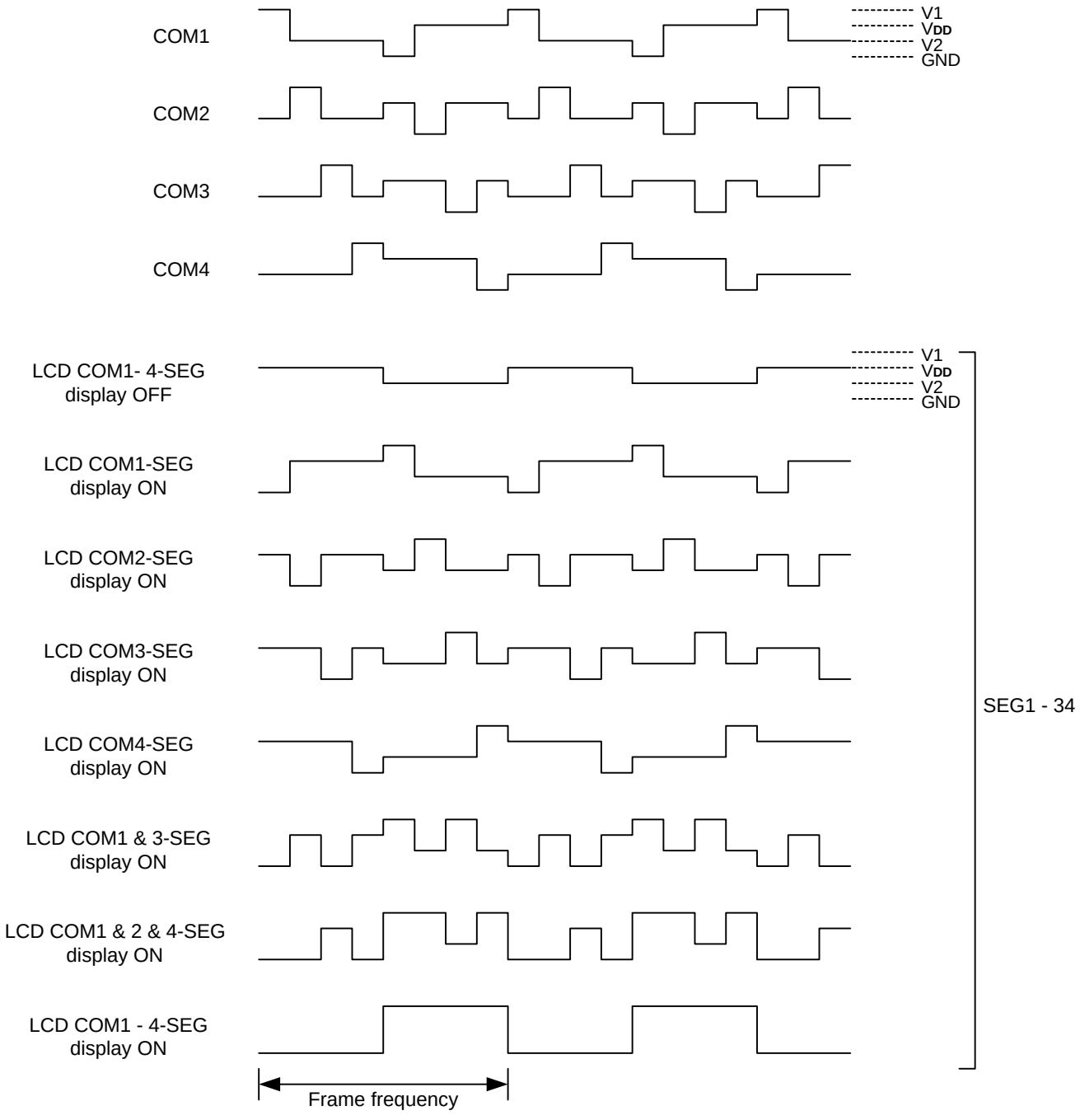


Notice:

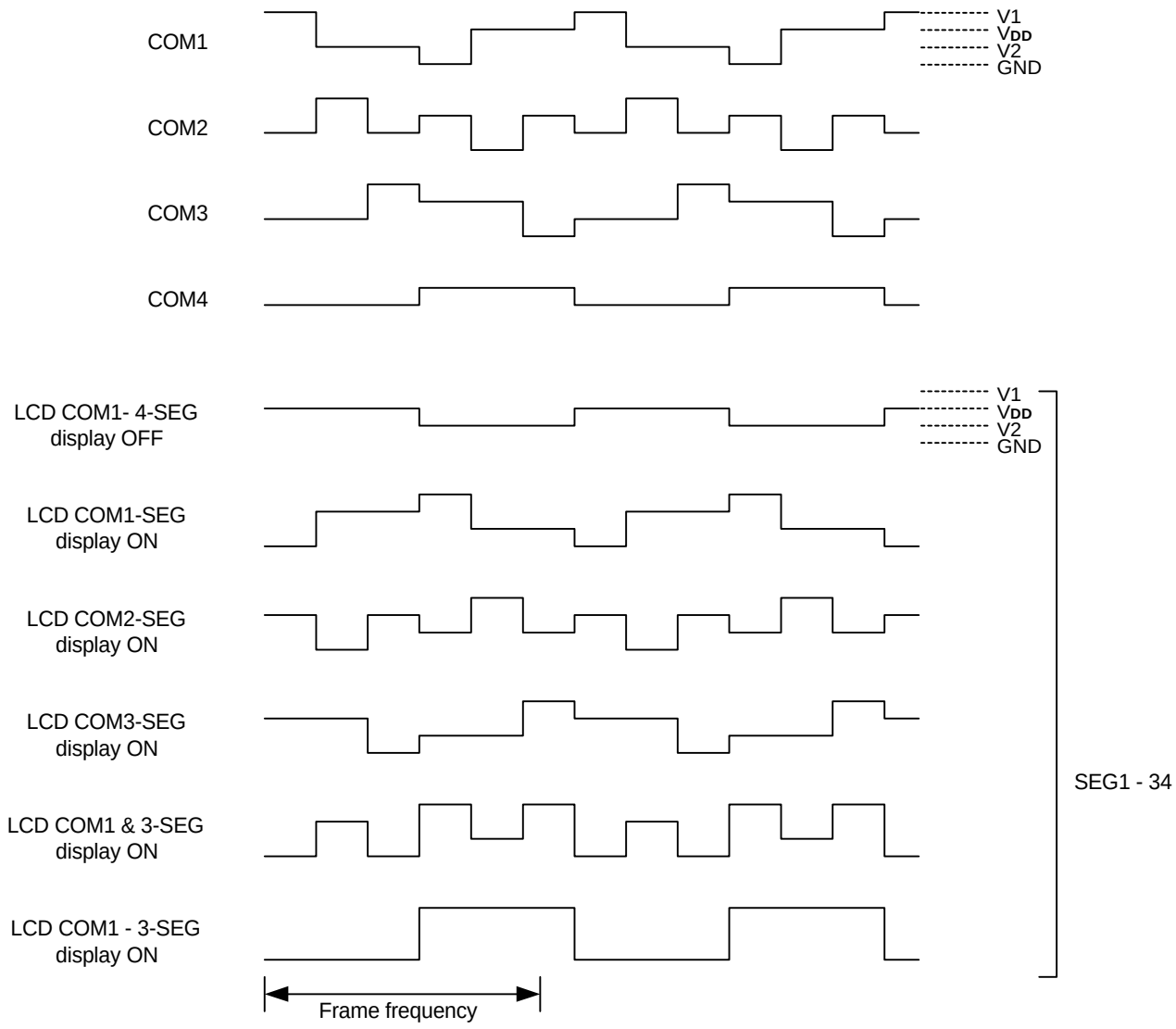
The pump circuit frequency could be 8KHz, 4KHz, 2KHz and 1KHz (selected by mask option). When use small LCD panel, user can select 1KHz pump frequency to save power. And when use large LCD panel, user can select 8KHz pump frequency to have more power supply ability for LCD use. Default the pump circuit frequency is 4KHz.

(d) LCD Waveform

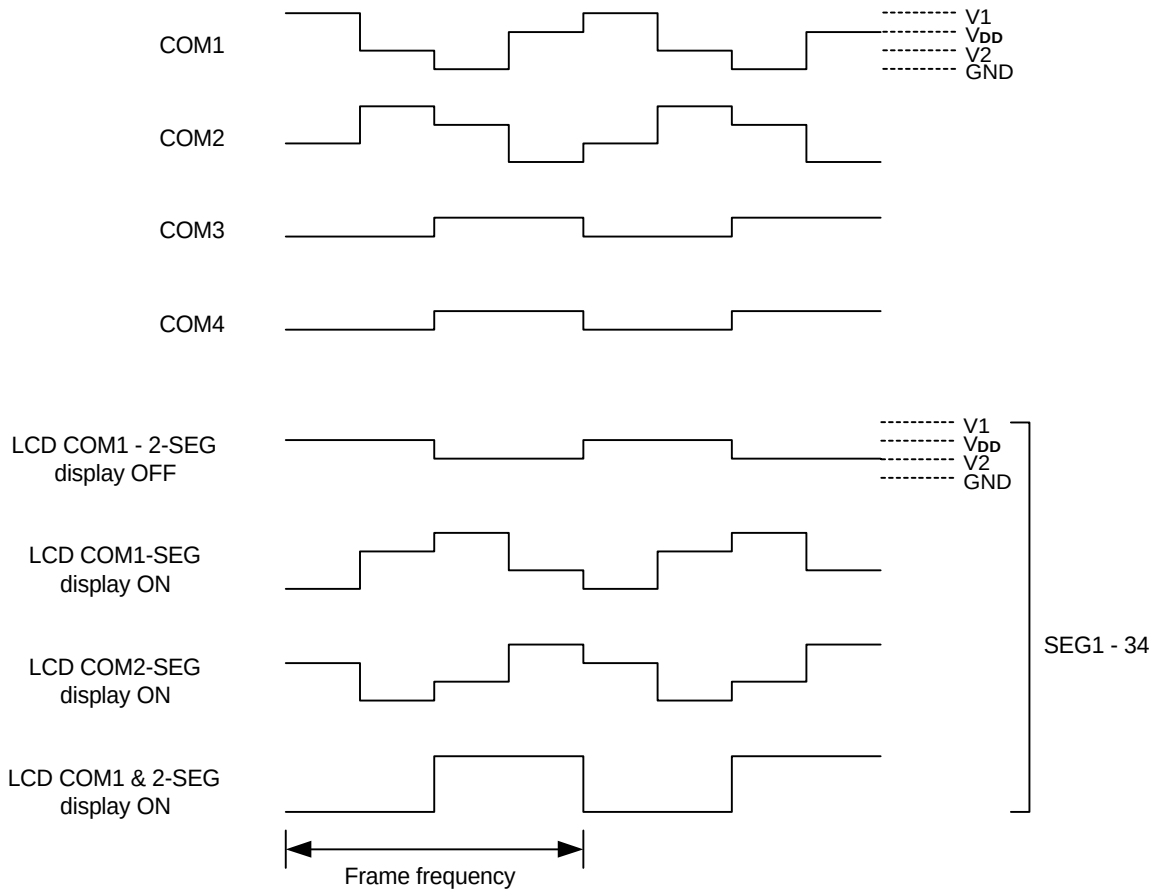
1/4 duty, 1/3 bias (V_{DD} = 3.0V, V1 = 4.5V, V2 = 1.5V, GND = 0V)



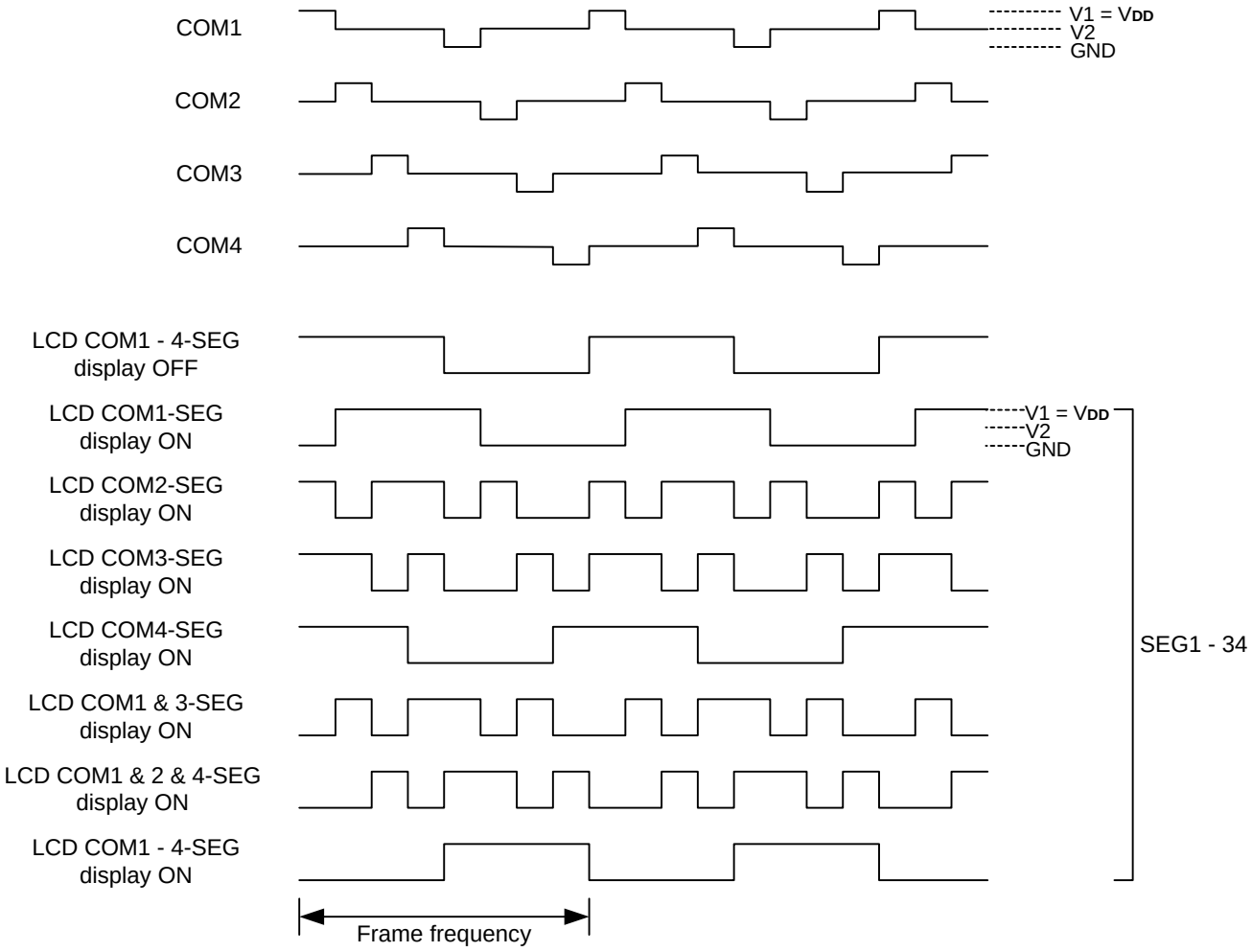
1/3 duty, 1/3 bias (V_{DD} = 3.0V, V1 = 4.5V, V2 = 1.5V, GND = 0V)



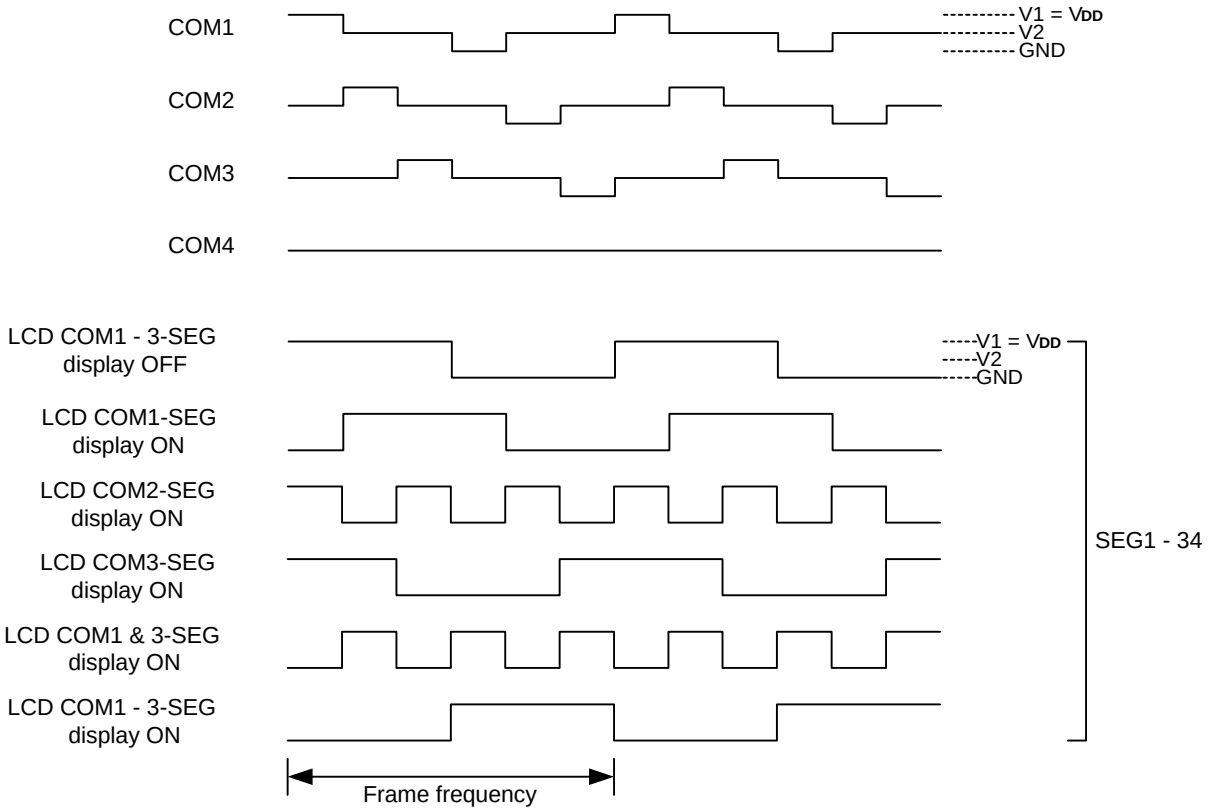
1/2 duty, 1/3 bias (V_{DD} = 3.0V, V1 = 4.5V, V2 = 1.5V, GND = 0V)



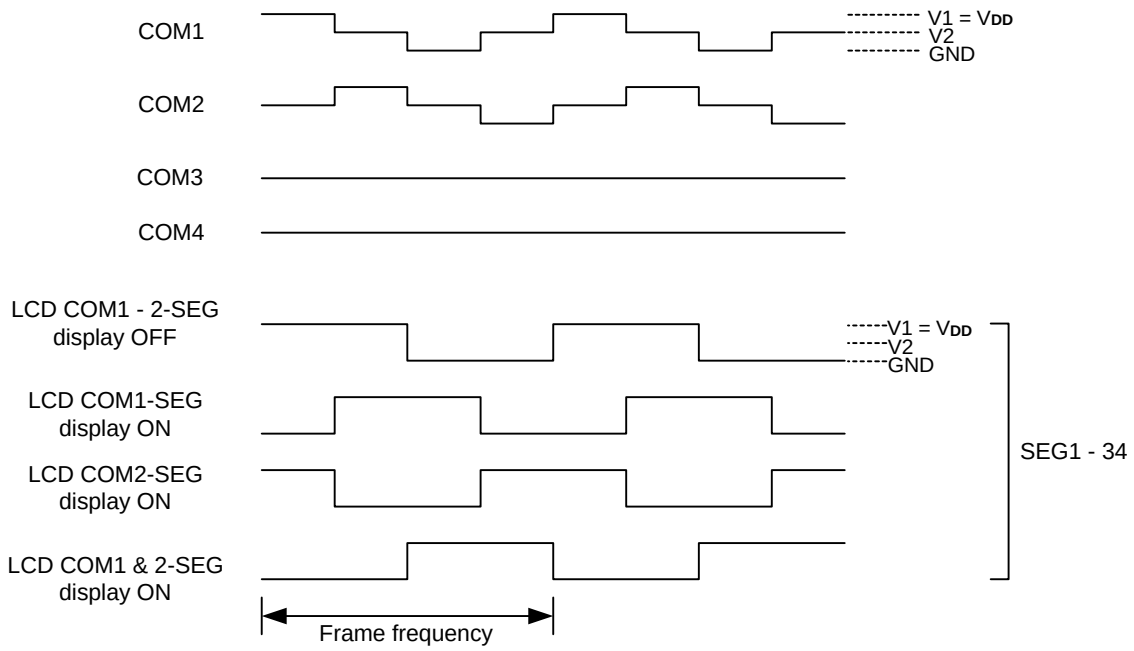
1/4 duty, 1/2 bias (V_{DD} = 3.0V, V1 = V_{DD} = 3.0V, V2 = 1.5V, GND = 0V)



1/3 duty, 1/2 bias (V_{DD} = 3.0V, V1 = V_{DD} = 3.0V, V2 = N1.5V, GND = 0V)



1/2 duty, 1/2 bias (V_{DD} = 3.0V, V1 = V_{DD} = 3.0V, V2 = 1.5V, GND = 0V)



10. Interrupt

Four interrupt sources are available on SH6603:

External interrupt (share with PA.0)

Timer0 interrupt

Timer1 interrupt

Port's rising edge detection interrupt (PBC)

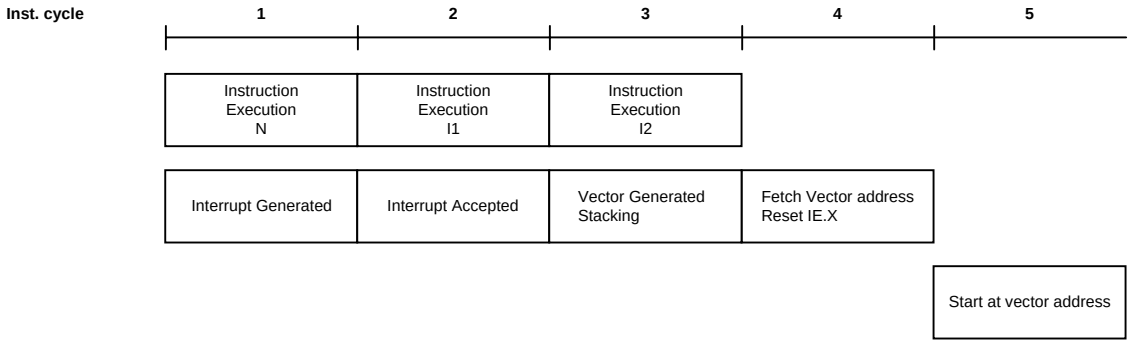
(a) Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags	0000

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

(b) Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

(c) External Interrupt (INT)

External interrupt is shared with the bit0 of PORTA. When bit3 of system register 0 (IEX) is set to 1, the external interrupt will be enabled, and a rising edge signal on PA.0 will generate an external interrupt. (Note: while external interrupt is enabled, writing a "1" to bit0 of PORTA will generate an external interrupt.) When PortA.0 is shared with PSG output, The external INT was disabled even the IEX is set to 1.

(d) Timer (Timer0,Timer1) Interrupt

The input clock of Timer0 and Timer1 are based on OSC clock. The timer overflow will generate an internal interrupt request, when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will start. This can also be used to wake the CPU from HALT mode.

(e) Port Interrupt

The PORTB and PORTC are used as port interrupt sources. Since PORT I/O is bit programmable I/O, so only the input port can generate an external interrupt. Any one of the PORTB and PORTC input pin transitions from GND to V_{DD} would generate an interrupt request. Further rising edge transition would not be able to make an interrupt request until all of the input pins have returned to GND. This can also be used to wake the CPU from STOP mode.

11. EL-LIGHT

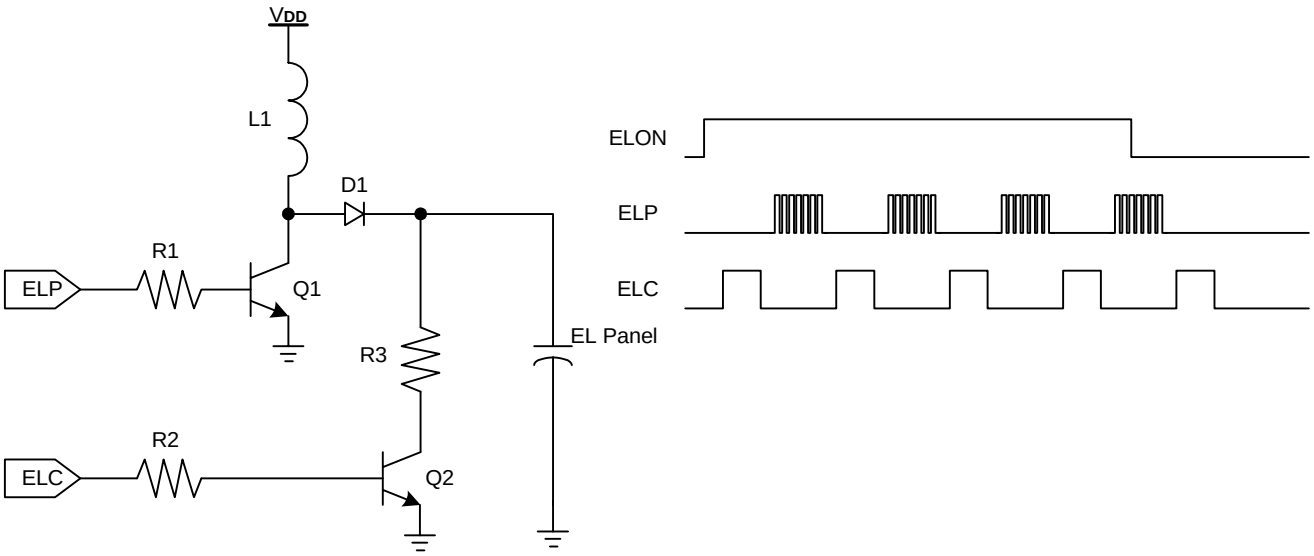
System Register $0D (Bit3 ~1):

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$0D	ELON	ELF	ELPF	OSCS	R/W	ELON: EL-LIGHT on/off control ELPF: EL-LIGHT driver charge frequency select ELF: EL-LIGHT driver discharge frequency select OSCS: OSC type selection	0000
	X	X	0	X		ELP pad output frequency = ELCLK	Yes
	X	X	1	X		ELP pad output frequency = ELCLK / 2	
	X	0	X	X		ELC pad output frequency = ELCLK / 64	Yes
	X	1	X	X		ELC pad output frequency = ELCLK / 32	
	0	X	X	X		EL-LIGHT driver turn off	Yes
	1	X	X	X		EL-LIGHT driver turn on	

ELCLK = 32KHz @32KHz crystal or 131KHz/4 @131KHz RC oscillator.

When EL-LIGHT off, the ELP and ELC output low.

Setup system register 0DH to select the EL-LIGHT driver waveform. Set ELON = 1 will turn on EL-LIGHT driver. ELC and ELP will output driver waveform automatic as diagram blew. With externally transistor, diode, inductance and resistor, we can pump the EL panel to AC 100 - 250V.



While EL-LIGHT turned on, the ELC will turn on before ELP turned on. When EL-LIGHT turn off, the ELP will turn off first, then ELC will still work for one cycle to make sure no voltage left on EL panel.

EL-LIGHT would keep on working in HALT mode. But it would turn off after executed "STOP" instruction (ELC & ELP keep low).

Notice:

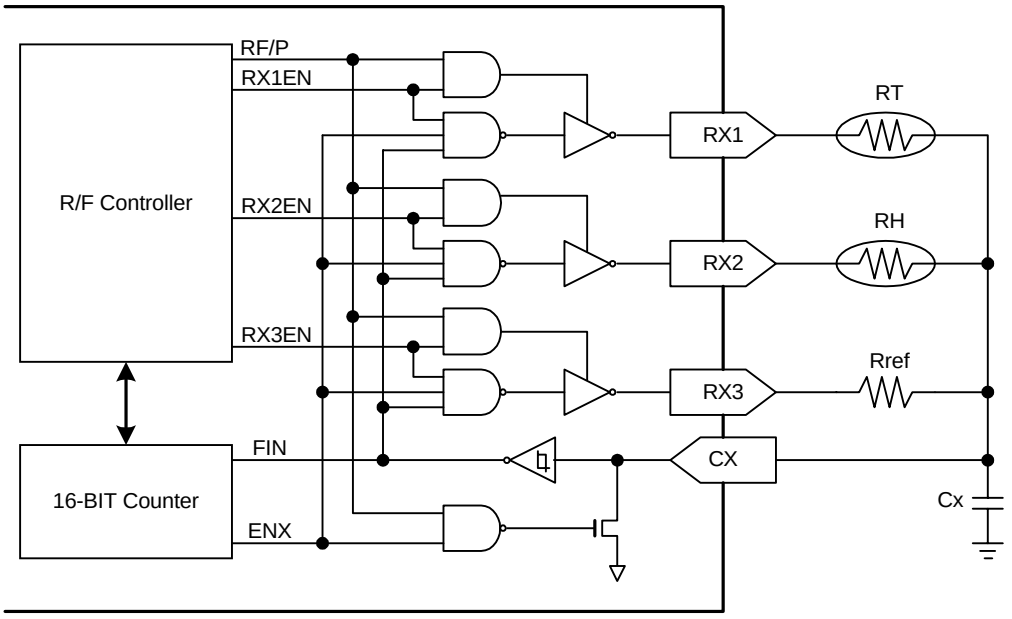
1. Please turn off EL-LIGHT before execute “STOP” instruction.

12. Resistor to Frequency Converter

System Register $0B, $0C, $1B - $1E:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	System Reset
$0B	RF/P	EL/P	S/P	PAM	R/W	PAM: Set PORTA1 - 0 as PSG output S/P: Set PORTC as segment output EL/P: Set PORTA3 - 2 as EL light output RF/P: Set PORTB as R-F converter	0000
$0C	ENX	RX3EN	RX2EN	RX1EN	R/W	RX1, 2, 3EN: Enables the RC oscillation of RX1, 2, 3 ENX: RFC counter on	0000
$1B	RFL.3	RFL.2	RFL.1	RFL.0	R/W	RFC 16-bit counter register low nibble	0000
$1C	RFML.3	RFM.2	RFML.1	RFML.0	R/W	RFC 16-bit counter register middle_low nibble	0000
$1D	RFMH.3	RFMH.2	RFMH.1	RFMH.0	R/W	RFC 16-bit counter register middle_high nibble	0000
$1E	RFH.3	RFH.2	RFH.1	RFH.0	R/W	RFC 16-bit counter register high nibble	0000

When set RF/P = 1, PortB are used as R-F converter. A RC oscillation circuit and a 16-bit counter are used to calculate the relative resistance of temperature and humidity sensor. The diagram is shown below:



The methodologies for measuring the input count value:

- Set RXnEN = 1 (Enables the RC oscillation of RXn). n = 1 or 2, 3.
- Using timer1 or timer0 as interval control and set ENX = 1 (start R-F counter).
- When timer1 or timer0 interrupt happened, The 16-bit counter value is the RXn-F count value.

So, repeat set can capture different count value of RT, RH and Rref.

Notice:

1. When RF/P = 1, PORTB interrupt was disabled.
2. The 16-bit counter can use as an event counter when not using RFC.
3. Max-frequency of RFC should less then 2MHz.
4. RFC could keep on working in HALT mode, and would stop automatic when execute "STOP" instruction. (Keep the last state of RX1-3 ports and stop the R-F counter)
5. Temperature sensor resistor: 10K - 50K @25^{0}C (for reference only)
6. Humidity sensor: 60K @25^{0}C, 50%RH (for reference only)

13. Watch Dog Timer

Watch dog timer is a down-count counter, and its clock source is 32768Hz or 131/4KHz. The watchdog timer automatically generates a device reset when it overflows. Software can enable and disable this function. The watchdog timer control registers (WDT bit0 - 2) is selects different overflow frequency. WDT bit3 is watchdog timer overflow flag.

System Register $1F (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power ON
$1F	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit0 - 2: Watch dog timer control WD: Watch dog timer overflow flag.(Read only)	0000
	X	0	0	0		Watchdog timer disable	Yes
	X	0	0	1		Watchdog timer overflow frequency = 0.125Hz	
	X	0	1	0		Watchdog timer overflow frequency = 0.25Hz	
	X	0	1	1		Watchdog timer overflow frequency = 0.5Hz	
	X	1	0	0		Watchdog timer overflow frequency = 1Hz	
	X	1	0	1		Watchdog timer overflow frequency = 2Hz	
	X	1	1	0		Watchdog timer overflow frequency = 4Hz	
	X	1	1	1		Watchdog timer overflow frequency = 8Hz	
	0	X	X	X		No watchdog timer overflow reset	Yes
	1	X	X	X		Watchdog timer overflow	

CPU will be reset when watchdog timer overflows. In normal operation, read or write WDT ($1F), the watchdog timer should re-count before overflow happens.

14. HALT and STOP Mode

After the execution of HALT instruction, SH6603 will enter halt mode. In halt mode, CPU will stop operating. But peripheral circuit (Timer0, Timer1, LCD display, RFC, EL-light, and watchdog timer) will keep operating.

After the execution of STOP instruction, SH6603 will enter stop mode. In stop mode, the whole chip (including oscillator, watchdog timer) will stop operating.

In HALT mode, SH6603 can be waked up if any interrupt occurs.

In STOP mode, SH6603 can be waked up if external Interrupt & port interrupt occurs.

15. Warm-up Timer

The SH6603 builds in oscillator warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

(1) Hardware reset

(2) Power on reset

(3) Wake-up from stop mode

Warm-up time interval:

(1) In RC mode, the warm-up counter prescaler is divided by 2^7 (128), the warm-up time interval is 0.98 ms.

(2) In Crystal mode, the warm-up counter prescaler is divided by 2^{12} (4096), the warm-up time interval is 125 ms.

Initial State

There are 3 types of system reset.
1. Hardware reset input
2. Power on reset
3. Watchdog timer overflow reset (When watchdog timer enable)

Hardware	After System Reset
Program Counter	$000
CY	Undefined
Data Memory	Undefined
AC	Undefined
Timer Counter	Undefined
Timer Mode Register	$0
Interrupt Enable Flags	$0
Interrupt Request Flags	$0
DPH, DPM, DPL	Undefined
TBR	Undefined
INX	Undefined
I/O Port (Port A, B, C)	Input
PPULL	0 (Disable PORT pull-down MOS)
PSG driver	OFF
LCD driver	LCD on, 1/4 duty, 1/3 bias (4 X 30)
EL-LIGHT driver	OFF
RFC driver	OFF
WDT	0000B (Hardware reset or Power on reset) 1000B (Watchdog timer overflow reset)

Instructions

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.
Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC [3]; AC [0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank = 000, 001
p	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input Voltage. . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . .0°C to +70°C

Storage Temperature . . . . . .-55°C to +125°C

*Comments

Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.2	3.0	3.6	V	
Operating Current	I_{OP}	-	5	8	μA	Execute NOP instruction, all output pads unload Include LCD current (1/4duty, 1/3bias) Exclude EL, RFC & PSG current,
Standby Current	I_{SB1}	-	2.5	4.0	μA	In HALT mode, all output pads unload Include LCD current (1/4duty, 1/3bias) Exclude EL, RFC & PSG current
Standby Current	I_{SB2}	-	-	0.5	μA	STOP mode, LCD off, all output pads unload
Input High Voltage	V_{IH1}	0.7 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC
Input High Voltage	V_{IH2}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	TEST, Ex.INT, $\overline{RESET}$
Input Low Voltage	V_{IL1}	GND - 0.3	-	0.3 X V_{DD}	V	PORTA, PORTB, PORTC
Input Low Voltage	V_{IL2}	GND - 0.3	-	0.2 X V_{DD}	V	TEST, Ex.INT, $\overline{RESET}$
Output High Voltage	V_{OH1}	0.8 X V_{DD}	-	-	V	PORTA, PORTC (I_{OH} = -1.0mA)
Output Low Voltage	V_{OL1}	-	-	0.2 X V_{DD}	V	PORTA, PORTC (I_{OL} = 2.0mA)
Output High Voltage	V_{OH2}	0.8 X V_{DD}	-	-	V	BD/$\overline{BD}$ (set PA.0, PA.1 to PSG output), ELC,ELP (set PA.2, PA.3 to EL driver), (I_{OH} = -0.3mA)
Output Low Voltage	V_{OL2}	-	-	0.2 X V_{DD}	V	BD/$\overline{BD}$ (set PA.0, PA.1 to PSG output), ELC,ELP (set PA.2, PA.3 to EL driver), (I_{OL} = 0.3mA)
Output High Voltage	V_{OH3}	0.8 X V_{DD}	-	-	V	PORTB (I_{OH} = -3.0mA)
Output Low Voltage	V_{OL3}	-	-	0.2 X V_{DD}	V	PORTB (I_{OL}= 3.0mA)
Output High Voltage	V_{OH4}	V_1 - 0.2	-	-	V	SEGx (I_{OH} = -3.0μA, 1/3bias)
Output Low Voltage	V_{OL4}	-	-	0.2	V	SEGx (I_{OL} = 3.0μA, 1/3bias)
Output High Voltage	V_{OH5}	V_1 - 0.2	-	-	V	COMx (I_{OH} = -8.0μA, 1/3bias)
Output Low Voltage	V_{OL5}	-	-	0.2	V	COMx (I_{OL} = -8.0μA, 1/3bias)
Pull-low Resistor	R_{PL}	-	150	-	KΩ	Pull-down resistor (V_I = V_{DD})

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 131KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.2	3.0	3.6	V	
Operating Current	I_{OP}		20	30	μA	Execute NOP instruction, all output pads unload Include LCD current (1/4duty, 1/3bias) Exclude EL, RFC & PSG current
Standby Current	I_{SB1}		10	15	μA	In HALT mode, all output pads unload Include LCD current (1/4duty, 1/3bias) Exclude EL, RFC & PSG current
Standby Current	I_{SB2}			0.5	μA	STOP mode, LCD off, all output pads unload

AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	T_{STT}	-	1	2	s	F_{OSC} = 32.768KHz Crystal
Frequency stability	ΔF/F	-	-	5	%	F_{OSC} = 131KHz RC, |F(2.4V) - F(3.0V)|/F(3.0V)
Frequency Variation	ΔF/F	-	-	15	%	F_{OSC} = 131KHz RC, Chip to chip variation

Mask Option

1. Clock Source Select

0 = 32768Hz Crystal (default)
1 = 131KHz RC

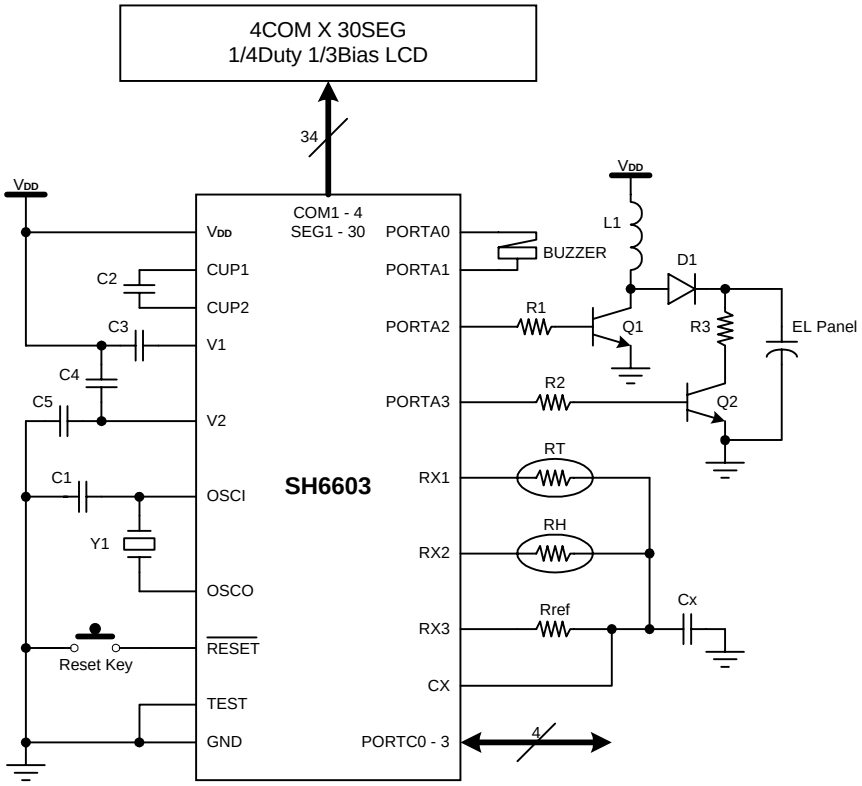
2. LCD Pump Circuit Frequency Select

0, 0 = 1KHz
0, 1 = 2KHz
1, 0 = 4KHz (default)
1, 1 = 8KHz

Application Circuit (for reference only)

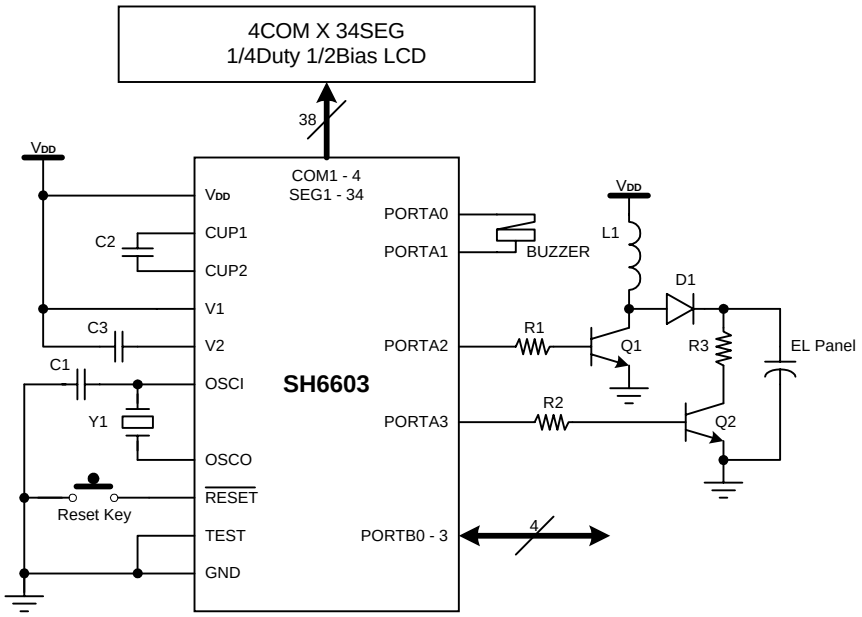
AP1:

(1) Oscillator: 32.768KHz Crystal (mask option and set system register $0D'bit0=1).
(2) PORTA0, 1: PSG output.
(3) PORTA2, 3: EL-Light output.
(4) PORTB0 - 3: RFC (Resistor to Frequency Converter).
(5) PORTC0 - 3: I/O (Input: Key in / Output: Direct drive analog movement).
(6) LCD driver: 1/4 Duty, 1/3 Bias, and 4.5V LCD.
(7) RT: Temperature Sensor.
(8) RH: Humidity Sensor.
(9) Rref: Reference Resister.
(10) Cx: R-F converter capacitor.
(11) V_{DD} = 3.0V, GND = 0V, Y1 = 32.768KHz Crystal.
(12) C1 = 12pF, C2 = C3 = C4 = C5 = 0.1μF, R1 = R2 = 100Ω, R3 = 10KΩ, D1 = IN4148, L1 = 3.2mH/15Ω.



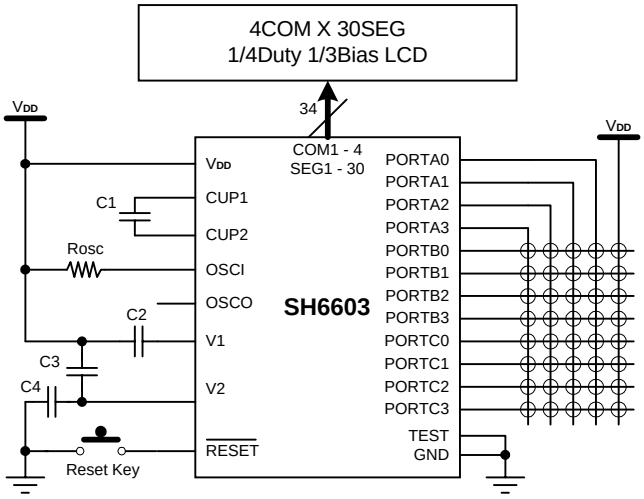
AP2:

(1) Oscillator: 32.768KHz Crystal (mask option and set system register $0D'bit0=1).
(2) PORTA0, 1: PSG output.
(3) PORTA2, 3: EL-Light output.
(4) PORTB0 - 3: I/O (Input: Key in / Output: Direct drive analog movement).
(5) PORTC0 - 3: Shared with SEG31 - 34.
(6) LCD driver: 1/4 Duty, 1/2 Bias, and 3V LCD.
(7) V_{DD} = 3.0V, GND = 0V, Y1 = 32.768KHz Crystal.
(8) C1 = 12pF, C2 = C3 = 0.1μF, R1 = R2 = 100Ω, R3 = 10KΩ, D1 = IN4148, L1 = 3.2mH/15Ω.



AP3:

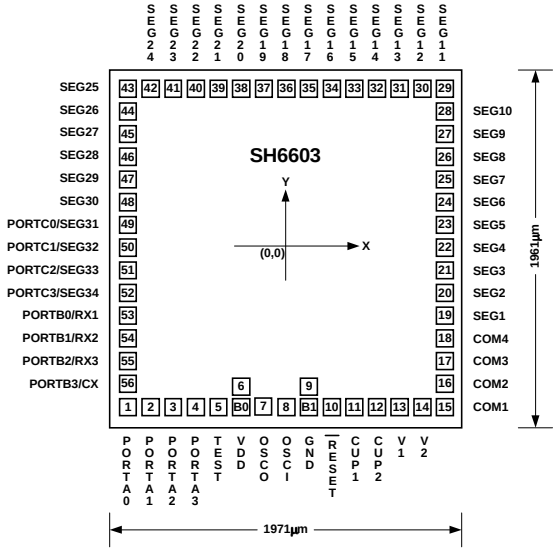
(1) Oscillator: 131KHz RC (mask option and set system register $0D'bit0=0).
(2) PORTA, B, C 0 - 3: I/O.(40Keys)
(3) LCD driver: 1/4 Duty, 1/3 Bias, and 4.5V LCD.
(4) V_{DD} = 3.0V, GND = 0V.
(5) R_{OSC} =1.8MΩ, C1 = C2 = C3 = C4 = 0.1μF.



Ordering Information

Part No.	Package
SH6603H	CHIP FORM

Bonding Diagram



* Substratum connects to GND.

Unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTA0	-852.00	-847.00	28	SEG10	852.00	715.00
2	PORTA1	-720.00	-847.00	29	SEG11	852.00	847.00
3	PORTA2	-590.00	-847.00	30	SEG12	720.00	847.00
4	PORTA3	-470.00	-847.00	31	SEG13	590.00	847.00
5	TEST	-350.00	-847.00	32	SEG14	470.00	847.00
6	V_{DD}	-233.00	-755.00	33	SEG15	350.00	847.00
	B0	-233.00	-847.00	34	SEG16	230.00	847.00
7	OSCO	-115.00	-847.00	35	SEG17	115.00	847.00
8	OSCI	0.00	-847.00	36	SEG18	0.00	847.00
9	GND	118.00	-755.00	37	SEG19	-115.00	847.00
	B1	118.00	-847.00	38	SEG20	-230.00	847.00
10	$\overline{\text{RESET}}$	235.00	-847.00	39	SEG21	-350.00	847.00
11	CUP1	350.00	-847.00	40	SEG22	-470.00	847.00
12	CUP2	470.00	-845.00	41	SEG23	-590.00	847.00
13	V1	590.00	-847.00	42	SEG24	-720.00	847.00
14	V2	720.00	-847.00	43	SEG25	-852.00	845.00
15	COM1	852.00	-847.00	44	SEG26	-852.00	715.00
16	COM2	852.00	-715.00	45	SEG27	-852.00	585.00
17	COM3	852.00	-585.00	46	SEG28	-852.00	465.00
18	COM4	852.00	-465.00	47	SEG29	-852.00	345.00
19	SEG1	852.00	-345.00	48	SEG30	-852.00	230.00
20	SEG2	852.00	-230.00	49	PORTC0	-852.00	115.00
21	SEG3	852.00	-115.00	50	PORTC1	-852.00	0.00
22	SEG4	852.00	0.00	51	PORTC2	-852.00	-115.00
23	SEG5	852.00	115.00	52	PORTC3	-852.00	-230.00
24	SEG6	852.00	230.00	53	PORTB0	-852.00	-345.00
25	SEG7	852.00	345.00	54	PORTB1	-852.00	-465.00
26	SEG8	852.00	465.00	55	PORTB2	-852.00	-585.00
27	SEG9	852.00	585.00	56	PORTB3	-852.00	-715.00

Appendix:

1. Music Scale Reference Table (for reference only)

(a) Table 1: Following is the music scale reference table for PSG under actual clock = 32KHz.

Note	Ideal freq.	N	LSFR (C1.6-C1.0)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6-C1.0)	Real freq.	Error %
C3	130.81	122	20	131.15	0.26%	**G4**	392.00	41	58	390.24	-0.44%
C3#	138.59	115	61	139.13	0.39%	**G4#**	415.31	39	63	410.26	-1.21%
D3	146.83	109	51	146.79	-0.03%	**A4**	440.00	36	1A	444.44	1.01%
D3#	155.56	103	19	155.34	-0.14%	**A4#**	466.17	34	69	470.59	0.95%
E3	164.81	97	45	164.95	0.08%	**B4**	493.85	32	25	500.00	1.24%
F3	174.61	92	33	173.91	-0.40%	**C5**	523.24	31	4B	516.13	-1.36%
F3#	185.00	86	6A	186.05	0.57%	**C5#**	554.37	29	2E	551.72	-0.48%
G3	195.99	82	27	195.12	-0.44%	**D5**	587.32	27	3B	592.59	0.90%
G3#	207.65	77	7A	207.79	0.07%	**D5#**	622.25	26	77	615.38	-1.10%
A3	220.00	73	21	219.18	-0.37%	**E5**	659.24	24	5C	666.67	1.13%
A3#	233.08	69	1C	231.88	-0.51%	**F5**	698.44	23	39	695.65	-0.40%
B3	246.94	65	44	246.15	-0.32%	**F5#**	739.99	22	73	727.27	-1.72%
C4	261.62	61	49	262.30	0.26%	**G5**	783.96	20	4C	800.00	2.04%
C4#	277.18	58	4D	275.86	-0.48%	**G5#**	830.60	19	19	842.11	1.38%
D4	293.66	54	5A	296.30	0.90%	**A5**	880.00	18	32	888.89	1.01%
D4#	311.13	51	56	313.73	0.84%	**A5#**	932.32	17	65	941.18	0.95%
E4	329.62	49	5B	326.53	-0.94%	**B5**	987.76	16	4A	1000.00	1.24%
F4	349.22	46	5E	347.83	-0.40%	**C6**	1046.48	15	15	1066.67	1.93%
F4#	369.99	43	76	372.09	0.57%	**C6#**	1108.72	14	2A	1142.86	3.08%

(b) Table2: Following is the music scale reference table for PSG under actual clock = 16KHz.

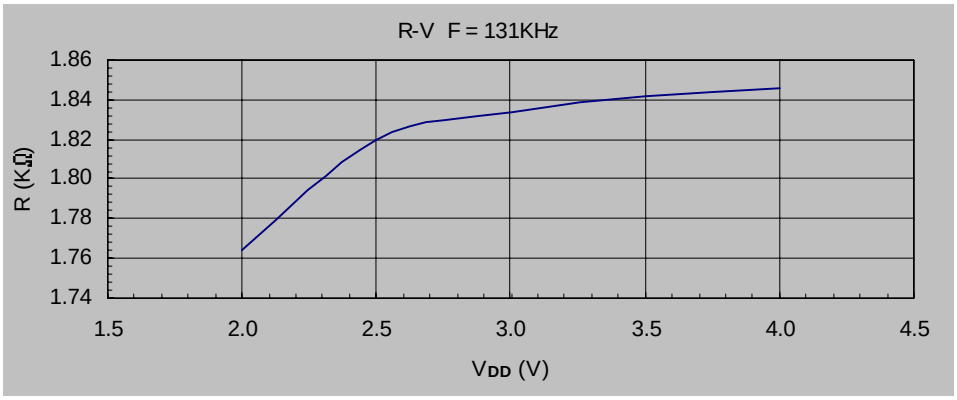
Note	Ideal freq.	N	LSFR (C1.6-C1.0)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6-C1.0)	Real freq.	Error %
C2	65.41	122	20	65.58	0.26%	**G3**	195.99	41	58	195.12	-0.44%
C2#	69.30	115	61	69.57	0.39%	**G3#**	207.65	39	63	205.13	-1.21%
D2	73.42	109	51	73.40	-0.03%	**A3**	220.00	36	1A	222.22	1.01%
D2#	77.78	103	19	77.67	-0.14%	**A3#**	233.08	34	69	235.30	0.95%
E2	82.41	97	45	82.48	0.08%	**B3**	246.94	32	25	250.00	1.24%
F2	87.31	92	33	86.96	-0.40%	**C4**	261.62	31	4B	258.07	-1.36%
F2#	92.50	86	6A	93.03	0.57%	**C4#**	277.18	29	2E	275.86	-0.48%
G2	98.00	82	27	97.56	-0.44%	**D4**	293.66	27	3B	296.30	0.90%
G2#	103.83	77	7A	103.90	0.07%	**D4#**	311.13	26	77	307.69	-1.10%
A2	110.00	73	21	109.59	-0.37%	**E4**	329.62	24	5C	333.34	1.13%
A2#	116.54	69	1C	115.94	-0.51%	**F4**	349.22	23	39	347.83	-0.40%
B2	123.47	65	44	123.08	-0.32%	**F4#**	369.99	22	73	363.64	-1.72%
C3	130.81	61	49	131.15	0.26%	**G4**	392.00	20	4C	400.00	2.04%
C3#	138.59	58	4D	137.93	-0.48%	**G4#**	415.31	19	19	421.06	1.38%
D3	146.83	54	5A	148.15	0.90%	**A4**	440.00	18	32	444.45	1.01%
D3#	155.56	51	56	156.87	0.84%	**A4#**	466.17	17	65	470.59	0.95%
E3	164.81	49	5B	163.27	-0.94%	**B4**	493.85	16	4A	500.00	1.24%
F3	174.61	46	5E	173.92	-0.40%	**C5**	523.24	15	15	533.34	1.93%
F3#	185.00	43	76	186.05	0.57%	**C5#**	554.37	14	2A	571.43	3.08%

(c) Table3: Following is the music scale reference table for PSG under actual clock = 131KHz.

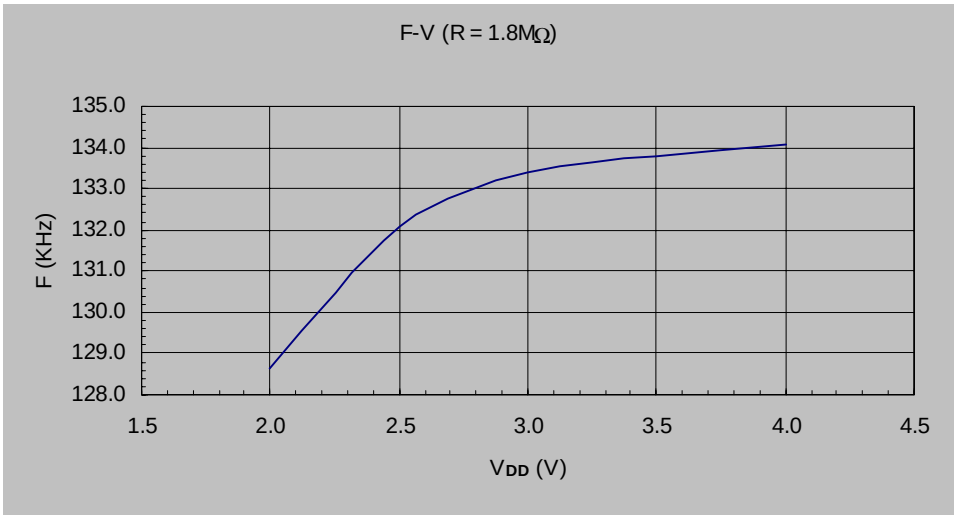
Note	Ideal freq.	N	LSFR (C1.6-C1.0)	Real freq.	Error %	Note	Ideal freq.	N	LSFR (C1.6-C1.0)	Real freq.	Error %
C5	523.24	125	04	524.00	0.15%	**G6**	1568.00	42	6C	1559.52	-0.54%
C5#	554.37	118	0C	555.08	0.13%	**G6#**	1661.24	39	63	1679.49	1.10%
D5	587.32	112	0A	584.82	-0.43%	**A6**	1760.00	37	0D	1770.27	0.58%
D5#	622.25	105	1E	623.81	0.25%	**A6#**	1864.68	35	34	1871.43	0.36%
E5	659.24	99	11	661.62	0.36%	**B6**	1975.40	33	52	1984.85	0.48%
F5	698.44	94	2C	696.81	-0.23%	**C7**	2092.96	31	4B	2112.90	0.95%
F5#	739.99	89	1D	735.96	-0.55%	**C7#**	2217.48	30	17	2183.33	-1.54%
G5	783.96	84	29	779.76	-0.54%	**D7**	2349.28	28	5D	2339.29	-0.43%
G5#	830.60	79	3E	829.11	-0.18%	**D7#**	2489.00	26	77	2519.23	1.21%
A5	880.00	74	50	885.14	0.58%	**E7**	2636.96	25	6E	2620.00	-0.64%
A5#	932.32	70	0E	935.71	0.36%	**F7**	2793.76	23	39	2847.83	1.94%
B5	987.76	66	62	992.42	0.47%	**F7#**	2959.96	22	73	2977.27	0.58%
C6	1046.48	63	12	1039.68	-0.65%	**G7**	3135.84	21	66	3119.05	-0.54%
C6#	1108.72	59	26	1110.17	0.13%	**G7#**	3322.40	20	4C	3275.00	-1.43%
D6	1174.64	56	36	1169.64	-0.43%	**A7**	3520.00	19	19	3447.37	-2.06%
D6#	1244.52	53	35	1235.85	-0.70%	**A7#**	3729.28	18	32	3638.89	-2.42%
E6	1318.48	50	2D	1310.00	-0.64%	**B7**	3951.04	17	65	3852.94	-2.48%
F6	1396.88	47	6F	1393.62	-0.23%	**C8**	4185.92	16	4A	4093.75	-2.20%
F6#	1479.96	44	7B	1488.64	0.59%	**C8#**	4434.88	15	15	4366.67	-1.54%

2. RC Oscillator Characteristics (for reference only)

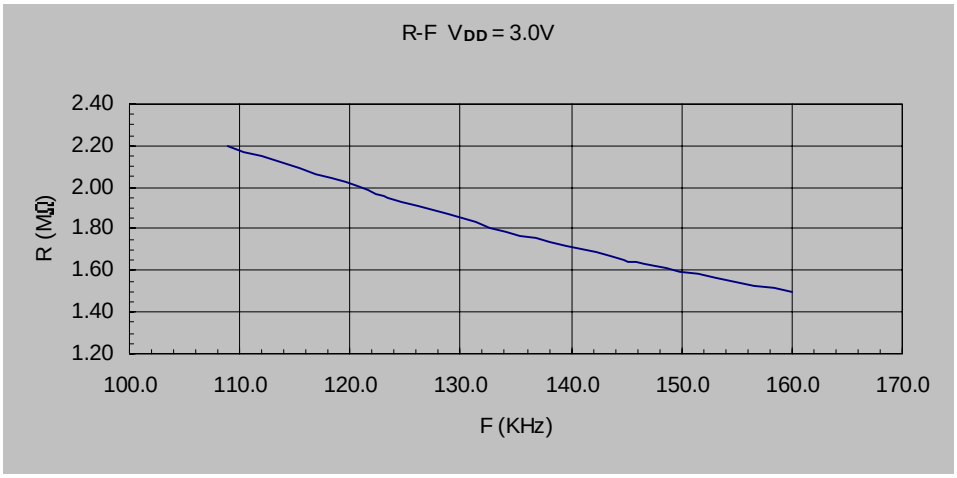
(a) Typical RC oscillator Resistor vs. V_{DD}:



(b) Typical RC oscillator Frequency vs. V_{DD}:



(c) Typical RC oscillator Resistor vs. Frequency:



Data Sheet Version History

Version	Content	Date
0.3	DC electrical characters change. Functional Description changes.	Jul. 2003
0.2	Preliminary SPEC. DC electrical characters change. Application circuit added. Bonding diagram added.	Jan. 2002
0.1	Original	May. 2001