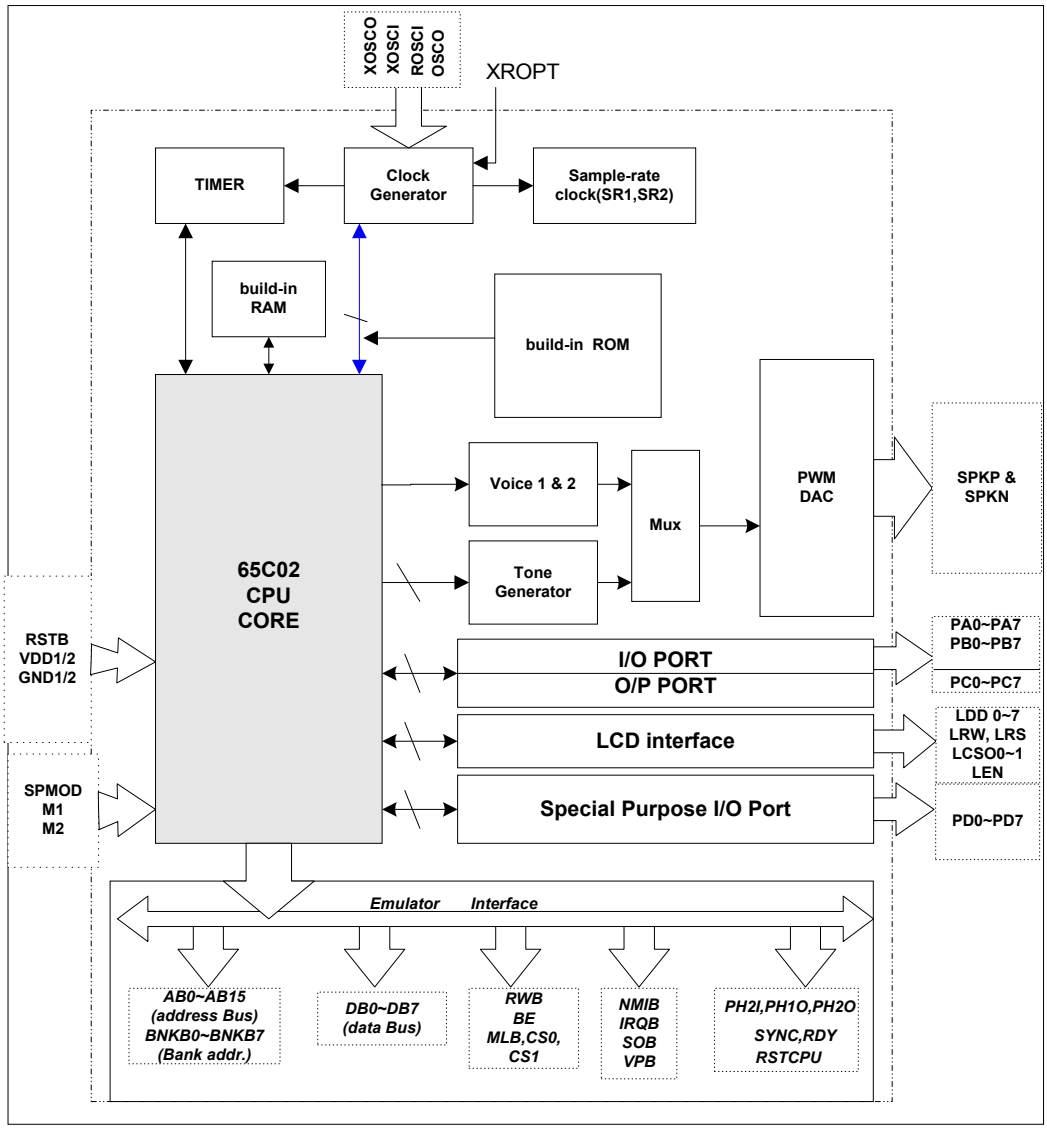
Features

- 65C02-based single chip 8 bit micro-controller
- Operation voltage:2.2V~3.5V
- Dual oscillation circuits:System oscillator
  RC or Crystal Mode selected by pad option
  (oscillator can be 3.58M ceramic or 4~16M Crystal or 4~16M RC under 3.0V Operating)
  32.768K Crystal for real time clock
- MCU(CPU) operate speed --software programmable
  Source Clock /2, /4, /8 mode
  32.678KHz (Crystal)
- RAM: Built-in 12K x 8 bits(incl. program Var. & stack)
  External RAM available (Max. up to 2M byte)
- ROM: Built-in 256K x 8 bits (incl. Program and Data)
  External ROM available (Max. up to 4M byte)
- Internal and external ROM Co-existed (Max. 4M byte)
- Voice Synthesizer of 2 channels & Tone
- Software selectable compression structure for various sound quality and duration requirements:
  4 bits ADPCM or 5 bit u-law or 8 bit PCM
- 2 Modes of PWM/DAC output
  Double-Pin Single Ended (only for PWM)
  Single-Pin Single Ended
- Can connect with 2 speakers output for STEREO effect
- UART with maximum baud rate 57.6Kbps is available
- Two I/O ports--PA & PB (16 I/O pads)
- One O/P port--PC (8 O/P pads)
- One Special Purpose I/O port – PD (this port can be switched as I/O or special function port)
  1 external interrupt
  1 build-in remote control carrier synthesizer – software programmable
  1 serial input for UART
  1 serial output for UART
  8 bit I/O configured as push-pull/open-collector output
- Standard LCD driver interface (13 ports including 2 chip select)
- Three 8-bit timers----Timer0, Timer1, Timer2.
- Two 16-bit sample rate counters (SR1,SR2)
  SR1and SR2 are used for Voice sample rate clock
- One programmable watchdog timer
- One programmable wake-up timer
- Two interrupt levels and various interrupt sources:
  NMI and IRQ (priority: NMI > IRQ)
  IRQ source
  Timer0, Timer1, Timer2, Wake-Up Timer, PA&PB (falling edge), External Interrupt, SR2 Sample rate clock
  NMI source
  PA, SR1 Sample rate clock, SRI & STI for serial interface
- Power saving mode and wake-up function
- Low power detector

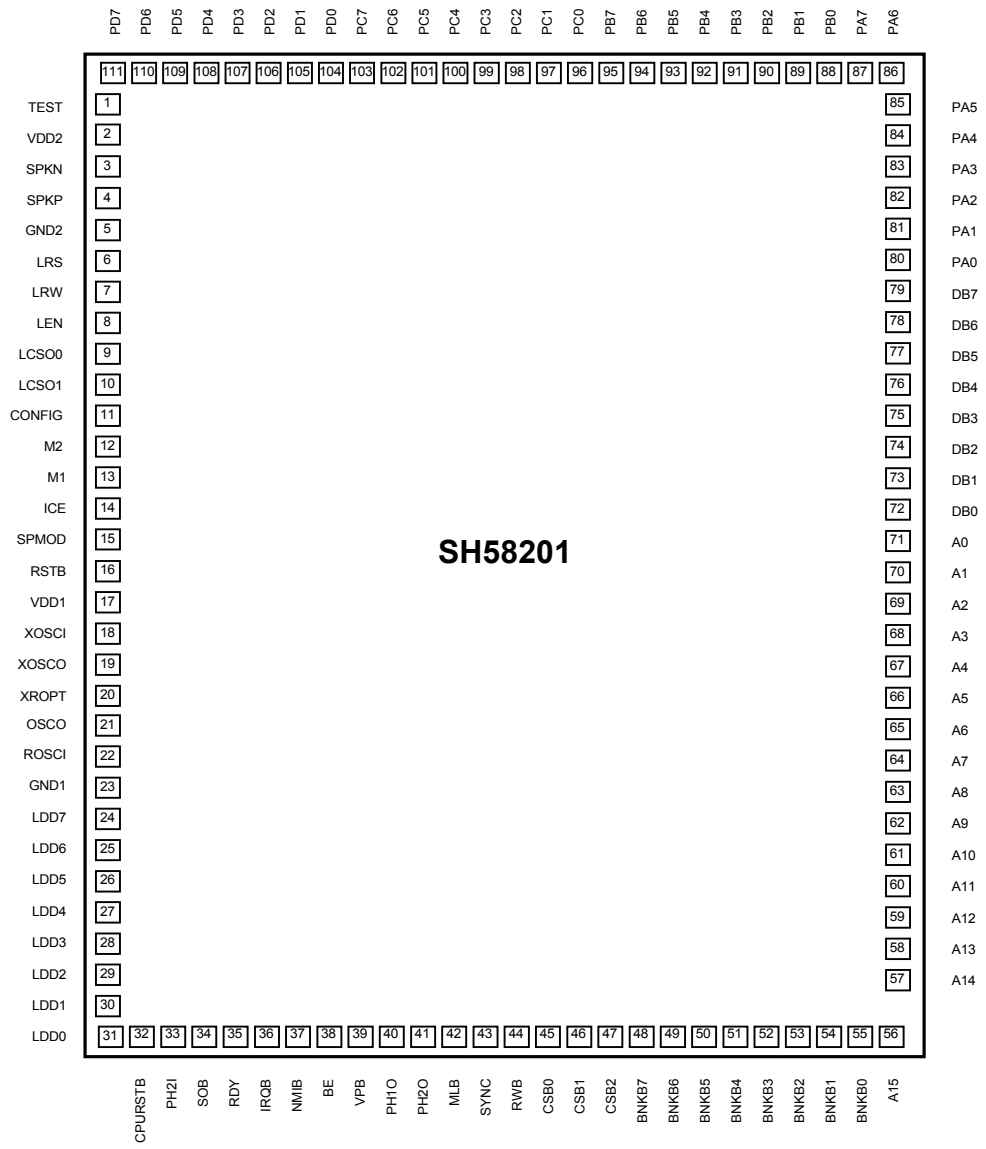
General Description

The SH58201 is a powerful 8-bit micro-controller with LCD drivers interfaces. It integrates a 65C02 8-bit core CPU, SRAM, ROM, and complicated logic blocks, such as timers, PWM/DAC. The dual-buffered PWM allows user to connect one speaker directly or 2 speakers with external components. The standby/wakeup function, which can be used to stop/wake-up the oscillator, facilitates the system entrance/quitting the low power dissipation. This chip offers 2 channels of voice or tone or mixed, the speech sources can be coded as PCM, u-Law or ADPCM format through NOVATEK's tools.
Voice duration depends on the compression structure. Lower compression rate gains high sound quality and shorter duration. Normally, ADPCM can meet most requirements especially the sound frequency varies not so violent.
SH58201 also offers total 16 I/O, 8 O/P pins and 8 speical purpose I/O, which can be used for keyboard scan or others high I/O pins needed application. The embeded UART also facilitates the device communicating with the PC via RS232 serial port. Using the LCD interface, it's suitable to be a LCD ELA product control engine. Furthermore, the electronic dictionary, the electrical data bank or personal digital assistance (PDA) equipment, talking instrument and general speech synthesizer are also applicable.

Block Diagram



Pad Configuration



Pin、Pad Descriptions

Pin No.	Pad No	Designation	I/O	Description
		XOSCI	I	32768 Hz crystal oscillator input pin
		XOSCO	O	32768 Hz crystal oscillator output pin
		ROSCI	I	System oscillator (RC or Crystal) input pin
		OSCO	O	System oscillator (Crystal) output pin (Pad option)
		XROPT	I	0=RC type; 1=X'tal /Resonator type
		RSTB	I	Reset pin
		VDD1	I	Positive power pin
		GND1	I	Ground pin
		VDD2	I	Positive power pin
		GND2	I	Ground pin
		PA0~PA7	I/O	Bi-directional I/O port (all bit programmable)
		PB0~PB7	I/O	Bi-directional I/O port (high /low nibble programmable)
		PC0~PC7	O	Output only port
		PD0 / EXT_INT PD1 / TXD PD2 / RXD PD3 / REMO PD4 ~ PD7	I/O	Special purpose I/O (can switch as normal I/O or special function pin) PD.0 can be switched as external interrupt; PD.3 can be switched as Remote control synthesizer carrier; PD2 & PD1 can be switched as UART receive input and transmit output, individually. PD4~7 can be selected as open drain output.
		SPKP,SPKN	O	Positive/Negative terminal of PWM output pins (directly connect with speaker or separate as 2 channels)
		LDD0~~LDD7	I/O	LCD interface(for data bus)
		LRS	O	LCD interface(for register select, choose Command/Data mode)
		LCSO0~LCSO1	O	LCD interface(for chip select in the multi-chip mode)
		LRW	O	LCD interface(read /write signal)
		LEN	O	LCD interface(read/write enable signal)
		CSB0	O	External ROM chip select enable (Low active)
		CSB1	O	External Flash ROM chip select enable (Low active)
		CSB2	O	External RAM chip select enable (Low active)
		SPMOD	I	Special mode switch
		CONFIG	O	CONFIG SETTING (Low active)
		M1, M2	I	Mode selection(ICE or Normal mode) → Default: M1 floating
		BNKB0~BNKB7	O	Address Bus for bank switch
		DB0~DB7	I/O	65C02 CPU signal(data bus)
		A0~A15	I/O	65C02 CPU signal(address Bus)
		BE	O	65C02 CPU signal (Bus enable signal)
		MLB	I/O	65C02 CPU signal (Memory lock)
		RWB	I/O	65C02 CPU signal (Read or write selection)
		PH2I	O	65C02 CPU signal (Phase 2 input clock)
		PH1O,PH2O	I/O	65C02 CPU signal (Phase1,2 output clock)
		SYNC	I/O	65C02 CPU signal (Synchronize input)
		RDY	O	65C02 CPU signal (Ready)
		NMIB, IRQB	O	65C02 CPU signal (Non-maskable IRQ, Interrupt request)
		SOB	O	65C02 CPU signal (Set overflow)
		VPB	I/O	65C02 CPU signal (Vector full)
		CPURSTB	I/O	65C02 CPU signal (CPU reset)
		ICE	I	For ICE with 65C02
		TEST	I	Test pin
Total pin No. 111pin				

SYSTEM REGISTER (1)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W
MEMORY										
$1F00	**ROM_BNK1**	BNK1.7	BNK1.6	BNK1.5	BNK1.4	BNK1.3	BNK1.2	BNK1.1	BNK1.0	R/W
$1F01	**ROM_BNK2**	BNK2.7	BNK2.6	BNK2.5	BNK2.4	BNK2.3	BNK2.2	BNK2.1	BNK2.0	R/W
$1F0B	**RAM_BNK**	BNK3.7	BNK3.6	BNK3.5	BNK3.4	BNK3.3	BNK3.2	BNK3.1	BNK3.0	R/W
$1F02	**RAM_NO**	-	-	-	-	-	RAM.2	RAM.1	RAM.0	R/W
$1F03	**ROM_NO**	-	-	-	-	-	ROM.2	ROM.1	ROM.0	R/W
$1F0C	**EX_RAM_E**	enable	-	-	-	-	-	-	-	W
$1F0D	**EX_ROM_S**	enable	-	-	-	-	-	-	-	W
SYSTEM CONTROL										
$1F04	**SPECIAL1**	PD	-	-	PC_H	PC_L	PB_H	PB_L	PA_H	R/W
$1F05	**SPECIAL2**	EXTINT	UART	WDT	REMO	-	-	-	-	R/W
$1F06	**SYS_CTRL**	D.7	D.6	D.5	D.4	D.3	-	-	-	R/W
$1F07	**PWR_SAV**	-	-	-	-	-	-	X32KEN	SPDUP	R/W
$1F08	**RESET**	-	-	-	-	-	WT	WD	IPA	R
$1F09	**LPD_CTRL**	LPD_EN	-	-	-	-	-	-	LPD	R/W
$1F0A	**CONFIG**	SPM	-	-	-	-	-	-	CONFIG	R or W
INTERRUPT										
$1F10	**NMI_IE**	NMISR1	-	-	-	-	NMISR	NMIST	NMIPA	R/W
$1F11	**NMI_IF**	NMISR1	-	-	-	-	NMISRI	NMISTI	NMIPA	R
$1F12	**IRQ_IE**	IRQSR2	IRQWT	IRQEXT	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	R/W
$1F13	**IRQ_IF**	IRQSR2	IRQWT	IRQEXT	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	R
TIMER										
$1F14	**TM0_CTRL**	BD/TM	T/RCLK	-	-	TM0.3	TM0.2	TM0.1	TM0.0	W
$1F15	**TM0COUNT**	T7	T6	T5	T4	T3	T2	T1	T0	R/W
$1F16	**TM1_CTRL**	BD/TM	T/RCLK	-	-	TM1.3	TM1.2	TM1.1	TM1.0	W
$1F17	**TM1COUNT**	T7	T6	T5	T4	T3	T2	T1	T0	R/W
$1F18	**TM2_CTRL**	-	-	-	-	-	TM2.2	TM2.1	TM2.0	W
$1F19	**TM2COUNT**	T7	T6	T5	T4	T3	T2	T1	T0	R/W
$1F1A	**WKT_CTRL**	-	-	-	-	-	-	WKT.1	WKT.0	W
$1F1B	**WDT_RST**	-	-	-	-	-	-	-	-	W
CARRIER SYNTHIZER										
$1F1C	**RF_CTRL**	enable	-	-	-	-	-	-	RFQ.0	W
$1F1D	**RF_OUTPUT**	-	-	-	-	-	-	-	DATA	R/W
INPUT/OUTPUT PORT										
$1F20	**IPA_MODE**	-	-	-	-	-	-	-	Edge/level	W
$1F21	**PA**	PA.7	PA.6	PA.5	PA.4	PA.3	PA.2	PA.1	PA.0	R/W
$1F22	**PAC**	PAC.7	PAC.6	PAC.5	PAC.4	PAC.3	PAC.2	PAC.1	PAC.0	R/W
$1F23	**PB**	PB.7	PB.6	PB.5	PB.4	PB.3	PB.2	PB.1	PB.0	R/W
$1F24	**PBC**	-	-	-	-	-	-	PBC.H	PBC.L	R/W
$1F25	**PC**	PC.7	PC.6	PC.5	PC.4	PC.3	PC.2	PC.1	PC.0	W
$1F26	**PD**	PD.7	PD.6	PD.5	PD.4	PD.3	PD.2	PD.1	PD.0	R/W
$1F27	**PDC**	PDC.7	PDC.6	PDC.5	PDC.4	PDC.3	PDC.2	PDC.1	PDC0	R/W
$1F28	**PDS**	PDS.7	PDS.6	PDS.5	PDS.4	PDS.3	PDS.2	PDS.1	PDS.0	R/W
LCD Interface										
$1F29	**LCS**	-	-	-	-	-	CSH/L	SEL1	SEL0	W
$1F2A	**LRS**	-	-	-	-	-	-	-	RS	W
$1F2B	**RD_DATA**	7	6	5	4	3	2	1	0	R
$1F2C	**LCD0**	7	6	5	4	3	2	1	0	R/W
$1F2D	**LCD1**	7	6	5	4	3	2	1	0	R/W

SYSTEM REGISTER (2)

SPEECH & SOUND CONTROL										
$1F30	**TG1_L**	TG1.7	TG1.6	TG1.5	TG1.4	TG1.3	TG1.2	TG1.1	TG1.0	R/W
$1F31	**TG1_H**	TG1.15	TG1.14	TG1.13	TG1.12	TG1.11	TG1.10	TG1.9	TG1.8	R/W
$1F32	**TG1_CTL**	enable	loop	-	-	-	-	CS1	CS0	W
$1F33	**TG2_L**	TG2.7	TG2.6	TG2.5	TG2.4	TG2.3	TG2.2	TG2.1	TG2.0	R/W
$1F34	**TG2_H**	TG2.15	TG2.14	TG2.13	TG2.12	TG2.11	TG2.10	TG2.9	TG2.8	R/W
$1F35	**TG2_CTL**	enable	loop	-	-	-	-	CS1	CS0	W
$1F36	**TG1_ENV**	-	E6	E5	E4	E3	E2	E1	E0	R/W
$1F37	**TG2_ENV**	-	E6	E5	E4	E3	E2	E1	E0	R/W
$1F39	**SR1_COUNT(L)**	SR1.7	SR1.6	SR1.5	SR1.4	SR1.3	SR1.2	SR1.1	SR1.0	R/W
$1F3A	**SR1_COUNT(H)**	SR1.15	SR1.14	SR1.13	SR1.12	SR1.11	SR1.10	SR1.9	SR1.8	R/W
$1F3B	**SR1_CTRL**	enable	loop	-	-	-	-	CS1	CS0	W
$1F3C	**SR2_COUNT(L)**	SR2.7	SR2.6	SR2.5	SR2.4	SR2.3	SR2.2	SR2.1	SR2.0	R/W
$1F3D	**SR2_COUNT(H)**	SR2.15	SR2.14	SR2.13	SR2.12	SR2.11	SR2.10	SR2.9	SR2.8	R/W
$1F3E	**SR2_CTRL**	enable	loop	-	-	-	-	CS1	CS0	W
$1F3F	**VOICE1**	D7	D6	D5	D4	D3	D2	D1	D0	W
$1F41	**VOICE2**	D7	D6	D5	D4	D3	D2	D1	D0	W
$1F43	**PWM_CTL**	SR2_E	-	-	-	-	-	-	ST_ON	R/W
$1F44	**SD_CTL**	PWM/DAC	-	-	-	DAC2EN	PWM2EN	DAC1EN	PWM1EN	R/W
UART										
$1F50	**STBUF**	TD.7	TD.6	TD.5	TD.4	TD.3	TD.2	TD.1	TD.0	R/W
$1F51	**SRBUF**	RD.7	RD.6	RD.5	RD.4	RD.3	RD.2	RD.1	RD.0	R
$1F52	**SCON**	SM	-	-	REN	TB8	RB8	-	-	R/W

Functional Descriptions

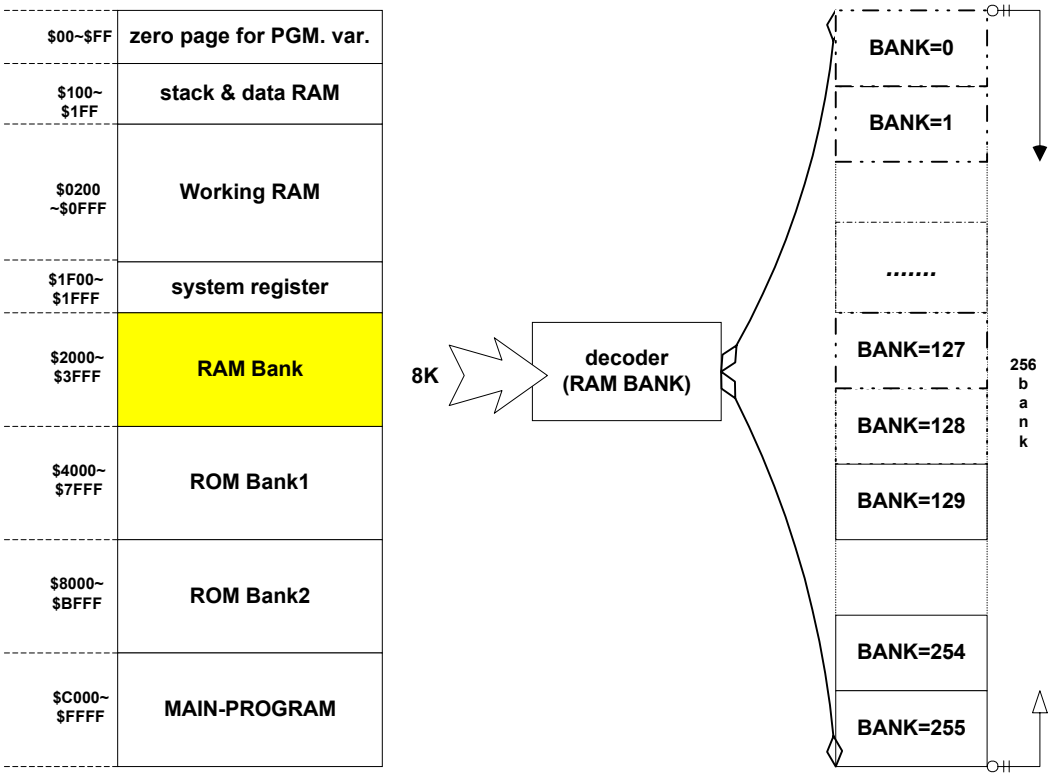
Memory Allocation

RAM allocation

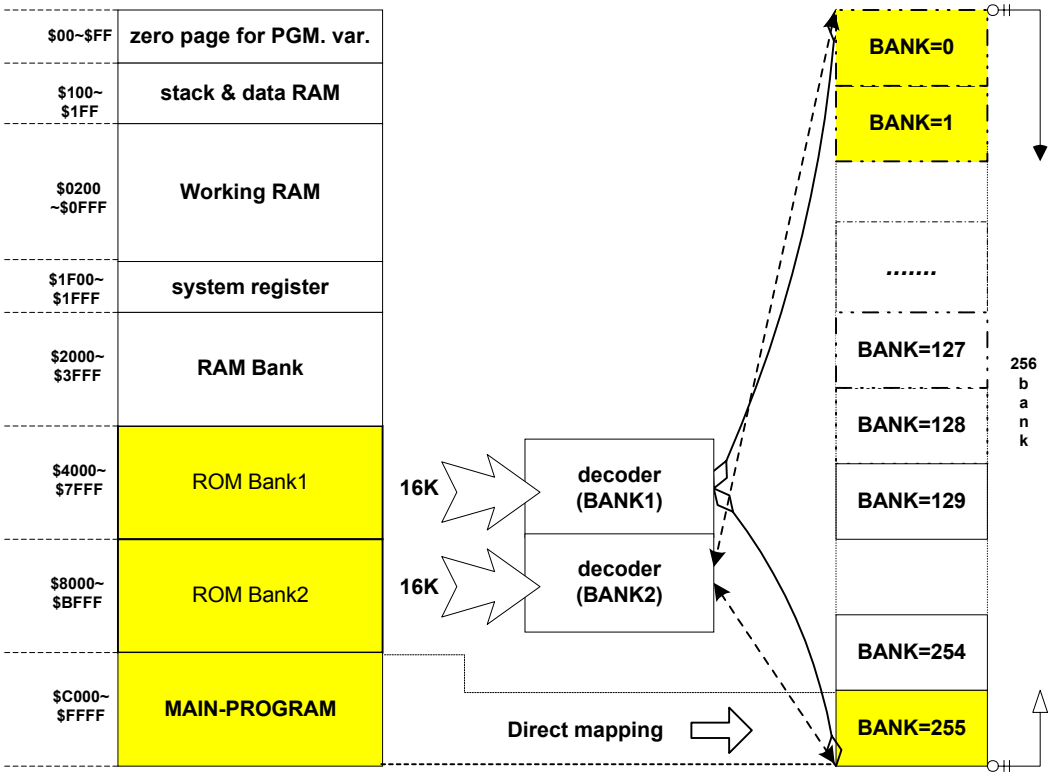
SH58201 provides 12k x 8 bit RAM, including data memory, stack, programming variable & system register

RAM ADDRESS	Description
$0000~$00FF	Zero page for program variable
$0100~$01FF	Stack Area
$0200~$0FFF	Working RAM
$2000~$3FFF	Working RAM (Window for Bank)
$1F00~$1FFF	System register

RAM mapping



ROM allocation map



ROM mapping

Under 65C02 core structure, the program counter (16 bit) can only addressed 64K x 8 bit space, hence, for the ROM/RAM size above 64K x 8 bit, the SH58201 offers the method of switching banks to extend the CPU address space. This chip offers 3 bank mapping areas, one is located at $2000~$3FFF(8K), one is located at $4000~$7FFF(16K) and the other is located at $8000~$BFFF (16K). There are 256 banks derived from each mapping area decoding.
There are 2 chip selections for choosing memory modules. For $2000~$3FFF, this block indicates 8K x 8bit while at $4000~$7FFF and $8000~$BFFF, this block will indicate16K x 8 bit. Hence, the system can address max. 2048K x 8 bit (RAM) and 4096K x 8 bit (ROM).

Bank switch register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F00	ROM_BNK1	BNK1.7	BNK1.6	BNK1.5	BNK1.4	BNK1.3	BNK1.2	BNK1.1	BNK1.0	R/W	11111111
$1F01	ROM_BNK2	BNK2.7	BNK2.6	BNK2.5	BNK2.4	BNK2.3	BNK2.2	BNK2.1	BNK2.0	R/W	11111111
$1F0B	RAM_BNK	BNK3.7	BNK3.6	BNK3.5	BNK3.4	BNK3.3	BNK3.2	BNK3.1	BNK3.0	R/W	11111111
Initial setting		Default: :: ROM_BNK1, ROM_BNK2=FFh, RAM_BNK = FFh									

(A). The 16-bit program counter of 65C02 just can address 64K x 8 bits memory space. Bank switch is used to extend the CPU address space. The two upper 16K bytes ROM ($4000~$7FFF & $8000~$BFFF) blocks map to coordinate bank (according to the BANK register, listed as follows:) while the middle 8K bytes RAM blocks map to coordinate bank.

(B). The ROM & RAM mapping is described as follows:

ADDRESS	ROM_BNK1 ROM_BNK2 =0	ROM_BNK1 ROM_BNK2 =1	.....	ROM_BNK 1ROM_BN K2=238	ROM_BNK 1ROM_BN K2=239	ROM_BNK 1ROM_BN K2=240	....	ROM_BNK 1ROM_BN K2=254	ROM_BNK 1ROM_BN K2=255
$C000~$FFFF									0K~16K
$4000~$7FFF	4080~4096 K	4064~4080 K		272~288K	256~272K	240~256K		16~32K	0K~16K
$8000~$BFFF	4080~4096 K	4064~4080 K		272~288K	256~272K	240~256K		16~32K	0K~16K

ADDRESS	RAM_BNK =0	RAM_BNK =1	.....	RAM_BNK =222	RAM_BNK =223	RAM_BNK =224	....	RAM_BNK =254	RAM_BNK =255
$0000~$1FFF									
$2000~$3FFF	2040~2048 K	2032~2040 K		264~272K	256~264K	248~256K		8~16K	0~8K

Unit: Byte

(C). Bank Switch:

(1). When the SH58201 is powered on, the ROM_BNK1, ROM_BNK2 & RAM_BNK are initially switched to bank FFh.

(2). In order to linearize the ROM mapping, the address $C000~$FFFF will direct map to the bank 255, listed above, and it will meet the rule of the vector table for the 65C02(the vector table should be located at $FFFA~$FFFF)

(3). Wherever the ROM bank is, if the program counter read the $C000~$FFFF area, the bank must be switched to bank 255, thus, the program code and the vector table will not be lost in the bank switching. (the value of ROM_BNK1, ROM_BNK2 will not be changed)

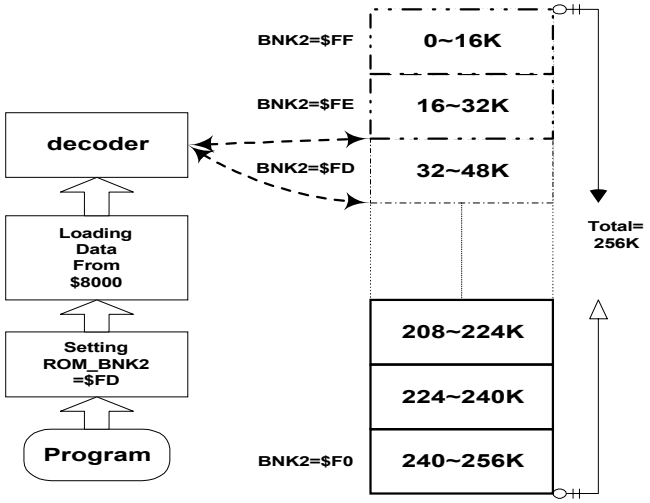
(4). The SH58201 build in 256K x 8 bit ROM, hence, in the Normal Mode (shown in the next page), ROM_BNK1 & ROM_BNK2 only can set in the following range: $F0~$FF.

(5). If the user need the ROM size over than 256K x 8 bit, the SH58201 also supply the External ROM access solution:

Step 1: Into the special mode by jumping the SPMOD pin to high (SPMOD=1), set proper ROM size by writing $1F03 (ROM size select register).

Step 2: Choose the External ROM mode by setting the M1, M2.

Example:



Chip Operation Mode Select

Develop environment switch (Mode1, Mode2)

(1). M1, M2: choose the developing environment In ICE or Normal mode with Internal ROM or External ROM.

MODE	MEMORY ACCESS	M2	M1
Normal Mode (internal CPU)	Internal ROM	0	0
	External ROM	0	1
ICE Mode (External CPU)	Internal ROM	1	0
	External ROM	1	1
M2: Choose Develop in the ICE mode or internal CPU mode M1: Choose the ROM mode in the Internal ROM or External ROM			

(2). In the case of internal ROM mode, that is [M2, M1]=[0,0] or [1,0]. If any extension ROM is connected to the SH58201 address bus, when programme accesses the address above 256K byte, the SH58201's address decoder will decode to the external ROM. (In the case of internal ROM mode, the internal ROM and external ROM can be co-existed.)

(3). It is suggested when the internal ROM mode is selected, for the build-in ROM, it can be used to store the important documents or data or password, and so on, and the external ROM usually contains the main programme.

(4). In the case of external ROM mode, it will be unavailable to access the build-in ROM (256K byte). That is to say, in the external ROM mode, the address decoder will decodes to external ROM.(Not Access the built-in ROM)

Special Mode control (SPMOD)

(1). The SPMOD pin is used to control the function block Enabled/Disabled for the SH582xx expansion serial products.

(2). The special mode environment is only existed in the SPMOD pin being set.(that is: SPMOD =1). And the following register would be useful.

Special mode control register (SPMOD =1)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F04	**SPECIAL1**	PD	-	-	PC_H	PC_L	PB_H	PB_L	PA_H	R/W	1--11111
$1F05	**SPECIAL2**	EXTINT	UART	WDT	REMO	-	-	-	-	R/W	1111----
$1F0A	**CONFIG**	SPM	-	-	-	-	-	-	CONFIG	R or W	0------0

Control bit	Function description	Default	
	Special Mode : SPMOD=1	**SPMOD=0**	**SPMOD=1**
PA_H	Enable/Disable the function block of PORTA's HIGH nibble (0:disable)	1	1
Note: the use of PB_H, PC_H is the same as PA_H			
PB_L	Enable/Disable the function block of PORTB's LOW nibble (0:disable)	1	1
Note: the use of PC_L is the same as PB_L			
PD	Enable/Disable the function block of PORTD (0:disable)	1	1
REMO	Enable/Disable the function block of CARRIER GENERATOR (0:disable)	1	1
WDT	Enable/Disable the function Block of WATCHDOG (0:disable)	1	1
UART	Enable/Disable the function Block of UART (0:disable)	1	1
EXTINT	Enable/Disable the function Block of External Interrupt (0:disable)	1	1

(1). The control bit of WDT is used to turn ON/OFF Watchdog function block, there are several ways to disable the Watchdog timer.

(1.a). Because the clock source of Watchdog timer is come from the 32.768K X'tal oscillator, hence, disable the 32.768K X'tal by setting the control bit of X32KEN ($1F07 PWR_SAV) as “0” will turn off the Watchdog timer clock.

(1.b). Disable the control bit of WDT ($1F05,SPECIAL2) can also turn off the Watchdog function.

(2). The control bit of REMO is used to turn ON/OFF the CARRIER GENERATOR function block. If it is enabled, the remote output pin is shared with the PORTD.3.

(3). The control bit of EXTINT is used to turn ON/OFF the External Interrupt function block. If it is enabled, the external interrupt input pin is shared with the PORTD.0.
(4). The control bit of UART is used to turn ON/OFF the Universal Asynchonous Receiver_Transmitter function block. If it is enabled, the transmitter output pin is shared with the PORTD.1 as well as the receiver input pin with the PORTD.2.

Configure Setting control register ($1F0B)

	R/W	Function Description	Default
SPM	Read Only	Read the status of SPMOD Pin	rely on SPMOD pin
CONFIG	Write/Only	Driver the Configure LED	0

Note:

(1). For the SH582xx expansion products, some will not have the PA high nibble function or REMO. In this case, it is necessary to set properly the corresponding bit to enable or disable the relevant function. Otherwise, the SH58201 can not be used to emulate the different serial products.
(2). Only entering the special mode situation (the SPMOD pin is connected to HIGH), the ROM and RAM size register just can be used to control the ROM size, RAM size for the different extension product.
(3). In the Special mode: Default = enable all function.
(4). In the SH58201 mode, all the functions are enabled.

Configure setting method

(1). Set the SPMOD pin to HIGH (only in the SPMOD =1, the control register of SPECIAL1, SPECIAL2 is useful.)
(2). Set the control bit of CONFIG ($1F0A) to HIGH. (It will turn the external LED OFF to announce the user)
" IT IS CONFIGURATION SETTING NOW, BE WAITING " At the same time, this signal will also send to the system to permit the Configuration setting of SH58201.
(3). Properly set the SPECIAL MODE control register of SPECIAL1, SPECIAL2 (according to the feature of NT582XX expansion series, turn ON/OFF the coordinate control bit)
(4). Properly set the RAM and ROM size register ($1F02, $1F03)
(5). Properly set the configuration setting of SH58201.
(6). Set the control bit of CONFIG ($1F0A) to LOW.(It will turn the external LED ON to announce the user:
" CONFIGURATION SETTING END ", To set the SPMOD pin to LOW right now. At the same time, it means that the SH58201 has finished the system configuration setting.

RAM Size Selection (SPMOD=1)

RAM size select register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F02	RAM_NO	-	-	-	-	-	RAM.2	RAM.1	RAM.0	R/W	-----000

(A). The SH58201 chip includes a lot of different RAM sizes. It can be used to emulate the different chips in SH582xx series by choosing a proper RAM size (SPMOD =1)

(B). Since the different RAM size, if it is selected improperly, it won't get right result. That is to say, if the RAM size is set as 2K under the SPMOD=1, the programme accessing range will not exceed (Read/Write) the address of 2K.

RAM.2	RAM.1	RAM.0	RAM size (byte)	SPMOD=0	SPMOD=1
0	0	0	12K	Default	Default
0	0	1	8K		
0	1	0	4K		
0	1	1	2K		
1	0	0	1.5K		
1	0	1	1K		
1	1	×	0.5K		

(C). Data RAM (program variable) can be shared with the stack. (Unit: Byte)

RAM Size	Zero Page Available	BYTE	Stack Available	BYTE	Other(program Variable)	BYTE
12K	0000h~00FFh	256	0100h~01FFh	256	0200h~0FFFh	3584
					2000h~3FFFh	8192
8K	0000h~00FFh	256	0100h~01FFh	256	0200h~0FFFh	3584
					2000h~2FFFh	4096
					3000h~3FFFh (reserved)	
4K	0000h~00FFh	256	0100h~01FFh	256	0200h~0FFFh	3584
2K	0000h~00FFh	256	0100h~01FFh	256	0200h~07FFh	1536
1.5K	0000h~00FFh	256	0100h~01FFh	256	0200h~05FFh	1024
1K	0000h~00FFh	256	0100h~01FFh	256	0200h~03FFh	512
0.5K	0000h~00FFh	256	0100h~01FFh	256		

External RAM control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F0C	EX_RAM_E	enable	-	-	-	-	-	-	-	W	0-------

enable	Description
0	External SRAM disable (default)
1	External SRAM enable (Pin CSB2=0; low active)

Note:

This bit7 of the external RAM control register is used to control the external RAM chip select signal. If the value of EX_RAM_E is ''0" (default), the external RAM is not available. That means the system can only access the internal RAM. At this time, the RAM_BNK register ($1F0B) is unavailable for operation.

If the value of EX_RAM_E is ''1", the external RAM is available. That is to say, when the system RAM accessing range exceeds the relevant size (maximum: 12Kbyte) controlled by certain setting of the RAM.2~RAM.0bits, the operation of RAM reading/writing can access the external RAM automatically through proper writing the value of the RAM_BNK register ($1F0B). But, if the programme needs accessing the internal RAM (Range: $2000 ~ $3000), the EX_RAM_E bit must be writen to "0" again. Otherwise the accessing operation will not be executed. Therefor, the operating for this bit (enable) at $1F0C is always available whenever the SPMOD pin is fixed to high or low.

ROM Size Selection (SPMOD=1)

ROM size select register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F03	ROM_NO	-	-	-	-	-	ROM.2	ROM.1	ROM.0	R/W	-----100

(A). The SH58201 chip includes a lot of different ROM sizes. It can be used to emulate the different chips in SH582xx series by choosing a proper ROM size (SPMOD =1)

(B). Since the different ROM size, if it is selected improperly, it won't get right result.

ROM.2	ROM.1	ROM.0	ROM Size	Bank Limited	SPMOD=0	SPMOD=1
0	0	0	4M	00 h ~ FF h		
0	0	1	2M	80 h ~ FF h		
0	1	0	1024K	C0 h ~ FF h		
0	1	1	512K	E0 h ~ FF h		
1	0	0	256K	F0 h ~ FF h	Default	Default
1	0	1	128K	F8 h ~ FF h		
1	1	×	64K	FC h ~ FF h		

(C). For the different ROM size, if it is set improperly, it won't be got right result. For instance, if the ROM size is selected 128K, in the SPMOD=1, the programme accessing (Read) won't exceed the address of 128K.

(D). When the ROM size is above 256K byte, The system can be worked in the purely external ROM or internal and external ROM co-existed by setting the M1, M2 pins. (see in the page 10)

External ROM control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F0D	EX_ROM_S	enable	-	-	-	-	-	-	-	W	0-------

enable	Description
0	External ROM enable (Pin CSB0=0, CSB1=1; low active) (default)
1	External Flash ROM enable (Pin CSB0=1, CSB1=0; low active)

Note:

(1). When in the external ROM case (M1=1), if the program counter reads the $C000~$FFFF area, the CSB0 pin will always be active. That means the system CPU can only fetch codes from the external EPROM, regardless the M2 pin is fixed to high or low, regardless the value of EX_ROM_S is set to "1" or "0", either.

(2). If the value of EX_ROM_S is "0" (default), when the PC's accessing range exceeds $C000~$FFFF under the external ROM case, the system can also access the external EPROM.

(3). If the value of EX_ROM_S is set to "1" by program writing, when the PC's accessing range exceeds $C000~$FFFF, the system must access the external FLASH ROM automatically (Pin CSB1=0/CSB0=1, low active), regardless M1 is fixed to high or low.

Dual Clock Selection

The SH58201 offers dual clock selection one for RC/Crystal oscillation, the other is 32.768K oscillator for real time clock. At the same time, MCU's operating speed is also software programmable, it is controlled by setting the following register.

System control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F06	SYS_CTRL	D.7	D.6	D.5	D.4	D.3	-	-	-	R/W	00000---

D.7	System Clock Source select bit
0	Select system clock source from RC/Crystal
1	Select system clock source from time base clock (32.768K Crystal)
D.6 D.5	When D.7=0, this bit is used to select clock source frequency
0 0	F_{OSC} = 4M (or 3.58M)
0 1	F_{OSC} = 8M
1 0	F_{OSC} = 12M
1 1	F_{OSC} = 16M

D.4	D.3	Prescaler
0	0	/8
0	1	/4
1	×	/2
When D.7=0, CPU clock is fetched from this prescaler		

Note:

(A). System oscillator component must be connected and it can be RC or crystal type according to the "XROPT" pin state(pad option). As to the time base clock,32768 Hz,Crystal oscillator may be connected or not depended on the application condition.

(B). When the 32.768K crystal is connected, the system register $1F07 "X32KEN" (see the Next page) should be set to “1” to enable 32.768KHz crystal oscillator.

(C). The CPU clock is 32768Hz when bit7(D.7) is set to “1”. Normally, this situation just happened at "STANDBY" mode to keep LCD display in regular.

(D). When 32.768k is used as system clock source, that is D.7=1, then D[6:3] are no more effected.

(E). d[7:3]=00h(default). That means "Clock Source is not from 32.768KHz, F_{OSC}=4MHz, and the Prescaler = /8 ", So the system will work on 500K Hz.

Caution:

The Tone frequency generator circuit of Melody will vary in the different operating voltage, by properly setting this bit, it will be suitable for the different application environment.

Low Power Detection

Function of LPD circuit

The low power detection (LPD) is used to monitor the supply voltage and generate an internal flag for indicating the battery energy having been much lower that may damage the operation status of system. The appearance of low voltag signal can remind user to replace the battery.

LPD operation

When a SH58201 operates in the 3V power supply condition, the LPD voltage is defined as 2.5V. Therefore, if the power supply voltage is any lower than 2.5V, the LPD circuit must detect out and then set the flag (bit0 of the LPD_CTRL) as “1”.

Electrical Property	V_{DD}	V_{LPD}
	3.0V	2.5V

LPD control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F09	LPD_CTRL	LPD_EN	-	-	-	-	-	-	LPD	R/W	0------0

LPD	Description	R/W
1	“1” means the CPU detects out the $V_{DD} \leqq V_{LPD}$ (0: $V_{DD} > V_{LPD}$)	R

LPD_EN	Description	R/W
1	LPD enable (otherwise: disable)	W

(1). Enable the LPD detection by set LPD_EN =1, Default: LPD_EN = 0 (disable)
(2). If the LPD is enabled, the flag (LPD) will be set to “1” when the LPD circuit has detected out $V_{DD} \leqq V_{LPD}$,. In this case, the programme maybe turn into the LPD service subroutine to indicate that it's time to replace the supply battery.

Power Saving Control

To reduce power consumption, this chip offers 2 power-saving steps:
(1). The 65C02 power saving method: STOP instruction
(2). Power saving register control: to control ON/OFF the 32.768KHz oscillator

Power Saving register:

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F07	PWR_SAV	-	-	-	-	-	-	X32KEN	SPDUP	R/W	------11
$1F08	RESET	-	-	-	-	-	WT	WD	IPA	R	-----000

Control bit	Description	Default
X32KEN	Turn ON/OFF 32.768K crystal. If CPU & Crystal is turned off at the same time, the system will be shut down. That is, only the I/O PortA can wake up the chip.	1 (Turn-ON)
SPDUP	Speed up the 32K Oscillator in the CPU turn-on status.(1:turn on the function) It should be noticed that turnning off the function when the CPU is stable.	1 (Turn-ON)

RESET (reset status register):

WT	WD	IPA	Description
		1	System was reset by External trigger(PORTA interrupt)
	1		System was reset by Watchdog
1			System was reset by wake up timer

Note:

(1). Once the operation of reading this reset status register is occured, the 3-bits will be immediately cleared on the next ph0 rising edge. This register can be used to detect which source has caused the system reset. After reading operation, the register's status will be cleared so it can be ready for next reset happening. In addition, the most important thing is that pin RSTB causing the system reset will clear all status of this register firstly and immediately. (6502 power on reset vector is located at the $FFFC ~$FFFD)

(2). Before STOP instruction is commanded in the program, if the 32.768K oscillator has been turn off, there is only one way to wake the CPU up---that is: PORTA interrupt.

(3). Before STOP instruction is commanded in the program, if the 32.768K oscillator is still turned on, there will have three ways to wake the CPU up—they are: Wake up timer, Watchdog timer, and the PortA interrupt.

(4) When the system is in the power saving condition (after executing STOP instruction), the PORTA interrupt can wake up CPU. At this time, there are two types of interrupt provided for different applications. One is low level triggering (default) as well as the other is edge triggering (falling active). The different function is selected by the status of the IPA mode control register (IPA_MODE) bit0.

IPA mode control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F20	IPA_MODE		-	-	-	-	-	-	Edge/Level	W	-------0

Edge/Level	Description
0	PORTA interrupt level triggering (low active) (default)
1	PORTA interrupt edge triggering (falling edge)

Interrupt-NMI & IRQ

NMI enable

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F10	**NMI_IE**	NMISR1	-	-	-	-	NMISR	NMIST	NMIPA	R/W	0----000

(A). The register is used to **decide** which NMI source will be activated.(Non-Maskable Interrupt).
(B). 0: Disable (default)
1: Enable (If the bit is set to "1", that means the relevant event can interrupt CPU.)

NMISR1	NMIPA	DESCRIPTION
-	1	Input PORTA trigger
1	-	SR1 Counter counts overflow

NMI request flag register:

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F11	**NMI_IF**	NMISR1	-	-	-	-	NMISRI	NMISTI	NMIPA	R	0----000

(A). The register is used to **record** NMI request status. For Example, if the NMI source (SR1) counts overflow from FFFFh to 0000h, the bit7 of this register will be set. In this time, if the coordinate NMI_IE is set to "1", the NMI will be triggered, and the program counter will point to the NMI vector.(6502 NMI vector is located at the $FFFAh~$FFFBh)
(B). When the operation of reading this register, the status of this register will be cleared right now.

0=inactive (the Counter don't count overflow yet…….Default)
1=active (the Counter counts overflow from $FF to $00, NMI flag activates)

IRQ enable register:

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F12	**IRQ_IE**	IRQSR2	IRQWT	IRQEXT	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	R/W	00000000

(A). The register is used to **decide** which IRQ source will be triggered (IRQ: Interrupt Request).
(B). 0: Disable (default)
1: Enable (If the bit is set to "1", that means the relevant event can interrupt CPU.)

IRQSR2	IRQWT	IRQEXT	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	DESCRIPTION
							1	Timer0 count overflow
						1		Timer1 count overflow
					1			Timer2 count overflow
				1				Input PORTA trigger
			1					Input PORTB trigger
		1						external interrupt
	1							Wake up timer overflows
1								SR2 Counter counts overflow
0: Disable (Default)								1: Enable

IRQ request flag

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F13	**IRQ_IF**	IRQSR2	IRQWT	IRQEXT	IRQPB	IRQPA	IRQT2	IRQT1	IRQT0	R	00000000

(A). The register is used to **record** individually IRQ request flag, simply as NMI_IF.
(B). The IRQ will be triggered when the IRQ_IE.x=1 and the corresponding bit of IRQ_IF=1 together. At this time, IRQ will activate and the program counter will start from the IRQ vector address. (65C02's IRQ vector is defined in $FFFEh ~ $FFFFh)
(C). After IRQ occured, the relevant bit of IRQ request flag was set to "1". If the IRQ_IF flag won't be cleared, the IRQ will be triggered immediately again (because the IRQ_IE.x was still enabled). The unpredicted thing will be happened (Ex: stack overflow). Therefore, the IRQ request (IRQ_IF) must be cleared immediately by reading the IRQ_IF at the beginning of the IRQ interrupt service subroutine.

Note:

(A). When NMI enable register (NMI_IE) is set to "1", the SH58201 can service multi-level interrupt. However, there is only one NMI vector for 65C02, therefore, it is necessary to reset the NMI_IF register if there are several (NMI) interrupt sources shared in the program. In this situation, it is important to store the value of NMI_IF into the program variable before clearing NMI_IF flag. Then, it is available to judge the (NMI) interrupt source causing the NMI.
(B). If the corresponding NMI_IE.x is set to "0", the NMI_IF.x will not be set to "1" while NMI source is coming up.
(C). Interrupt priority: NMI >> IRQ

Example:

```
        MAIN PROG                       ISR
……
        LDA     IRQ_IF                  LDA     IRQ_IF
                                        STA     wSAVE_FLAG
        LDA     #01                     ……
        STA     IRQ_IE                  ……
……                                      ……
        this programme can be triggered by timer0 interrupt.
        When TM0 counts from FFH→00H
        the PC. will jump to Interrupt Service Routine.
```

Timer / Counter

SH58201 has several timers: Timer0, Timer1, Timer2, Wake-up timer and Watchdog timer.

Timer0

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F14	**TM0_CTRL**	BD/TM	T/RCLK	-	-	TM0.3	TM0.2	TM0.1	TM0.0	W	00--0000
$1F15	**TM0COUNT**	T7	T6	T5	T4	T3	T2	T1	T0	R/W	00000000

(1). Timer0 is a 8 bit up-count timer. When it counts overflow from FFh to 00h, it will generate a timer IRQ request (and set the coordinate IRQ request flag IRQT0=1). If the corresponding bit of IRQ_IE is set to "1" then timer0 interrupt will be activated.
(2). The clock source of Timer0 can be system clock or external crystal (32.768K).
(3). Timer0 starts counting when the TM0COUNT is setting.

TM0_CTRL(timer0 control register):

BD/TM	Timer0 function control
0	General timer (default)
1	Timer0 used as Baud rate generator
T/RCLK	**Transmit/Receive clock selection (available only when BD/TM=1)**
0	Timer0 overflow used as receiver clock (default)
1	Timer0 overflow used as transmitter clock
TM0.3	**Control timer0 enable or disable**
0	Disable
1	Enable
TM0.2	**Control auto reload function**
0	Disable
1	Enable (always enable when BD/TM=1)

TM0.1	TM0.0	Description			TM0 divisor (TM0COUNT)	Frequency from TM0
		Timer 0 clock source from				
		System oscillator (assume 8MHz, and /2 mode)	Pre-scale	Timer 0 clock input		
0	0	System clock (4MHz)	/65536	61.04Hz	1(FF) ~ 256(00)	61.04~0.24Hz
0	1	System clock (4MHz)	/2048	1953.13Hz	1(FF) ~ 256(00)	1953.13~7.66Hz
1	0	System clock (4MHz)	/2	2MHz	1(FF) ~ 256(00)	2M~7843.14Hz
1	1	32.768KHz or 31.25KHz	/8	4096Hz or 3096.25Hz	1(FF) ~ 256(00)	4096.00~16.06Hz or 3096.25~12.14Hz

(A). TM0.1 and TM0.0 are used to decide the pre-scale values.
(B). If the external clock32.768K) is not connected to the system, then TM0.1=1 and TM0.0=1 will cause the Timer0 to change the source from 32.768KHz to the system clock, 31.25K.
(C). If BD/TM=1, TM0.1 and TM0.0 will choose the different prescaler values which will be described in detail as follow.

TM0.1	TM0.0	Description			TM0 divisor (TM0COUNT)	Frequency from TM0
		Timer 0 clock source from		Timer 0 clock input		
		System oscillator (assume 8MHz, and /2 mode)	Pre-scale			
0	0	System clock (4MHz)	/1	4MHz	1(FF) ~ 256(00)	4M~15686.28
0	1	System clock (4MHz)	/2	2MHz	1(FF) ~ 256(00)	2M~7843.14Hz
1	×	System clock (4MHz)	/16	250KHz	1(FF) ~ 256(00)	250K~980.39Hz

TM0COUNT (timer0 counter register):

(A). In the read mode: The counter value can be accessed. But due to the asynchronous counting characteristics, the reading value may not be accurate! It must be careful for processing the value accessed from Timer0.

(B). In the write mode: This counter value can be programmed as preload counter. Writing data to this register can set initial counting value, thus it can change the peroid of the timer's overflowing.

Example:

If the clock source=system (4M), prescale=65536 (TM0.1=0, TM0.0=0), TM0_COUNT=128, then
Timer0 frequency={4000000 / (65536)} / {256-128}=0.48 Hz

When Timer0 is used as Baud rate generator (BD/TM=1), if oscillator frequency is 8MHz and in 1/2 mode (system clock=4MHz), prescaler=1, TM0_COUNT=48, then
the Baud rate (timer0's overflow)= {4000000 / 16} / {256-48}=1201.92 Hz
According to 1200 baud rate, the deviation is ({1201.92-1200}/1200) 0.16%.

If: (system clock=4MHz), prescaler=1, TM0_COUNT=243, then
the Baud rate (timer0's overflow)= {4000000 / 16} / {256-243}= 19230.77 Hz the relevant deviation is 0.16%

If: (system clock=4MHz), prescaler=1, TM0_COUNT=230, then
the Baud rate (timer0's overflow)= {4000000 / 16} / {256-230}= 9615.38 Hz the relevant deviation is 0.16%

If: (system clock=4MHz), prescaler=1, TM0_COUNT=204, then
the Baud rate (timer0's overflow)= {4000000 / 16} / {256-204}= 4807.69 Hz the relevant deviation is 0.16%

If: (system clock=4MHz), prescaler=1, TM0_COUNT=152, then
the Baud rate (timer0's overflow)= {4000000 / 16} / {256-152}= 2403.85 Hz the relevant deviation is 0.16%

Caution:

When the timer is used as baud rate generator, Timer0 and Timer1 can not be used in the same transmitter or receiver clock, simultaneously. Otherwise, the UART system will not operate correctly.

Timer1

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F16	**TM1_CTRL**	BD/TM	T/RCLK	-	-	TM1.3	TM1.2	TM1.1	TM1.0	W	01--0000
$1F17	**TM1COUNT**	T7	T6	T5	T4	T3	T2	T1	T0	R/W	00000000

TM1_CTRL (timer1 control register):

BD/TM	Timer1 function control
0	General timer (default)
1	Timer1 used as Baud rate generator
T/RCLK	**Transmit/Receive clock selection (available only when BD/TM=1)**
0	Timer1 overflow used as receiver clock (default)
1	Timer1 overflow used as transmitter clock
TM1.3	**Control timer1 enable or disable**
0	Disable
1	Enable
TM1.2	**Control auto reload function**
0	Disable
1	Enable (always enable when BD/TM=1)

TM1.1	TM1.0	Description			TM1 divisor (TM1COUNT)	Frequency from TM1
		Timer1 clock source from	Pre-scale	Timer 1 clock input		
0	0	Timer0 overflow			1(FF) ~ 256(00)	
0	1	System clock (4MHz)	/2048	1953.13Hz	1(FF) ~ 256(00)	1953~7.66Hz
1	0	32.768K or 31.25K	/16	2048Hz or 1953.13Hz	1(FF) ~ 256(00)	2048 ~ 8.03Hz or 1935.13 ~ 7.66Hz
1	1	32.768K or 31.25K	/2	16384Hz or 15625Hz	1(FF) ~ 256(00)	16384 ~ 64.25Hz or 15625 ~ 61.27Hz

(A). If the clock source of Timer1 comes from Timer0, a new preload value of timer1 for getting various frequency won't be loaded into the counter until TM0 overflows. Actually, it is available to change the contents of Timer0 to get a desired frequency from TM1 without preload a new value into TM1.

(B). If the external clock (32.768K) is not connected to the system, then TM1.1=1 and TM1.0=1 will cause the Timer1 to change the source from 32.768KHz to the system clock, 31.25K.

(C). If BD/TM=1, TM1.1 and TM1.0 will choose the different prescaler values from that mentioned above. The difference is described in detail as follow.

TM1.1	TM1.0	Description			TM1 divisor (TM1COUNT)	Frequency from TM1
		Timer 1 clock source from		Timer 1 clock input		
		System oscillator (assume 8MHz, and /2 mode)	Pre-scale			
0	0	System clock (4MHz)	/1	4MHz	1(FF) ~ 256(00)	4M~15686.28
0	1	System clock (4MHz)	/2	2MHz	1(FF) ~ 256(00)	2M~7843.14Hz
1	×	System clock (4MHz)	/16	250KHz	1(FF) ~ 256(00)	250K~980.39Hz

TM1COUNT (timer1 count register):

(A). In the read mode: The counter value can be accessed. But due to the asynchronous counting characteristics, the reading value may not be accurate! It must be careful for processing the value accessed from Timer1.
(B). In the write mode: This counter value can be programmed as preload counter. Writing data to this register can set initial counting value, thus it can change the peroid of the timer's overflowing.

Example:

If the clock source=timer0, system clock=(4M), prescale=2048(TM0.1=0, TM0.0=1), TM0_COUNT=128, TM1_COUNT= 64, Timer1 frequency={[4000000 /(2048)] / [256-128] } / [256-64] =0.08 Hz

When Timer1 is used as Baud rate generator (BD/TM=1), if oscillator frequency is 8MHz and in 1/2 mode (system clock=4MHz), prescaler=16, TM1_COUNT=48, then
the Baud rate (timer1's overflow)= {4000000 / 16} / {256-48}=1201.92 Hz
According to 1200 baud rate, the deviation is ({1201.92-1200}/1200) 0.16%.

If: (system clock=4MHz), prescaler=1, TM1_COUNT=243, then
the Baud rate (timer0's overflow)= {4000000 / 16} / {256-243}= 19230.77 Hz the relevant deviation is 0.16%

If: (system clock=4MHz), prescaler=1, TM1_COUNT=230, then
the Baud rate (timer0's overflow)= {4000000 / 16} / {256-230}= 9615.38 Hz the relevant deviation is 0.16%

If: (system clock=4MHz), prescaler=1, TM1_COUNT=204, then
the Baud rate (timer0's overflow)= {4000000 / 16} / {256-204}= 4807.69 Hz the relevant deviation is 0.16%

If: (system clock=4MHz), prescaler=1, TM1_COUNT=152, then
the Baud rate (timer0's overflow)= {4000000 / 16} / {256-152}= 2403.85 Hz the relevant deviation is 0.16%

Caution:

When the timer is used as baud rate generator, Timer0 and Timer1 can not be used in the same transmitter or receiver clock, simultaneously. Otherwise, the UART system will not operate correctly.

Timer2

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F18	TM2_CTRL	-	-	-	-	-	TM2.2	TM2.1	TM2.0	W	-----000
$1F19	TM2COUNT	T7	T6	T5	T4	T3	T2	T1	T0	R/W	00000000

TM2_CTRL (timer2 control register):

TM2.2	Control timer2 enable or disable
0	Disable
1	Enable
TM2.1	**Control auto reload function**
0	Disable
1	Enable

TM2.0	Description			TM2 divisor (TM2COUNT)	Frequency from TM2
	Timer2 clock source from	Pre-scale	Timer 2 clock input		
0	Timer1 overflow			1(FF) ~ 256(00)	
1	32.768K or 31.25K	/16	2048Hz or 1953.13Hz	1(FF) ~ 256(00)	2048~8.03Hz or 1953.13~7.66Hz

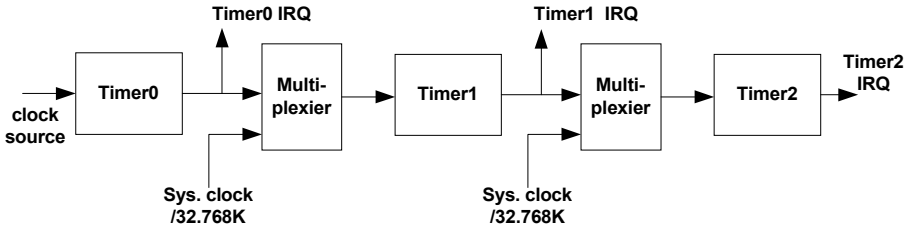
(A). If the clock source of Timer2 comes from timer1, a new preload value of TM2 for getting various frequency won't be loaded into the counter until TM1 overflows. Actually, it is available to change the contents of Timer1 to get a desired frequency from TM2 without preload a new value into TM2.

(B). If the external clock (32.768K) is not connected to the system, then TM2.0=1 will cause the Timer2 to change the source from 32.768KHz to the system clock, 31.25K.

TM2COUNT (timer2 count register):

(A). In the read mode: The counter value can be accessed. But due to the asynchronous counting characteristics, the reading value may not be accurate! It must be careful for processing the value accessed from Timer2.

(B). In the write mode: This counter value can be programmed as preload counter. Writing data to this register can set initial counting value, thus it can change the peroid of the timer's overflowing.



Timer cascade block diagram

Wakeup timer

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F1A	WKT_CTRL	-	-	-	-	-	-	WKT.1	WKT.0	W	------00

(A). The clock source of wakeup timer is 32.768K. It can be derived a different wake-up period by setting the WKT_CTRL register. If the associated bit of IRQ.IE (bit6) is set to "1", it will trigger the IRQ of wakeup timer when it counts overflow.

WKT.1	WKT.0	Timer-out period
0	0	0.25(sec)
0	1	0.5(sec)
1	0	1(sec)
1	1	2(sec)

(B). If the external crystal (32.768KHz) is not connected to the system or the oscillator is disabled (bit 1 of PWR_SAV=0), the Wakeup timer will be disabled either.

Watch dog timer (WDT)

WDT_RS T(watchdog reset register):

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W
$1F1B	WDT_RST	-	-	-	-	-	-	-	-	W

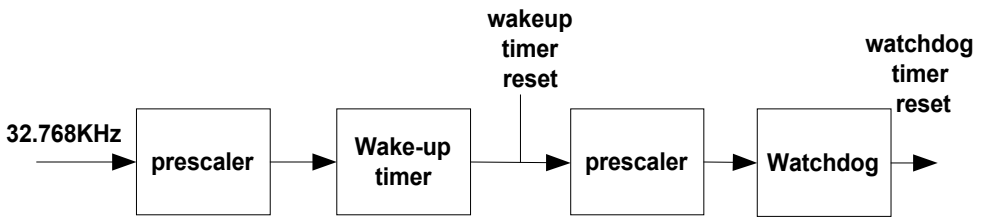
(A). The clock source of Watchdog timer is cascaded from wakeup timer. The Watchdog timer is designed for preventing a software malfunction or sequence jumping to an unknown location causing unpredictable results. It can be disabled by entering special mode (using **SPMOD** pin). If it is disabled, all executing for WDT will result in no operation.

(B). The period of watchdog timer is four times the wakeup timer. If the WDT is enabled, an overflow of Watchdog timer under the operation mode must enforce the system to create a **"RESET"** status. Therefore, for preventing it's timing out and generating a device RESET condition, it is necessary to write any data to the WDT_RST register.

The period of watchdog timer = 4 x (the period of wakeup timer)

(C). If the external crystal (32.768KHz) is not connected to the system or the oscillator is disabled (bit 1 of PWR_SAV=0), the Watchdog timer will be disabled either.

The cascade block diagram of Wakeup timer, Watchdog timer is as following:



I/O Port

The SH58201 provides 16 bits I/O (PA, PB), 8 O/P only port. (PC) and 1 special purpose I/O (PD)

PORT pull up control

(1). The pull-up devices are controlled by the port data registers (PA and PB) of each port. Hence, setting "1" to the relevant bit to turn ON the pull-up MOS individually.
(2). Internal pull-up MOS is only used in the INPUT mode.

Example:

If bit7 and bit2 of PORTA internal pull up are desired,

Step1. Setting #10000100b to the PORTA control register (input mode).
Step2. Setting #10000100b to the PORTA data register.

PORTA control register (bi-directional I/O):

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F21	**PA**	PA.7	PA.6	PA.5	PA.4	PA.3	PA.2	PA.1	PA.0	R/W	11111111
$1F22	**PAC**	PAC.7	PAC.6	PAC.5	PAC.4	PAC.3	PAC.2	PAC.1	PAC.0	W	11111111

PAC (PORTA control register):

PAC.[7~0]	Setting PA as Input /Output (all bit programmable)
1	Set PORTA.x as input buffer (default)
0	set PORTA.x as output buffer

PA (PORTA data register):The data output or input buffers.

PORTB control register (bi-directional I/O):

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F23	**PB**	PB.7	PB.6	PB.5	PB.4	PB.3	PB.2	PB.1	PB.0	R/W	11111111
$1F24	**PBC**	-	-	-	-	-	-	PBC.H	PBC.L	W	------11

PBC (PORTB control register):

PBC.H	PBC.L	Setting PB high nibble and low nibble as Input /Output
×	1	Set PB's low nibble as input ports (0: low nibble as output ports)
1	×	Set PB's high nibble as input ports (0: high nibble as output ports)

PB (PORTB data register): The data output or input buffers

PC(PORTC data register): (Output only)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F25	**PC**	PC.7	PC.6	PC.5	PC.4	PC.3	PC.2	PC.1	PC.0	W	00000000

PORTD control register (bi-directional I/O):

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F26	**PD**	PD.7	PD.6	PD.5	PD.4	PD.3	PD.2	PD.1	PD.0	R/W	11111111
$1F27	**PDC**	PDC.7	PDC.6	PDC.5	PDC.4	PDC.3	PDC.2	PDC.1	PDC.0	W	11111111
$1F28	**PDS**	PDS.7	PDS.6	PDS.5	PDS.4	PDS.3	PDS.2	PDS.1	PDS.0	W	11111111

PDC (PORTD control register):

PDC.[7~0]	Setting PD as Input /Output (all bit programmable)
1	Set PORTD.x as input buffer (default)
0	set PORTD.x as output buffer

PD (PORTD data register): The data output or input buffers.

PDS (PORTD special register): Special function On/Off.

PDS.0~7	Setting PD.0~7 as output push-pull or open drain (all bit programmable)
1	Set PORTD.x as push-pull output (default)
0	Set PORTD.x as Open-drain output

UART (Universal Asynchonous Receiver-Transmitter)

There is an UART (with RXD & TXD pins) embeded in SH58201, which can be used as serial interface. RXD pin shared with PORTD.2 is used as serial input , as well as TXD pin which is shared with PORTD.1 as serial output. The UART function will be available if the bit6 (UART) of the **SPECIAL2** register ($1F05) is set to "1".

Serial Transmitting output data buffer register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F50	**STBUF**	TD.7	TD.6	TD.5	TD.4	TD.3	TD.2	TD.1	TD.0	R/W	11111111

Serial Receiving input data buffer register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F51	**SRBUF**	RD.7	RD.6	RD.5	RD.4	RD.3	RD.2	RD.1	RD.0	R	11111111

Serial mode control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F52	**SCON**	SM	-	-	REN	TB8	RB8	-	-	R/W	0—000--

SM	Function	Baud rate
0	8_bit UART	Controlled by Timer0/1
1	9_bit UART	Controlled by Timer0/1

Receiving enable control bit

REN	Description	Note
0	Receive disable	default
1	Receive enable	

(A). TB8 is bit8 in transmitting function. When SM=1, TB8 is the bit9 of transmitting data. In this case, according most communiction protocal, it can usually be used as Odd/Even check. The TB8 can be set or reset by writing "1" or "0".

(B). RB8 is bit8 in receiving function. When SM=1, RB8 is the bit9 of received data. In this case, according most communiction protocal, it can usually be used as Odd/Even check.

NMI enable register:

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F10	NMI_IE	NMISR1	-	-	-	-	NMISR	NMIST	NMIPA	R/W	0----000

(A). The register is used to **decide** which NMI source will be activated.(Non-Maskable Interrupt).

(B). 0: Disable (default)
1: Enable (If the bit is set to "1", that means the relevant event can interrupt CPU.)

NMISR	NMIST	Description
-	1	Enable serial data transmitting interrupt
1	-	Enable serial data receiving interrupt

NMI request flag register:

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F11	**NMI_IF**	NMISR1	-	-	-	-	NMISRI	NMISTI	NMIPA	R	0-----00

(A). The register is used to **record** NMI request status. For Example, if the NMI source (SR1) counts overflow from FFFFh to 0000h, the bit7 of this register will be set. In this time, if the coordinate NMI_IE is set to "1", the NMI will be triggered, and the program counter will point to the NMI vector. (6502 NMI vector is located at the $FFFA~$FFFB)

(B). When the operation of reading this register, the status of this register will be cleared right now.

Transmitting interrupt flag

NMISTI	Description	Note
0	Flag cleared	Program reading
1	Interrupt active	Caused by H/W

Receiving interrupt flag

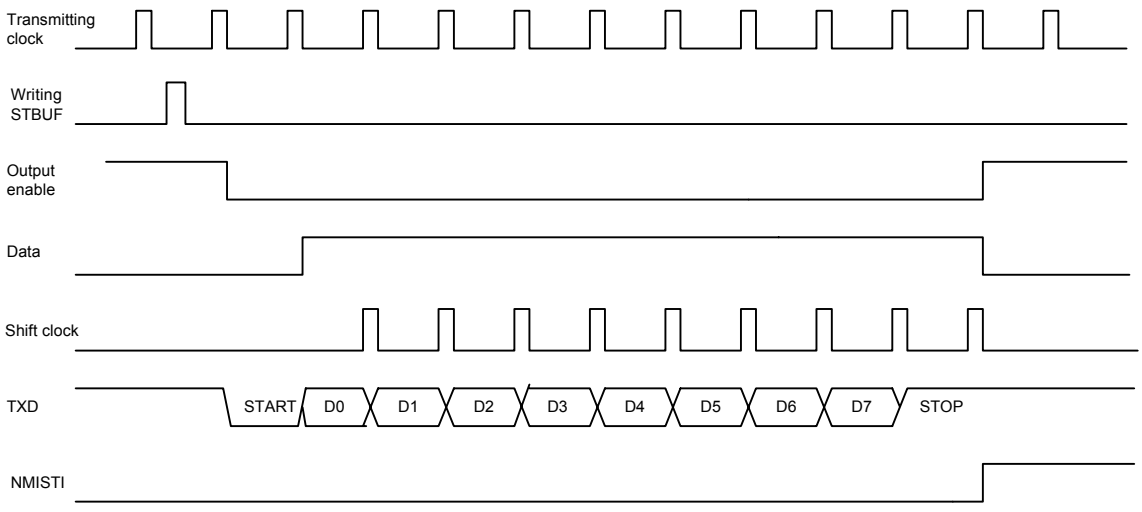
NMISRI	Description	Note
0	Flag cleared	Program reading
1	Interrupt active	Caused by H/W

8_bit UART Mode

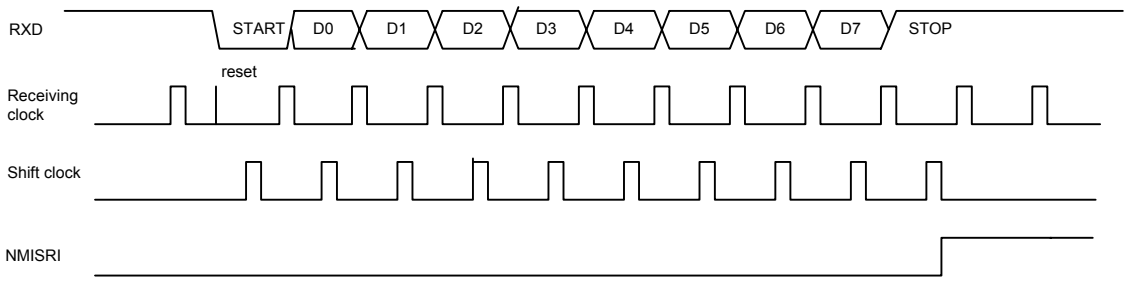
If SM is set to “0”, the UART is working under 8_bit mode. Actually, in this mode, the transferring format is 10 bits. That is to say, 1bit as START bit (“0”), 8 bits as DATA (LSB first), and 1bit as STOP bit (“1”). The system operation is transmitting from the TXD pin as well as receiving through the RXD pin. Transferring baud rate is selectable, and can be controlled by proper setting of Timer0 or Timer1. Meanwhile, the operations of transmitting and receiving can be used with different baud rates controlled by Timer0 or Timer1, respectively. (For more information, please refer to Timer and the relevant scetions.)

Transmtiing executing starts with the operation of writing the STBUF register. The output data shall be delivered to the Transmit_Shift_Register, as well as “1” is sent bit3 (TB8) of the SCON register. When the content of TB8 has been shifted out, the Transmit_Control_Unit sets the NMISTI to “1” and creates the NMI (NMIST) request immediately if the NMIST has been set to “1”.

Receiving executing starts with the having detected the falling edge at the RXD pin under the condition which the system has been set REN=1 and NMISRI=0. If the available falling edge triggering is achieved, and the first input bit is “0”, the input signal will be delivered into the Receive_Shift_Register, and the following data will be accepted consequently. Otherwise, the first bit is not a START bit, then the receiving operation should be abandoned, and reset the whole circuits of the receiving block simultaneously. When the last bit (STOP bit) has been shifted in, the 8bits data shall be delivered to the SRBUF register and the STOP bit to bit2 (RB8) of the SCON register. If the NMISRI has been cleared by programming reading before the last bit shfitting occurs, and the STOP bit is “1”, the Receive_Control_Unit will successfully set the NMISRI to ”1” and creates the NMI (NMISR) request immediately if the NMISR has been set to “1”. Otherwise, the total input data process will be lost finally.



Transmitting Timing



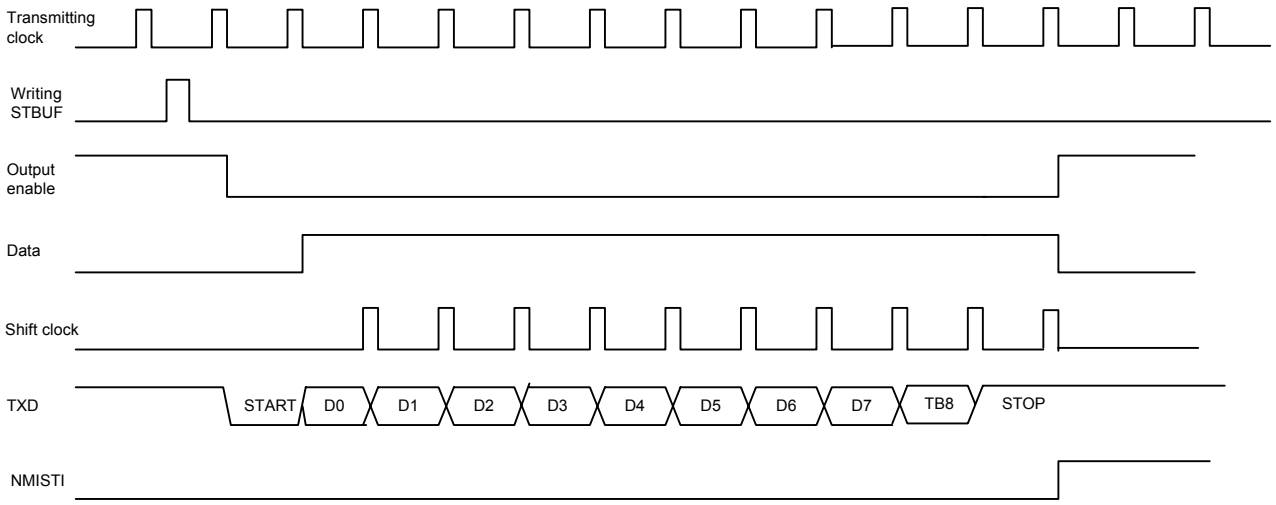
Receiving Timing

9_bit UART Mode

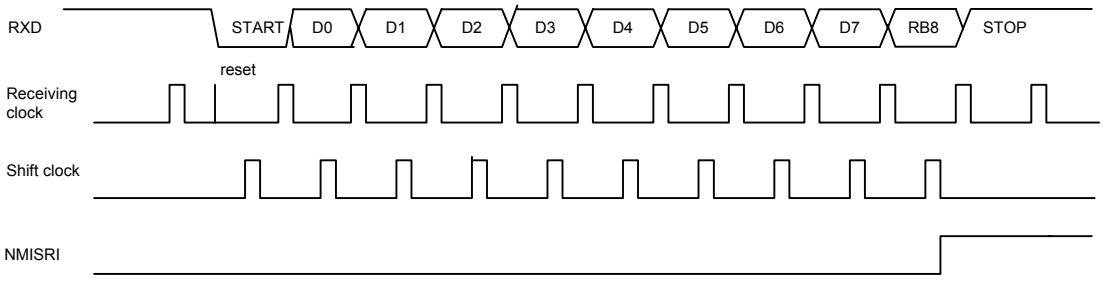
If SM is set to “1”, the UART is working under 9_bit mode. Actually, in this mode, the transferring format is 11 bits. That is to say, 1bit as START bit (“0”), 8 bits as DATA (LSB first), 1 programmable bit (or the ninth bit of data), and 1bit as STOP bit (“1”). The system operation is transmitting from the TXD pin as well as receiving through the RXD pin. Transferring baud rate is selectable, and can be controlled by proper setting of Timer0 or Timer1. Meanwhile, the operations of transmitting and receiving can be used with different baud rates controlled by Timer0 or Timer1, individually. (For more information, please refer to Timer and the relevant scetions.)

Transmtiing executing starts with the operation of writing the STBUF register. The output data shall be delivered to the Transmit_Shift_Register, as well as bit3 (TB8) of the SCON register is sent to the ninth bit of the Transmit_Shift_Register. During the first shifting phase, a ”1” will be feeded into the ninth bit of the Transmit_Shift_Register by the control_unit as a STOP bit. When the STOP bit has been shifted out, the Transmit_Control_Unit sets the NMISTI to “1” and creates the NMI (NMIST) request immediately if the NMIST has been set to “1”.

Receiving executing starts with the having detected the falling edge at the RXD pin under the condition which the system has been set REN=1 and NMISRI=0. If the available falling edge triggering is achieved, and the first input bit is “0”, the input signal will be delivered into the Receive_Shift_Register, and the following data will be accepted consequently. Otherwise, the first bit is not a START bit, then the receiving operation should be abandoned, and reset the whole circuits of the receiving block simultaneously. When the tenth bit (as the ninth data bit) has been shifted in, the 8bits data shall be delivered to the SRBUF register and the ninth data bit to bit2 (RB8) of the SCON register. If the NMISRI has been cleared by programming reading before the tenth bit shfitting occurs, the Receive_Control_Unit will successfully set the NMISRI to ”1” and creates the NMI (NMISR) request immediately if the NMISR has been set to “1”. Otherwise, the total input data process will be lost finally. Be careful, in this receiving mode, the content of bit2 (RB8) of the SCON register is the ninth bit of the receiving data, not the STOP bit as before. The value of the STOP bit does not have any relationship with the SRBUF, RB8, and even NMISRI.



TransmittingTiming



ReceivingTiming

Port Interrupt (PORTB, is the same)

The PORTA (B) can be used as port interrupt sources. Since PORTA (B) is bi-directional I/O, thus,

(A). Only the input port status could generate interrupt.
(B). Any input pin for PORTA (B) transitions from high level to low level would generate an interrupt request. No any other falling edge transitions of input pin can generate interrupt request again until all of the pins return to high level.

Example:

Step1: choose PORTA to be input port or output port (PAC.7~PAC.0)
Step2: read data (A be input port) or write data (A be output port) (PA.7~PA.0)
(A)

```
LDA     #0
STA     rPAC    choose Bit0~7 be output pin
LDA     #$0D
STA     rPA     send #$0d to PORTA
```

(B).

MAIN PROG.

```
……
LDA     #$FF
STA     PAC
LDA     #$08
STA     IRQ_IE
        ……
```

ISR

```
LDA     IRQ_IF
STA     wSAVE_IRQFLAG
```

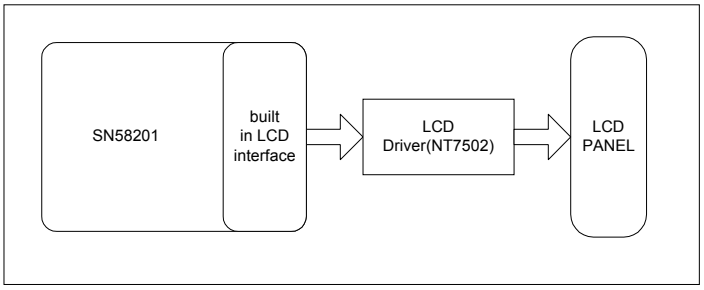
This program can trigger PORTA interrupt
Setting PORTA as input port and enable IRQPA.
When PORTA detects falling edge
The PC Will jump to **ISR**

External Interrupt

There is an external interupt function embeded in SH58201. It will be available if it is enabled by properly setting in special mode. (Please refer to the relevant section.) The External interrupt input pin shared with PORTD.0 will be triggered by falling edge.

LCD Interface

The SH58201 provides 13 pins for external LCD interface. The built-in LCD interface of the SH58201 is applicable for 8 bit parallel I/P structure. Ex: NT7502, NT3881/NT3882, NT3890/NT3891, NT53101, KS107/KS108, SED15xx or HDxx … and so on. The application blocks are shown as following:



LCD Application

Control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F29	**LCS**	-	-	-	-	-	CSH/L	SEL1	SEL0	W	-----011
$1F2A	**LRS**	-	-	-	-	-	-	-	RS	W	-------0
$1F2B	**RD_DATA**	7	6	5	4	3	2	1	0	R	11111111
$1F2C	**LCD0**	7	6	5	4	3	2	1	0	R/W	00000000
$1F2D	**LCD1**	7	6	5	4	3	2	1	0	R/W	00000000

LCS:
(1). SH58201 supplies the LCD “enable” signal timing for external LCD driver or module. It can be used to select the different width of the “enable” and “chip select” signals by writing bit1/0 of LCS register. Shown as following:

SEL1	SEL0	Clock division
0	0	SH58201 System clock /2
0	1	SH58201 System clock /4
1	0	SH58201 System clock /8
1	1	SH58201 System clock /16

(2). Bit2 of the LCS register is supplied for controlling the active level of chip selecting signal.

CSH/L	Chip Select Trigger level
0	Active Low (Default)
1	Active High

LRS:
This register is used to identify the data type on the data bus (LDD0~7). That is, when the LRS register is set to “1”, information delivered on the data bus at LCD interface are genuine data. In the contrast, information is instructions for controlling the LCD driver.

RS	Data mode
0	Instruction mode(Default)
1	Data mode

RD_DATA:
In the reading data mode, this register is used to store the input transferring data, that is, when the read command is set, the data is stored to the RD_DATA buffer.

Example:
If the reading data from the LCD driver (here assume driver0 is selected) is desired, the program flows should be as follow:
(a). execute the read command
(b). load data from the RD_DATA to LCD0(if driver 0 is selected)

```
LDA     $1F2C       ; load LCD0 data into LCD buffers.
LDA     $1F2B       ; load LCD buffer data into $1F2B register (RD_DATA)
STA     Variable    ; store the contents of RD_DATA register to a variable that is defined on zero page.
```

LCD0:
In the writing data mode, this register is used to store the data for writing out. LCD0 is used for the driver0. The SH58201 supplies maximum up to 2 LCD drivers. The data access is rely on the individual LCD drivers. (That is: LCD1 is used for the driver1)

LCD1:
In the writing data mode, this register is used to store the data for writing out. LCD1 is used for the driver1.

Interface pin

LDD0~7:
The data bus between SH58201 with general LCD driver.

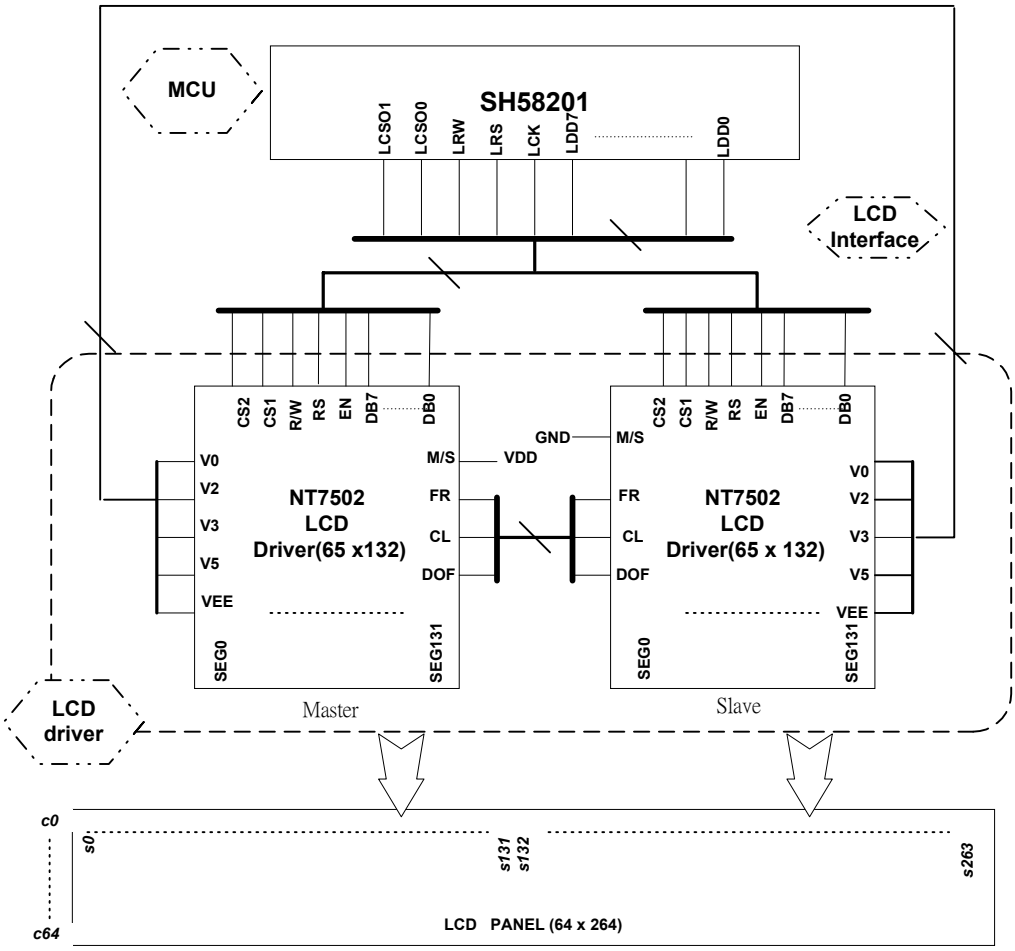
LRS:
The register defines the bus information as instructions/data between SH58201 with general LCD driver.

LCSO0~LCSO1:
Chip selection signals for external LCD driver.

LRW:
Read /Write controlling signal for the bus operation between the SH58201 with general LCD driver. (1: Read; 0: Write)

LEN:
Read/Write operating enable signal. (High active)

The application circuit:



Carrier synthesizer

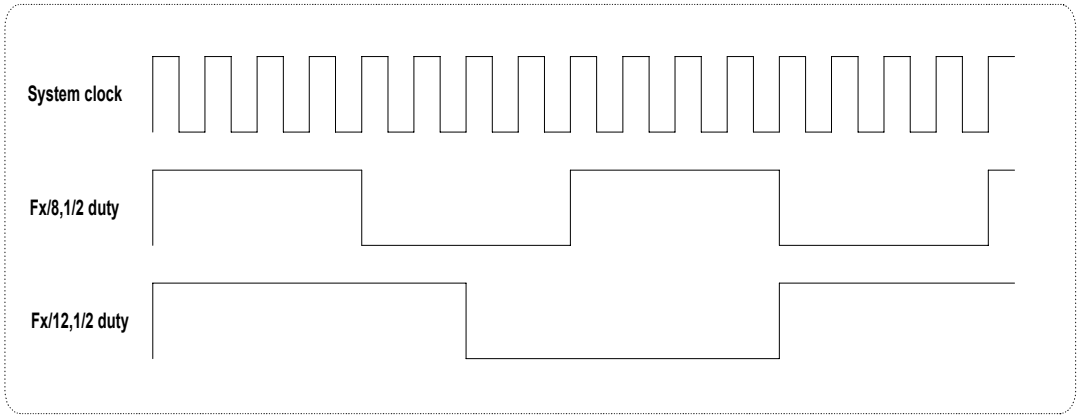
This chip builds in a carrier synthesizer for infrared or RF remote control circuit. It is available after the bit4 (REMO) of SPECIAL2 ($1F05) register have been set to “1”.

Remote control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F1C	RF_CTRL	enable	-	-	-	-	-	-	RFQ.0	W	0-------0
$1F1D	RF_OUTPUT	-	-	-	-	-	-	-	DATA	R/W	-------0

RF_FREQ (carrier frequency control)

RFQ.0	Carrier frequency
0	Frequency=56K,1/2 duty (default)
1	Frequency=38K,1/2 duty
enable	**Enable output pin data control**
0	Disable data output (default)
1	Enable data output
DATA	**Carrier data output control**
0	Disable carrier (default)
1	Carrier output



carrier waveform

Sound Control

Tone generator 1

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F30	**TG1_L**	TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0	R/W	00000000
$1F31	**TG1_H**	TG15	TG14	TG13	TG12	TG11	TG10	TG9	TG8	R/W	00000000
$1F32	**TG1_CTL**	enable	loop	-	-	-	-	CS1	CS0	W	00----10

A 16-bit programmable tone generator is built in SH58201. It generates specific frequency of tone with square wave. It can be used as a 16-bit down-count counter too. The meanings and control ways for each register of tone generator is similar to playback sample rate (SR1). The difference between SR1 and tone generator is that writing the SR1_H will cause the [SR1_H, SR!_L] to be loaded into the counter, but doing with TG1_H will not cause the [TG1_H, TG1_L] to be loaded into the counter. Writing “1xxx xxxx” into TG1_CTL will cause the [TG1_H, TG1_L] to be loaded into the counter and start counting. (❇ Writing “0xxx xxxx” into TG1_CTL will cause the [TG1_H, TG1_L] to be loaded into the counter.) It is important that the SR1 is used to play a voice as well as the tone generator for playing a tone. The SR1 cannot generate tone. Please note that the frequency of a specific tone is half of the counter overflow frequency. The illustration is described below:

Frequency = source_clock / ([TG1_H,TG1_L]+1)

(If clock source= 4,000,000Hz)

TG1_H	TG1_L	counter frequency	tone frequency	relative scale of tone
3BH	B8H	261.609	130.804	C3 (130.813)
38H	5EH	277.181	138.591	C3# (138.591)
35H	34H	293.643	146.821	D3 (146.832)
:	:	:	:	:
0EH	EDH	1046.572	523.286	C5 (523.251)
:	:	:	:	:
03H	BBH	4184.100	2092.050	C7 (2093.005)

The complete scale / counter setting table is listed in Appendix A.

Tone generator1 control register

CS1	CS0	Clock source
0	0	31,250Hz
0	1	External clock (normally 32.768KHz)
1	0	CPU clock (typical 4MHz) (default)
1	1	Reserved

enable	loop	Description
×	0	Counter working in one-shot mode (default)
×	1	Counter working in loop mode
0	×	Counter is disabled (default)
1	×	Counter is enabled

Tone generator 2

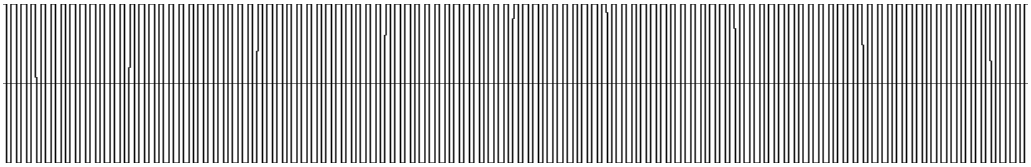
ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F33	**TG2_L**	TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0	R/W	00000000
$1F34	**TG2_H**	TG15	TG14	TG13	TG12	TG11	TG10	TG9	TG8	R/W	00000000
$1F35	**TG2_CTL**	enable	loop	-	-	-	-	CS1	CS0	W	00----10

Refer to tone generator 1 for more information.

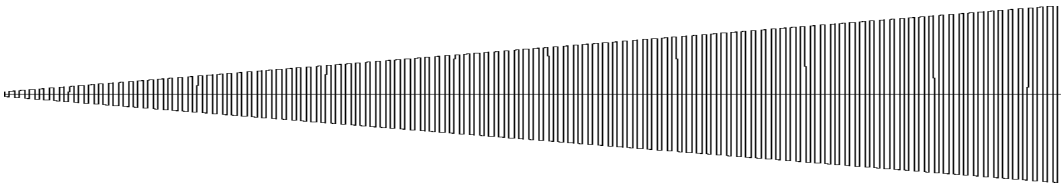
Tone 1 envelope control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F36	TG1_ENV	-	E6	E5	E4	E3	E2	E1	E0	R/W	-0000000

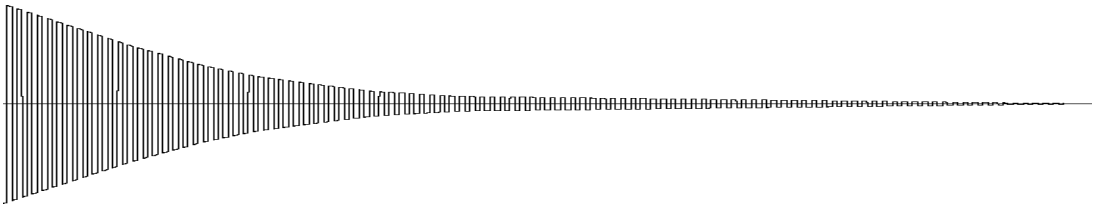
Tone 1 envelope is a 8-bit register designed to control the output level of tone 1. When it is set to be 0, the output level is lowest – no any tone output. After stopping playing tone 1, this register has to be set to 0. Changing the envelope of a tone can create various timbre of music. The waveform of normal square wave is like:



For SH58201, program can create such waveform as below through the envelope control register.
(Envelope A)



(Envelope B)



The same tone with envelope A and B sounds very different. The tone with envelope A sounds like harmonica and envelope B like piano. The phase of tone 1 will be reset when this register is read.

Tone 2 envelope control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F37	TG2_ENV	-	E6	E5	E4	E3	E2	E1	E0	R/W	-0000000

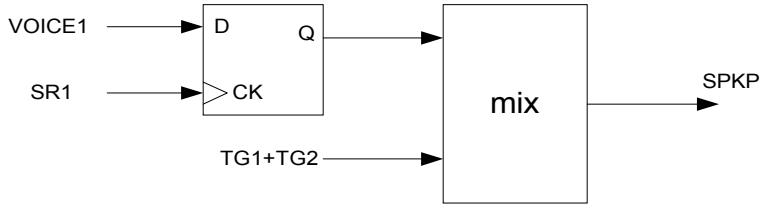
Same as tone 1 envelope, but this register controls the envelope of tone generator 2.

Voice Synthesizer

VOICE1

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F3F	VOICE1	D7	D6	D5	D4	D3	D2	D1	D0	W	00000000

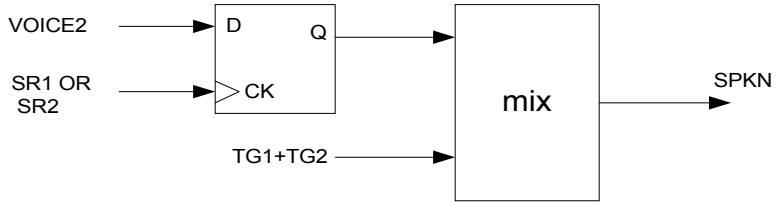
If the voice output method is set to be STEREO PWM, then VOICE1 is mixed with TG1+TG2.



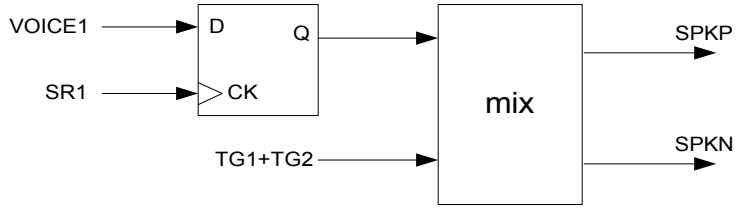
VOICE2

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F41	VOICE2	D7	D6	D5	D4	D3	D2	D1	D0	W	00000000

If the voice output method is set to be STEREO PWM, then VOICE2 is mixed with TG1+TG2.



If the voice output method is set to be MONO PWM, then only VOICE1 is used.



MONO PWM output structure:

SPKP(+) ---------- 0 ~ +127

SPKN(-) ---------- -1 ~ -128

Carrier = 2^{15} = 32KHz, CPU = 4MHz = 2^{22} = $2^{15} \bullet 2^{7}$

STEREO PWM output structure:

VOICE1 or VOICE2 symbol system	The value of VOICE1 or VOICE2	Duty
FF (max.)	+127	100% duty (255/256)
:	:	:
80(middle)	0	50% duty (128/256)
:	:	:
00(-max.)	-128	0% duty (0/256)

PWM mode control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F43	**PWM_CTL**	SR2_E	-	-	-	-	-	-	ST_ON	R/W	0------1

SR2_E	Description
0	Voice2 sample rate controlled by SR1 (default)
1	Voice2 sample rate controlled by SR2

ST_ON	Description
0	Voice output in MONO mode
1	Voice output in STEREO mode (default)

Voice mode control register

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F44	**SD_CTL**	PWM/DAC	-	-	-	DAC2EN	PWM2EN	DAC1EN	PWM1EN	R/W	1---0000

PWM/DAC	Description
0	DAC Output
1	PWM Output (default)

DAC2EN	DAC1EN	Description
0	×	DAC channel 2 disable (default)
1	×	DAC channel 2 enable
×	0	DAC channel 1 disable (default)
×	1	DAC channel 1 enable

PWM2EN	PWM1EN	Description
0	×	PWM channel 2 disable (default)
1	×	PWM channel 2 enable
×	0	PWM channel 1 disable (default)
×	1	PWM channel 1 enable

Sample rate clock (SR1)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F39	**SR1_COUNT(L)**	SR1.7	SR1.6	SR1.5	SR1.4	SR1.3	SR1.2	SR1.1	SR1.0	R/W	00000000
$1F3A	**SR1_COUNT(H)**	SR1.15	SR1.14	SR1.13	SR1.12	SR1.11	SR1.10	SR1.9	SR1.8	R/W	00000000
$1F3B	**SR1_CTRL**	enable	loop	-	-	-	-	CS1	CS0	W	00------10

SR1_COUNT(L)/(H) (sample rate counter register):

(1). This chip offers a 16 bit down-counter sampling rate clock generated from system clock.

(2). The counter value will be reloaded to the counter when writing data into the SR1_COUNT(H). Then, this clock will start counting. That is to say, if some data was written into the SR1_COUNT(L) and nothing was written into the SR1_COUNT(H), this counter will be still counting the original value until it's overflow. When the overflow is occurring, the new pre-load value is immediately loaded to the counter.

(3). Sample rate clock:

The frequency of sample rate= system clock /([SR1_COUNT(H),SR1_COUNT(L)]+1)

Example:

Assume the CPU cock is 2,000,000Hz

SR1_COUNT(H)	SR1_COUNT(L)	Sample Rate Frequency
00H	00H	invalid
00H	01H	1,000,000
00H	02H	666,666.67
:	:	:
FFH	FFH	30.52

SR1_CTRL (sample rate control register):

CS1	CS0	Clock source
0	0	31,250Hz
0	1	External clock (normally 32.768KHz)
1	0	CPU clock (typical 4MHz)
1	1	CPU clock/2

enable	loop	Description
×	0	Counter working in one-shot mode (default)
×	1	Counter working in loop mode
0	×	Counter is disabled (default)
1	×	Counter is enabled

Sample rate clock (SR2)

ADDRESS	REGISTER	7	6	5	4	3	2	1	0	R/W	Default
$1F3C	**SR2_COUNT(L)**	SR2.7	SR2.6	SR2.5	SR2.4	SR2.3	SR2.2	SR2.1	SR2.0	R/W	00000000
$1F3D	**SR2_COUNT(H)**	SR2.15	SR2.14	SR2.13	SR2.12	SR2.11	SR2.10	SR2.9	SR2.8	R/W	00000000
$1F3E	**SR2_CTRL**	enable	loop	-	-	-	-	CS1	CS0	W	00------10

Refer to sample rate clock(SR1) for more information.

Programming Notice

The status after different reset condition is listed below:

	Power on reset	Wakup from power down mode	CPU RSTB pin reset
SRAM data	unknown	unchanged	unknown
CPU register	unknown	unknown	unknown
Device register	default value	unchanged	default value

Absolute Maximum Rating

DC Supply Voltage……-0.3V to +5V

Input / Output Voltage……GND-0.3V to V_{DD}+03.V

Operating Ambient Temperature…-10^{0}C to +60^{0}C

Storage Temperature……..-55^{0}C to +125^{0}C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (1)

(GND = 0V, Temp = 25°C, F_{OSC} = 8MHz RC, System clock=4MHz, V_{DD} =3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	2.2	3.0	3.5	V	
V_{IH1}	Input High Voltage	0.7*V_{DD}		V_{DD}+0.3	V	
V_{IL1}	Input Low Voltage	GND-0.3		0.3*V_{DD}	V	
V_{IH2}	Input High Voltage	0.8*V_{DD}		V_{DD}+0.3	V	PortA,B, Reset, Exint, RXD, Test
V_{IL2}	Input Low Voltage	GND-0.3		0.2*V_{DD}	V	PortA,B, Reset, Exint, RXD, Test
V_{LPD}	Low Power Detect Voltage	2.3	2.5	2.7	V	
I_{OP}	Operating Current		4.8		mA	All output pins unload
I_{STB1}	Standby Current1		1	2	μA	CPU off, 32K off, No load, LPD off
I_{STB2}	Standby Current2		3	6	μA	CPU off, 32K On, No load, LPD off
I_{OH}	Port driving current	0.5	1.5		mA	V_{OH} = 2.7V PortA,B,C,D
I_{OL}	Port sink current	1	3		mA	V_{OL} = 0.4V PortA,B,C,D
R_P	Pull-up resister		200		KΩ	
R_{RST}	Reset pull-up resister		100		KΩ	

DC Electrical Characteristics (2)

(GND = 0V, Temp = 25°C, F_{OSC} = 4MHz RC, System clock=2MHz, V_{DD} =3V)

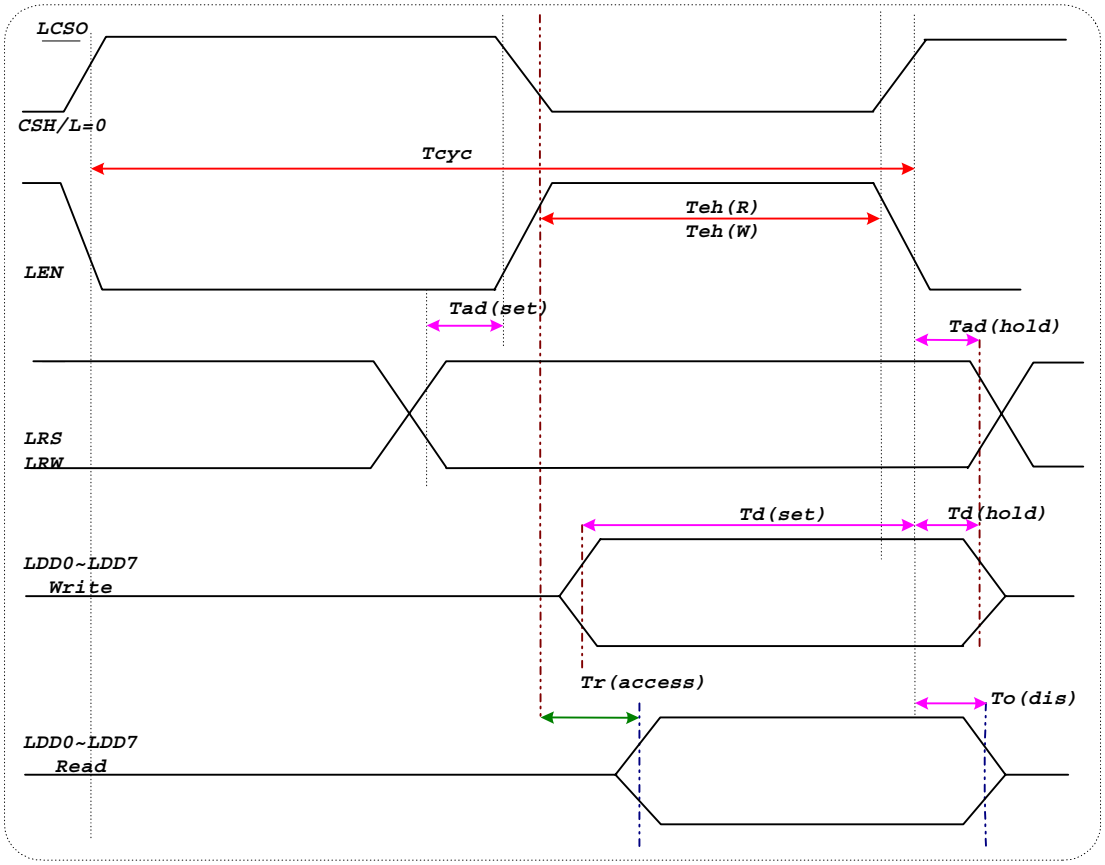
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	2.2	3.0	3.5	V	
V_{IH1}	Input High Voltage	0.7*V_{DD}		V_{DD}+0.3	V	
V_{IL1}	Input Low Voltage	GND-0.3		0.3*V_{DD}	V	
V_{IH2}	Input High Voltage	0.8*V_{DD}		V_{DD}+0.3	V	PortA,B, Reset, Exint, RXD, Test
V_{IL2}	Input Low Voltage	GND-0.3		0.2*V_{DD}	V	PortA,B, Reset, Exint, RXD, Test
V_{LPD}	Low Power Detect Voltage	2.3	2.5	2.7	V	
I_{OP}	Operating Current		2.4		mA	All output pins unload
I_{STB1}	Standby Current1		1	2	μA	CPU off, 32K off, No load, LPD off
I_{STB2}	Standby Current2		3	6	μA	CPU off, 32K On, No load, LPD off
I_{OH}	Port driving current	0.5	1.5		mA	V_{OH} = 2.7V PortA,B,C,D
I_{OL}	Port sink current	1	3		mA	V_{OL} = 0.4V PortA,B,C,D

AC Electrical Characteristics

(GND = 0V, Temp = 25°C, F_{OSC} = 8MHz)

Symbol		Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{PWM}	I_{OH}	PWM output driving current		12		mA	V_{DD} =3V, V_{OH} = 2.7V
	I_{OL}			25			V_{DD} =3V, V_{OL} = 0.4V
$\Delta F_{RC}/F_{RC}$		RC Frequency Stability			20	%	[F(3.0V)-F(2.5V)] / F(3.0V), F_{OSC}=16M
				8	10		[F(3.0V)-F(2.5V)] / F(3.0V), F_{OSC}=8M
				5	7		[F(3.0V)-F(2.5V)] / F(3.0V), F_{OSC}=4M
F_{CPU}		CPU working frequency	2	4	8	MHz	V_{DD}=3.0V F_{OSC} = 16MHz

LCD Timing Waveform



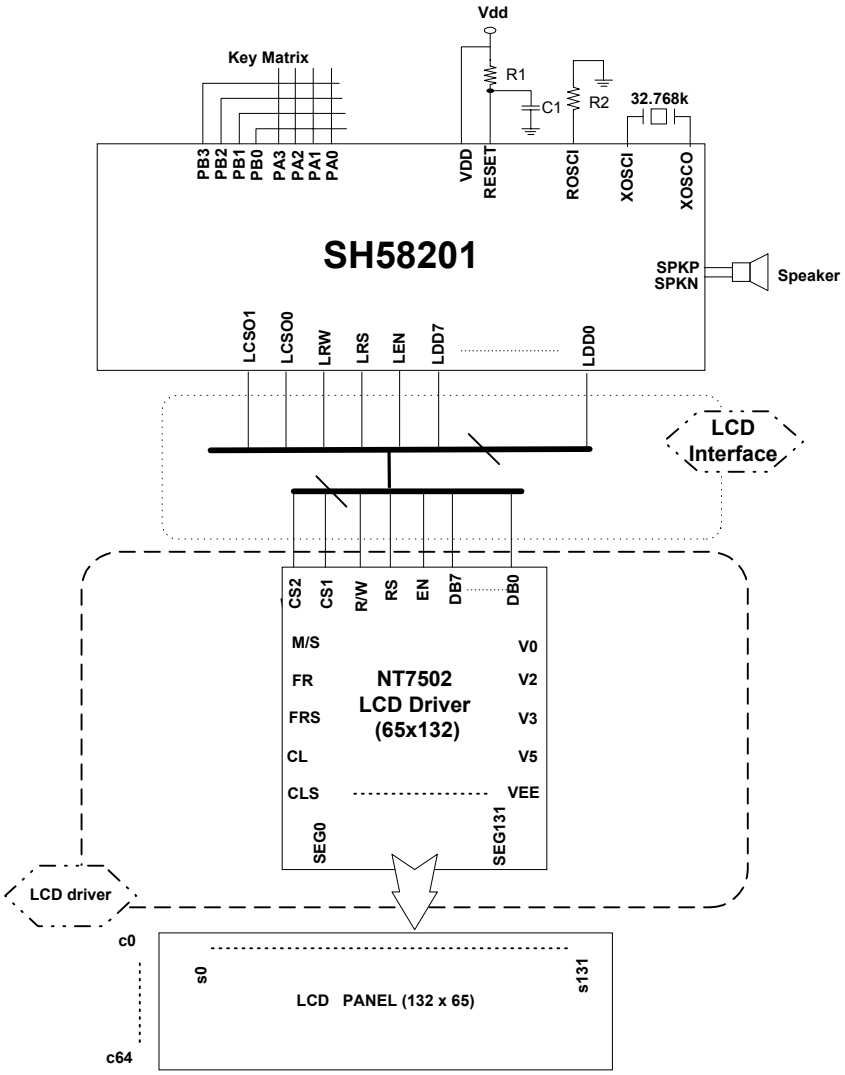
LCD Read /Write Timming

(GND = 0V, Temp = 25°C, V_{DD} =3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
TCYC	LCD driver system cycle time	300			ns	
Tad (set)	Address setup time	0			ns	
Tad (hold)	Address hold time	0			ns	
Td (set)	Data setup time	40			ns	
Td (hold)	Data hold time	15			ns	
Teh (R)	Enabe pulse width (Read)	120			ns	
Teh (W)	Enabe pulse width (Write)	60			ns	
Tr (access)	Read access time			140	ns	CL=100pF
To (dis)	Read Data output disable time	10		100	ns	CL=100pF

Application Circuit (for Reference Only) (1)

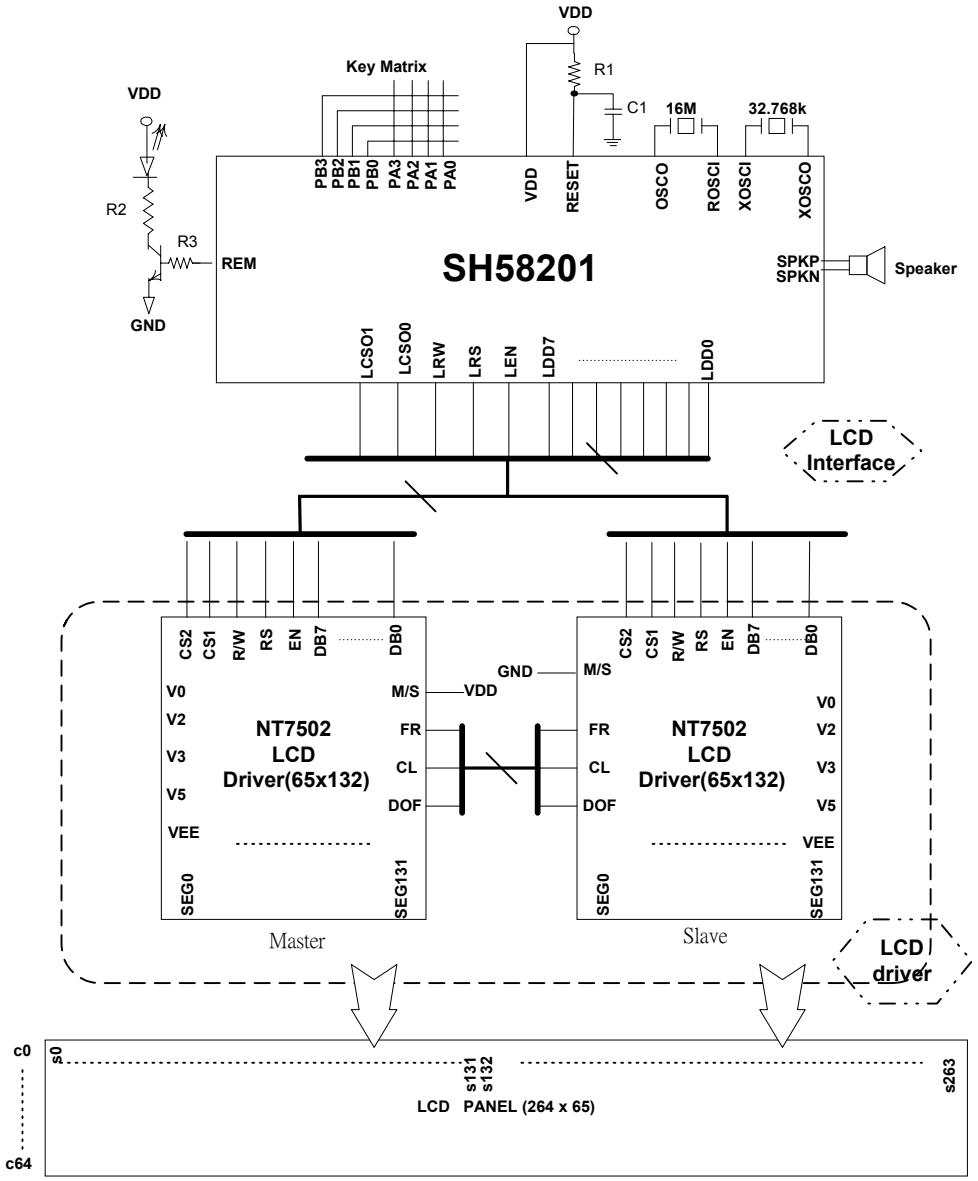
(Without IR, used in the RC mode, LCD interface with the LCD driver)



Application circuit (1)

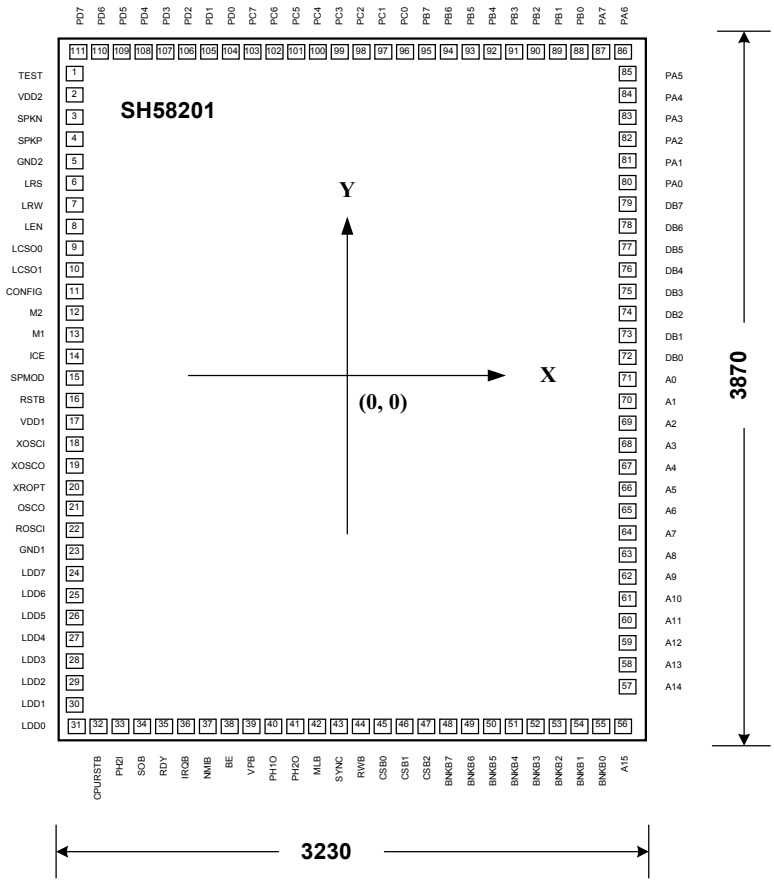
Application Circuit (for Reference Only)(2)

(used in the X'tal mode; LCD interface with the multi-chip LCD drivers)



Application circuit (2)

Bonding Diagram



* Substrate connects to GND

Pad Location

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	TEST	-1544	1732.5	11	CONFIG	-1544	517.5
2	VDD2	-1544	1602.5	12	M2	-1544	402.5
3	SPKN	-1544	1472.5	13	M1	-1544	287.5
4	SPKP	-1544	1342.5	14	ICE	-1544	172.5
5	GND2	-1544	1222.5	15	SPMOD	-1544	57.5
6	LRS	-1544	1102.5	16	RSTB	-1544	-57.5
7	LRW	-1544	982.5	17	VDD1	-1544	-172.5
8	LEN	-1544	862.5	18	XOSCI	-1544	-287.5
9	LCSO0	-1544	747.5	19	XOSCO	-1544	-402.5
10	LCSO1	-1544	632.5	20	XROPT	-1544	-517.5

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
21	OSCO	-1544	-632.5	67	A4	1544	-447.5
22	ROSCI	-1544	-747.5	68	A3	1544	-327.5
23	GND1	-1544	-862.5	69	A2	1544	-207.5
24	LDD7	-1544	-982.5	70	A1	1544	-87.5
25	LDD6	-1544	-1102.5	71	A0	1544	32.5
26	LDD5	-1544	-1222.5	72	DB0	1544	152.5
27	LDD4	-1544	-1342.5	73	DB1	1544	272.5
28	LDD3	-1544	-1472.5	74	DB2	1544	392.5
29	LDD2	-1544	-1602.5	75	DB3	1544	512.5
30	LDD1	-1544	-1732.5	76	DB4	1544	632.5
31	LDD0	-1530	-1862.5	77	DB5	1544	752.5
32	CPURSTB	-1400	-1862.5	78	DB6	1544	872.5
33	PH2I	-1270	-1862.5	79	DB7	1544	992.5
34	SOB	-1140	-1862.5	80	PA0	1544	1112.5
35	RDY	-1020	-1862.5	81	PA1	1544	1232.5
36	IRQB	-900	-1862.5	82	PA2	1544	1352.5
37	NMIB	-780	-1862.5	83	PA3	1544	1472.5
38	BE	-660	-1862.5	84	PA4	1544	1602.5
39	VPB	-540	-1862.5	85	PA5	1544	1732.5
40	PH1O	-420	-1862.5	86	PA6	1530	1862.5
41	PH2O	-300	-1862.5	87	PA7	1400	1862.5
42	MLB	-180	-1862.5	88	PB0	1270	1862.5
43	SYNC	-60	-1862.5	89	PB1	1140	1862.5
44	RWB	60	-1862.5	90	PB2	1020	1862.5
45	CSB0	180	-1862.5	91	PB3	900	1862.5
46	CSB1	300	-1862.5	92	PB4	780	1862.5
47	CSB2	420	-1862.5	93	PB5	660	1862.5
48	BNKB7	540	-1862.5	94	PB6	540	1862.5
49	BNKB6	660	-1862.5	95	PB7	420	1862.5
50	BNKB5	780	-1862.5	96	PC0	300	1862.5
51	BNKB4	900	-1862.5	97	PC1	180	1862.5
52	BNKB3	1020	-1862.5	98	PC2	60	1862.5
53	BNKB2	1140	-1862.5	99	PC3	-60	1862.5
54	BNKB1	1270	-1862.5	100	PC4	-180	1862.5
55	BNKB0	1400	-1862.5	101	PC5	-300	1862.5
56	A15	1530	-1862.5	102	PC6	-420	1862.5
57	A14	1544	-1667.5	103	PC7	-540	1862.5
58	A13	1544	-1537.5	104	PD0	-660	1862.5
59	A12	1544	-1407.5	105	PD1	-780	1862.5
60	A11	1544	-1287.5	106	PD2	-900	1862.5
61	A10	1544	-1167.5	107	PD3	-1020	1862.5
62	A9	1544	-1047.5	108	PD4	-1140	1862.5
63	A8	1544	-927.5	109	PD5	-1270	1862.5
64	A7	1544	-807.5	110	PD6	-1400	1862.5
65	A6	1544	-687.5	111	PD7	-1530	1862.5
66	A5	1544	-567.5				

APPENDIX A (tone base frequency)

TG?_H	TG?_L	Tone Freq	Scale
77H	71H	65.407	C2 (65.406)
70H	BDH	69.295	C2# (69.296)
6AH	69H	73.416	D2 (73.416)
64H	70H	77.782	D2# (77.782)
5EH	CDH	82.406	E2 (82.407)
59H	7BH	87.306	F2 (87.307)
54H	75H	92.498	F2# (92.499)
4FH	B7H	98.000	G2 (97.999)
4BH	3DH	103.831	G2# (103.830)
47H	05H	109.999	A2 (110.000)
43H	08H	116.543	A2# (116.541)
3FH	45H	123.472	B2 (123.471)

TG?_H	TG?_L	Tone Freq	Scale
3BH	B8H	130.813	C3 (130.813)
38H	5EH	138.591	C3# (138.591)
35H	34H	146.832	D3 (146.832)
32H	38H	155.557	D3# (155.563)
2FH	66H	164.813	E3 (164.814)
2CH	BDH	174.611	F3 (174.614)
2AH	3AH	184.997	F3# (185.000)
27H	DBH	196.002	G3 (196.000)
25H	9EH	207.662	G3# (207.652)
23H	82H	219.998	A3 (220.000)
21H	84H	233.073	A3# (233.082)
1FH	A2H	246.944	B3 (246.942)

1DH	DCH	261.609	C4 (261.626)
1CH	2EH	277.200	C4# (277.183)
1AH	99H	293.686	D4 (293.665)
19H	1BH	311.139	D4# (311.127)
17H	B2H	329.652	E4 (329.628)
16H	5EH	349.223	F4 (349.228)
15H	1CH	370.028	F4# (369.994)
13H	EDH	392.003	G4 (391.995)
12H	CFH	415.282	G4# (415.305)
11H	C0H	440.044	A4 (440.000)
10H	C1H	466.200	A4# (466.164)
0FH	D1H	493.827	B4 (493.883)

0EH	EDH	523.286	C5 (523.251)
0EH	17H	554.324	C5# (554.364)
0DH	4CH	587.372	D5 (587.330)
0CH	8DH	622.278	D5# (622.254)
0BH	D9H	659.196	E5 (659.255)
0BH	2EH	698.568	F5 (698.456)
0AH	8EH	739.919	F5# (739.989)
09H	F6H	784.006	G5 (783.991)
09H	67H	830.565	G5# (830.609)
08H	E0H	879.894	A5 (880.000)
08H	60H	932.401	A5# (932.328)
07H	E8H	987.654	B5 (987.767)

07H	76H	1046.572	C6 (1046.502)
07H	0BH	1108.647	C6# (1108.731)
06H	A6H	1174.398	D6 (1174.659)
06H	46H	1244.555	D6# (1244.508)
05H	ECH	1318.392	E6 (1318.510)
05H	97H	1396.648	F6 (1396.913)
05H	46H	1480.385	F6# (1479.978)
04H	FBH	1567.398	G6 (1567.982)
04H	B3H	1661.130	G6# (1661.219)
04H	6FH	1760.563	A6 (1760.000)
04H	30H	1863.933	A6# (1864.655)
03H	F3H	1976.285	B6 (1975.533)

03H	BBH	2092.050	C7(2093.005)

Code option:

Addresses: $ 4 0000
Body data: 0101 1000 (58)

$ 4 0001
data: 0010 0000 (20)

$ 4 0002
data: 0001 0000 (10)

Specification Revision History		
Version	**Content**	**Date**
1.0	Initial version	Feb. 14, 2001
1.1	Modify the transmitter register from “write only” to “Read/Write”. The 32768KHz crystal oscillator used as the UART control clock source is canceled.	May. 27, 2001
1.2	Add the bonding diagram	Oct. 10, 2001
1.3	Modify the application circuit(1). The external resistor for RC oscillator is revised to be connected to the GND.	Feb. 6,2002