

# AP0806

## C868

### **Interfacing SPI Serial EEPROM with C868 Microcontroller**

Microcontrollers



Never stop thinking.

**<C868>**

**Revision History: 2002-03**

V 0.1

Previous Version: -

Page	Subjects (major changes since last revision)

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## 1 Introduction

The C868 microcontroller offers the key feature of interfacing with an external EEPROM, (re)programming the EEPROM and loading program from EEPROM to on-chip SRAM/XRAM.

This application note describes the type of EEPROM supported, the hardware configuration of the EEPROM with the C868 and the EEPROM functions implemented by the C868 bootstrap loader. Software (three intel hex files) for this application note provides EEPROM (re)programming function. Table 1 gives the details of the software.

File Name	Function
<b>RPROTECT.HEX</b>	Remove EEPROM write protection.
<b>EPROA5_G.HEX</b>	Program EEPROM with the SRAM content and program the first byte of EEPROM as 0A5H.
<b>EPRO00_G.HEX</b>	Program EEPROM with the SRAM content and program the first byte of EEPROM as 00H.

Table 1: Software for the application note

## 2 Type of EEPROM

The type of external EEPROM supported is SPI serial EEPROM. Serial EEPROM devices offer significant advantages over parallel devices in applications where lower data transfer rates are acceptable. They also require less board space and allow microcontroller I/O pins to be conserved. This is valuable to our low pin count C868 microcontroller. Furthermore, SPI specification is easy to be implemented in software. Additionally, please note that only EEPROM in 32-byte page mode is supported. There is no limitation on the size of the EEPROM. However, as the SRAM size is 8K, It is suggested to use EEPROM ( $\geq 8K$  bytes) so that all SRAM content can be loaded to EEPROM.

## 3 Hardware Configuration

The EEPROM is connected to the C868 microcontroller in three-wire configuration as shown in Fig.1. In this configuration, the EEPROM serial data in (SI) and serial data out (SO) are both connected to the same C868

I/O pin, thereby saving a pin. This is possible because the C868 I/O pins can be dynamically reprogrammed as input or output.

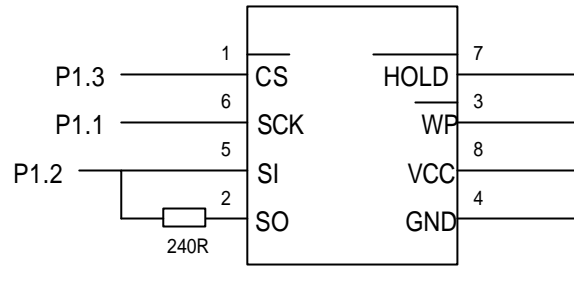


Fig. 1 Three-wire connection

## 4 Function Description

Through the C868 bootstrap loader, host PC software and software for this application note, the user can easily implement (re)programming the EEPROM and loading program from the EEPROM to SRAM/XRAM.

### 4.1 (Re)program EEPROM

After boot-up from bootrom, the MCU would try to read the first byte (Password) of EEPROM. If Password is 0A5H (a dummy code), the MCU would directly load program from the EEPROM to SRAM/XRAM and then execute from SRAM/XRAM after loading is completed. Otherwise, it would start serial communication with the host PC. The host controls the communication by sending special header information, which selects one of the working modes. For details of different working modes, please refer to application note AP08XX.

For the first time, the EEPROM is empty, so the MCU would start serial communication with the host PC. Write Protection of EEPROM must be removed to enable further EEPROM programming.

Step 1: Select Mode 0: download **RPROTECT.HEX** to XRAM.

Step 2: Select Mode 1: execute **RPROTECT.HEX** in XRAM.

Now the EEPROM is writable and can be programmed.

Step 3: Apply a reset and invoke serial communication with the host again.

Step 4: Select Mode 0: download either **EPROA5\_G.HEX** or **EPRO00\_G.HEX** to XRAM.

Step 5: Select Mode 1: execute code in XRAM.

In this way, EEPROM is programmed with the SRAM content. Pls take note that only SRAM content 0000H to 1FF7H can be programmed to EEPROM. The last 8 bytes of SRAM cannot be programmed. If you want to program the first byte of the EEPROM as the password 0A5H, use the **EPROA5\_G.HEX**; otherwise, use **EPRO00\_G.HEX**.

## 4.2 Load program from EEPROM to SRAM/XRAM

Once EEPROM is programmed with the password 0A5H, after boot-up from bootrom, the MCU would directly load program from the EEPROM to SRAM/XRAM and then execute from SRAM/XRAM after loading is completed. Otherwise, loading program from EEPROM to SRAM/XRAM can be invoked by host command mode 3.

## 5 Glossary

XRAM            On-chip ram mapped at address 0FF00H to 0FFFFH

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