SINO WEALTH

SH69P23

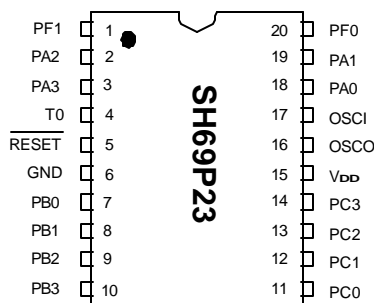PRELIMINARY

OTP 4-bit Microcontroller

Features

- SH6610C-based single-chip 4-bit micro-controller
- OTPROM: 4K X 16 bits
- RAM: 160 X 4 bits (data memory)
- Operation voltage: 2.4V - 6.0V (typical 3.0V or 5.0V)
- 14 CMOS bi-directional I/O pins
- Built in pull-up and pull-low resistor for PortA ~ PortF
- 4-level subroutine nesting (including interrupts)
- One 8-bit auto re-load timer/counter
- Warm-up timer for power on reset
- Powerful interrupt sources:
  - Internal interrupt (Timer0)
  - External interrupts: PortB & PortC (rising/falling edge)

- Oscillator (OTP option)
  - X`tal oscillator: 32.768KHz - 4MHz
  - Ceramic resonator: 400K - 4MHz
  - RC oscillator: 400K - 4MHz
  - External clock: 30K - 4MHz
- Instruction cycle time:
  - 4/32.768KHz(122us) for 32.768KHz OSC clock
  - 4/4MHz (1us) for 4MHz OSC clock
- Two low power operation modes: HALT and STOP
- Built-in watch dog timer (OTP option)
- Built-in power on reset
- Two LPD level(OTP option)
  - High level: 4.0V
  - Low level: 2.5V
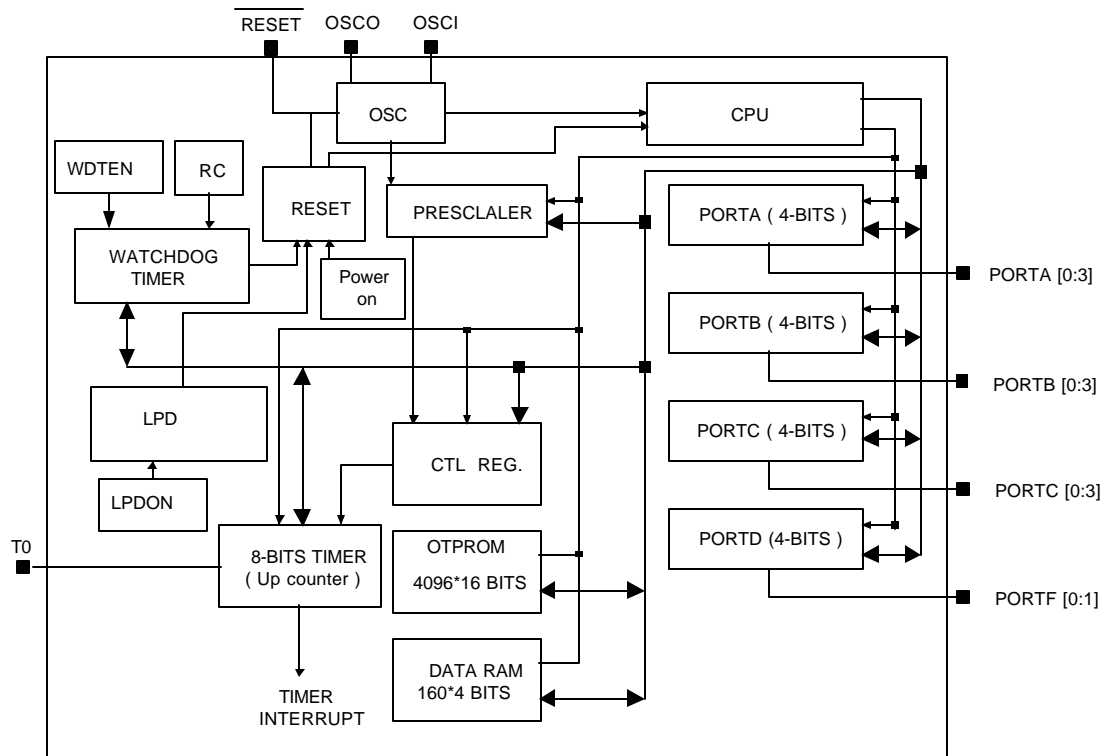- OTP type &Code protection

General Description

SH69P23 is a 4-bit micro controller. This chip integrates the SH6610C 4-bit CPU core with SRAM, 4K OTPROM, Timer and I/O Ports.

Pin Configuration

PF1	1	20	PF0
PA2	2	19	PA1
PA3	3	18	PA0
T0	4	17	OSCI
$\overline{RESET}$	5	16	OSCO
GND	6	15	V_{DD}
PB0	7	14	PC3
PB1	8	13	PC2
PB2	9	12	PC1
PB3	10	11	PC0

SH69P23

Block Diagram

Pin Description

Pin No.	Designation	I/O	Descriptions
20, 1	PF[0:1]	I/O	Bit programmable I/O
18,19, 2, 3	PA[0:3]	I/O	Bit programmable I/O.
4	T0	I	Timer Clock/Counter input pin. (Schmitt trigger input)
5	$\overline{\text{RESET}}$	I	Reset input (active low, Schmitt trigger input).
6	GND	P	Ground pin
7 - 10	PB[0:3]	I/O	Bit programmable I/O. Vector Interrupt (Active rising or falling edge by system register setup)
11 - 14	PC[0:3]	I/O	Bit programmable I/O. Vector Interrupt (Active rising or falling edge by system register setup)
15	V$_{DD}$	P	Power supply pin
16	OSCO	O	OSC output pin. No output for RC mode
17	OSCI	I	OSC input pin, connected to a crystal, ceramic or external resistor.

OTP Programming Pin Description (OTP program mode)

Pin No.	Symbol	I/O	Shared by	Description
15	V$_{DD}$	P	V$_{DD}$	Programming Power supply (+5.5V)
5	VPP	P	$\overline{\text{RESET}}$	Programming high voltage Power supply (+10.5V)
6	GND	P	GND	Ground
17	SCK	I	OSCI	Programming Clock input pin
18	SDA	I/O	PA[0]	Programming Data pin

Function Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and the Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 4K program ROM. It consists of 12-bits: the Page Register (PC11), and the Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BAC),

(2) When executing a subroutine call instruction (CALL),

(3) When an interrupt occurs,

(4) When the chip is in the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

1.2. ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)

Decision (BA0, BA1, BA2, BA3, BAZ, BAC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow which the arithmetic operation generates. During an interrupt servicing or call instruction, the carry flag is pushed into the stack and retrieved back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator

The Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data transfer between the accumulator and system register or data memory can be performed.

1.4. Stack

A group of registers are used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt. It is organized into 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of the Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). The stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceed 4, and the bottom of the stack will be shifted out.

2. OTPROM

The SH69P23 can address up to 4096 X 16 bit words of program area from $000 to $FFF.
Service routine as starting vector address.

Address	Instruction	Remarks
$000H	JMP Instruction	Jump to RESET service routine
$001H	NOP	Reserved
$002H	JMP Instruction	Jump to TIMER0 service routine
$003H	NOP	Reserved
$004H	JMP Instruction	Jump to PBC service routine

3. RAM

The built-in RAM consists of general-purpose data memory and the system register. Direct addressing in one instruction can access both data memory and the system register.

The following is the memory allocation map:

$000 - $01F: System register and I/O.
$020 - $0BF: Data memory (160 X 4 bits, divided into 2 banks. $020 - $07F: bank0, $080 - $0BF: bank1).

(a). The Configuration of the System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)
$03	-	-	-	-	-	Reserved
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit
$06-$07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B~$0C						**Bit0-3 is reserved,Always keep it to "0" in the User's program. Refer to I/O notice**
$0D	-	-	PF.1	PF.0	R/W	PORTF
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12		DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13 - $14						Reserved
$15	PULLEN	PH/PL	PBCFR	-	R/W	Bit1:PBC interrupt rising / failing edge set Bit2:Port pull-hi/low set Bit3: Port pull-up/low enable control
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	PortA input/output control 0: input 1: output
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	PortB input/output control 0: input 1: output
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	PortC input/output control 0: input 1: output
$19~$1A						**Bit0-3 is reserved,Always keep it to "1" in the User's program. Refer to I/O notice**
$1B	-	-	PF1OUT	PF0OUT	R/W	PortF input/output control 0: input 1: output
$1C	-	-	T0S	T0E	R/W	Bit0: T0 signal edge; Bit1: T0 signal source
$1D	-	-	-	-	-	Reserved
$1E	WDT	-	-	-	W	Bit3: WDT timer reset (write 1 to reset WDT)
$1F	-	-	-	-	-	Reserved

* System Register $00 - $12 (except $07H) refer to "SH6610C User manual".

(b) System Register state:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset / Low Voltage Reset	WDT Reset
$00	-	IET0	-	IEP	- 0 - 0	- 0 - 0
$01	-	IRQT0	-	IRQP	- 0 - 0	- 0 - 0
$02	-	TM0.2	TM0.1	TM0.0	- 000	- 000
$03	-	-	-	-	-	-
$04	TL0.3	TL0.2	TL0.1	TL0.0	0000	0000
$05	TH0.3	TH0.2	TH0.1	TH0.0	0000	0000
$06-$07	-	-	-	-	-	-
$08	PA.3	PA.2	PA.1	PA.0	1111	1111
$09	PB.3	PB.2	PB.1	PB.0	1111	1111
$0A	PC.3	PC.2	PC.1	PC.0	1111	1111
$0B~$0C						
$0D	-	-	PF.1	PF.0	- -11	- -11
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13 - $14					-	-
$15	PULLEN	PH/PL	PBCFR	-	010 -	010 -
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	0000	0000
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	0000	0000
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	0000	0000
$19~$1A					-	-
$1B	-	-	PF1OUT	PF0OUT	- - 00	- - 00
$1C	-	-	T0S	T0E	- - 00	- - 00
$1D	-	-	-	-	-	-
$1E	WDT	-	-	-	-	-
$1F	-	-	-	-	-	-

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

(c) Others initial state:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

4. Low Power Detection (LPD)

The LPD function is used to monitor the supply voltage and applies an internal reset in the micro-controller at the time of battery replacement. If the applied circuit satisfies the following conditions, the LPD can be incorporated using software control.
- Power supply voltage V_{DD} = 2.4 to 6.0 V

4.1 Functions of the LPD Circuit

The LPD function is selected by OTP option.
The LPD circuit has the following functions:
- It generates an internal reset signal when $V_{DD} \leq V_{LPD}$ and t t_{LPD}
- It cancels the internal reset signal when $V_{DD} > V_{LPD}$ or $V_{DD} \leq V_{LPD}$ and t < t_{LPD}
Here, V_{DD}: power supply voltage, V_{LPD}: LPD detect voltage, There are two level selected by OTP option:

        Low level: 2.3~2.7V, typical 2.5V
        High level: 3.8~4.2V, typical 4.0V
        tLPD: 100μ s~500μ s, typical 300μ s

LPD can be enabled or disabled permanently by OTP option.

5. I/O Ports

The SH69P23 provides 14 I/O pins. When every I/O is used as an input port, the port control register controls ON/OFF of the output buffer. Sections below show the circuit configuration of I/O ports.

Every I/O pin has a internal pull up / pull low resister, which is controled by PULLEN and PH/PL of $15

Each of these ports contains 4 or 2(PF) bits I/O pins. ON/OFF of the output buffer for port can be controlled by the port control register. Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Power On
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA	1111
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB	1111
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC	1111
$0B-$0C						**Bit0-3 is reserved,Always keep it to "0" in the User's program.**	
$0D			PF.1	PF.0	R/W	PORTF	1111

Equivalent Circuit for a Single I/O Pin
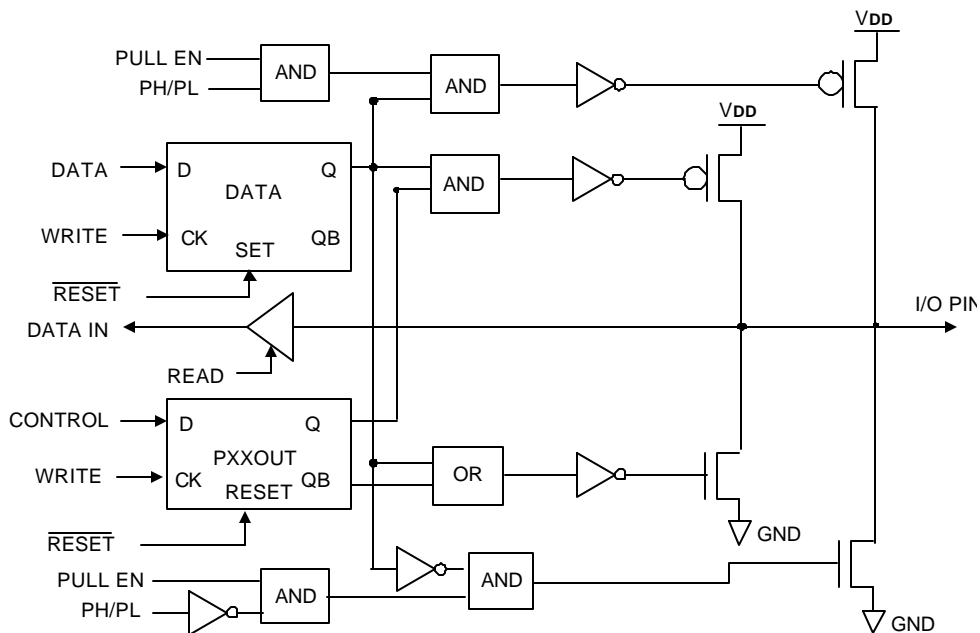
System Register $16 - $1B

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Power On
$15	PULLEN	PH/PL	PBCFR	-	R/W	Bit1:PBC interrupt rising / failing edge set Bit2:Port pull-hi/low set Bit3: Port pull-up/low enable control	010 -
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	PortA input/output control 0: input 1: output	0000
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	PortB input/output control 0: input 1: output	0000
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	PortC input/output control 0: input 1: output	0000
$19-$1A						**Bit0-3 is reserved,Always keep it to "1"** **in the User's program.**	
$1B	-	-	PF1OUT	PF0OUT	W	PortF input/output control 0: input 1: output	0000

* For SH69P23, after the chip reset, please first write 1111B to $19 $1A and write 0000B to $0B $0C . Otherwise, the halt current and stop current will be abnormal

PAXOUT, PBXOUT, PCXOUT (X = 0, 1, 2, 3), PFXOUT (X = 0, 1)

1: Use as an output buffer

0: Use as an input buffer (Power on initial)

PBCFR: 1: Rising Edge interrupt   0: Falling Edge interrupt,

PH/PL: 1: Port Pull up resister ON,   0: Port Pull low resister ON,

PULLEN: 1: Port Pull up /Pull low enable,   0: Port Pull up /Pull low disable

PORTB & PORTC interrupt

The PORTB and PORTC are used as port interrupt sources. Since PORT I/O is bit programmable I/O, so only the input port can generate an external interrupt.

When PBCFR set to 0, any one of the PORTB and PORTC input pin transitions from VDD to GND will generate an interrupt request. And further falling edge transition would not be able to make interrupt request until all of the pins return to VDD.

When PBCFR set to 1, any one of the PORTB and PORTC input pin transitions from GND to VDD will generate an interrupt request. And further rising edge transition would not be able to make interrupt request until all of the pins return to GND.

Following is the port interrupt function block-diagram.
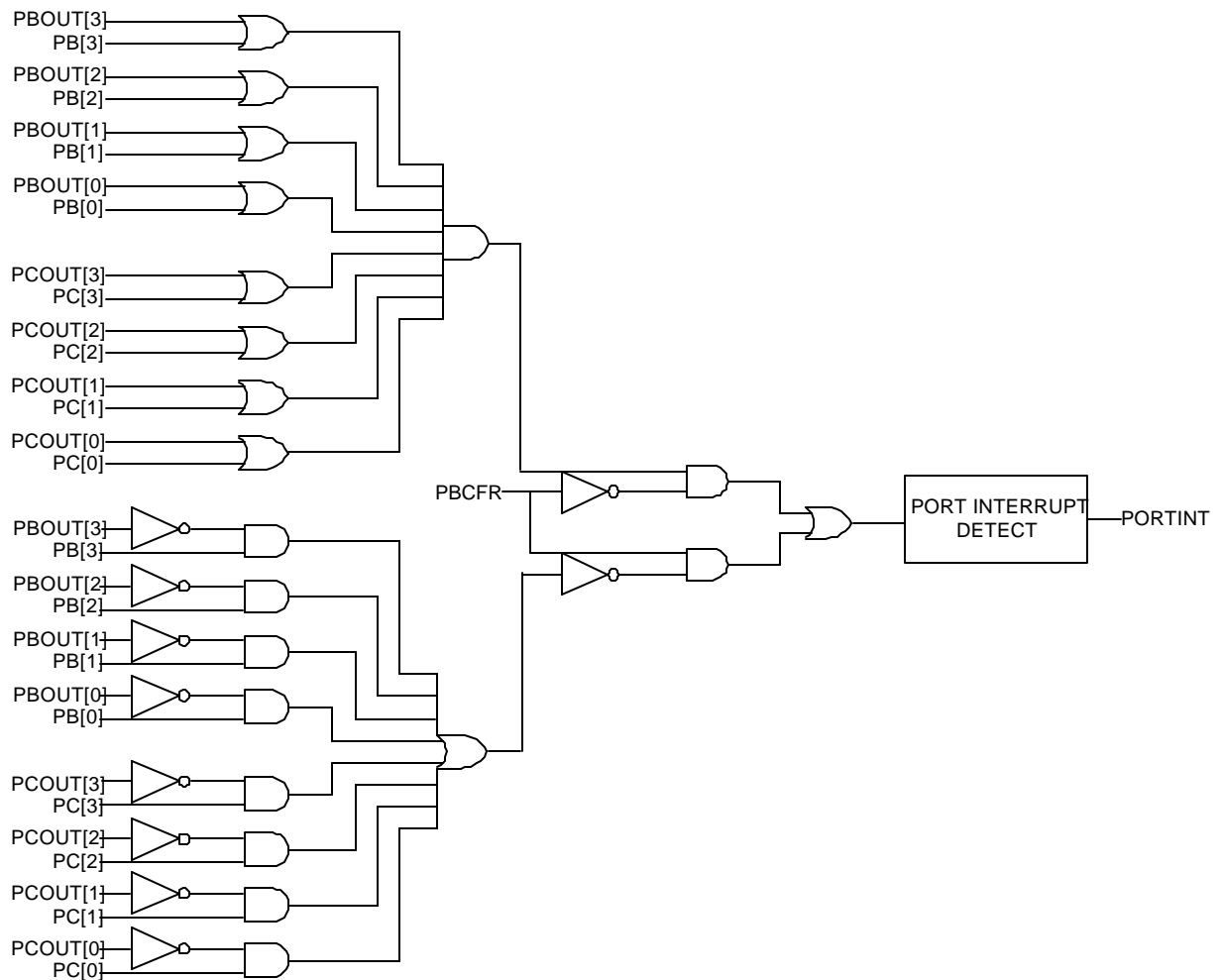
6. T0 & WDT

System Register $1C

Address	BIT3	BIT2	BIT1	BIT0	R/W	Remark
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge Bit1: T0 signal source

T0E: T0 signal edge

0: Increment on low-to-high transition T0 pin (Power on initial)
1: Increment on high-to-low transition T0 pin

T0S: T0 signal source.

0: OSC 1/4 (Power on initial).
1: Transition on T0 pin.
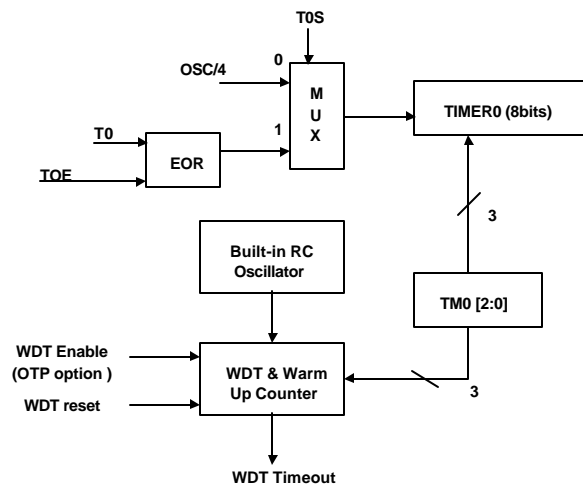
System Register $1E

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$1E	WDT	-	-	-	W	Bit3: Watchdog timer reset. (write 1 to reset WDT)

The input clock of the watchdog timer is generated by a built-in RC oscillator so that the WDT will always run even in the STOP mode. SH69P23 generates a RESET condition when the watchdog times-out. The watchdog can be enabled or disabled permanently by using the OTP option. To prevent it timing out and generating a device RESET condition, you should write this bit as "1" before timing-out. The WDT has a time-out period of more than 7ms(typical 18ms) . If longer time-out periods are desired, a prescaler with a division ratio of up to 1:2048 can be assigned to the WDT under software controll by writing to the TM0 register.

Pre-scaler divide ratio:

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Timer-out Period
1	1	1	1:1	7ms(min)
1	1	0	1:2	14ms(min)
1	0	1	1:4	28ms(min)
1	0	0	1:8	56ms(min)
0	1	1	1:32	224ms(min)
0	1	0	1:128	896ms(min)
0	0	1	1:512	3,584ms(min)
0	0	0	1:2048 (Power on initial)	14,336ms(min)
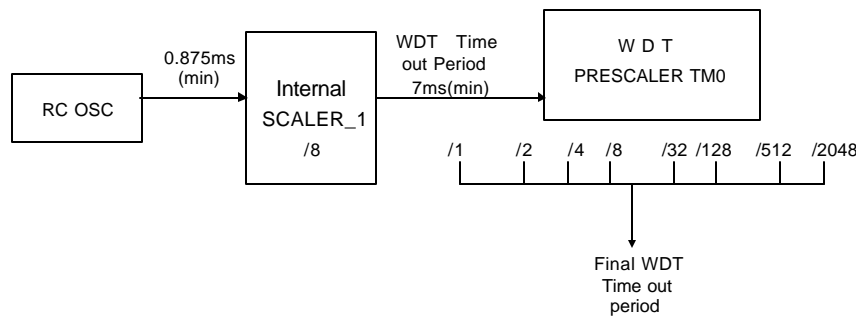
7. Timer0

SH69P23 has one 8-bit timer. The time/counter has the following features:

. 8-bit timer/counter
. Readable and writeable
. Automatic reloadable counter
. 8-prescaler scale is available
. Internal and external clock select
. Interrupt on overflow from $FF to $00
. Edge select for external event

Following is a simplified timer block diagram:
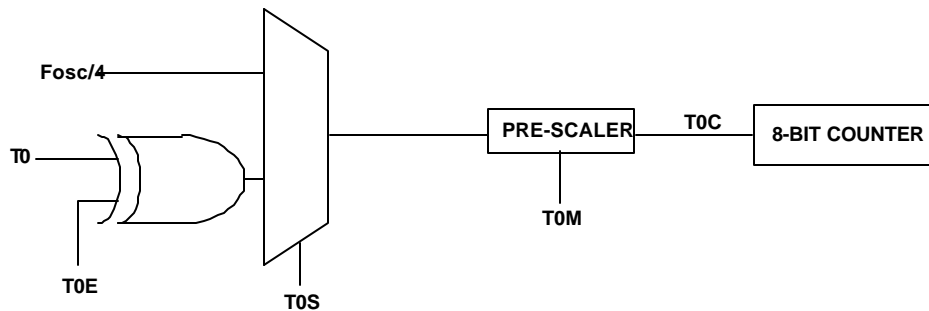
7.1. Configuration and Operation

Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The counter and load register both have low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter. Load register programming: Write the low-order digit first and then the high-order digit. The timer counter is loaded with the contents of the load register automatically when the high order digit is written or the counter counts overflow from $FF to $00.

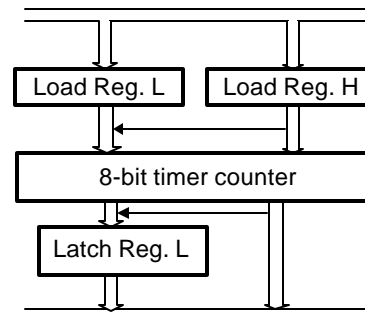Timer Load Register: Since the register H controls the physical READ and WRITE operation, please follow these rules:

Write Operation:

   First write Low nibble,
   Then write High nibble to update the counter.

Read Operation:

   High nibble first;
   Followed by Low nibble.

7.2. Timer0 Interrupt

The timer overflow will generate an internal interrupt request, when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will proceed. This can also be used to waken the CPU from HALT mode.

7.3. Timer0 Mode Register

The timer can be programmed in several different prescaler ratios by setting the Timer Mode register (TM0). The 8-bit counter counts prescaler overflow output pulses. The timer mode registers (TM0) are 3-bit registers used for timer control as shown in table1. These mode registers select the input pulse sources into the timer.

Table 1. Timer 0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^9$	512
0	1	0	$/2^7$	128
0	1	1	$/2^5$	32
1	0	0	$/2^3$	8
1	0	1	$/2^4$	4
1	1	0	$/2^1$	2
1	1	1	$/2^0$	1

7.4. External Clock/Event T0 as Timer0 Source

When an external clock/event input is used for the TM0, it is synchronized with the CPU system clock. Therefor the external source must follow certain constraints. The output from the T0M multiplex is T0C. It is sampled by the system clock in instruction frame cycle. Therefore it is necessary for the T0C to be high (at least 2 tosc) and low (at least 2 tosc). When the prescaler ratio selects $/2^0$, the T0C is the same as the system clock input. Therefore the requirement is as follows

$$T0H = T0CH = T0 \text{ high time} \geq 2 \text{ tosc} + \Delta T$$

$$T0L = T0CL = T0 \text{ low time} \geq 2 \text{ tosc} + \Delta T$$

Note: $\Delta T = 40ns$

When another prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical.

Then:

$$T0C \text{ high time} = T0C \text{ low time} = \frac{N * T0}{2}$$

Where

T0 = Timer0 input period

N = prescaler value

The requirement is, therefore:

$$\frac{N * T0}{2} \geq 2 \text{ tosc} + \Delta T \text{ , or T0} \geq \frac{4 * t_{OSC} + 2 \ T}{N}$$

The limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

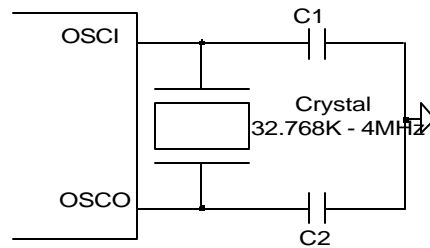$$T0 = \text{Timer0 period} \geq \frac{4 * t_{OSC} + 2\Delta T}{N}$$

8. System Clock and Oscillator

System clock generator produces the basic clock pulses that provide the system clock to the CPU and any peripherals. Instruction cycle time
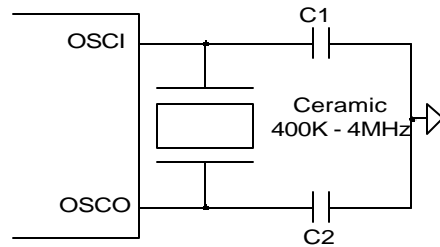
(1) 4/32.768KHz (≈122us) for 32.768KHz system clock

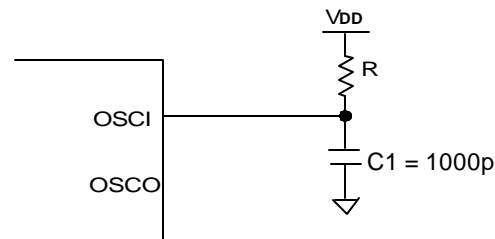(2) 4/4MHz (1us) for 4MHz system clock

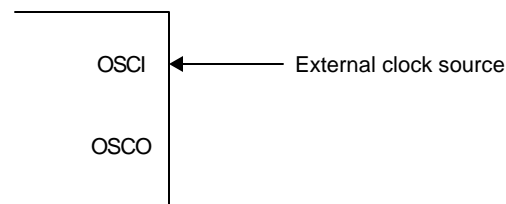### 8.1 Oscillator

(1) Crystal oscillator: 32.768KHz – 4MHz.

(2) Ceramic resonator: 400KHz – 4MHz.

(3) RC oscillator: 400KHz – 4MHz.


(4) External input clock: 30KHz – 4MHz.

9. OTP option
(a). Oscillator range
 0: OSC @ 32K~2MHz (default)
 1: OSC @ 2M ~ 4MHz
(b). LPD voltage range
 0: High LPD voltage (default)
 1: Low LPD Voltage
(c): LPD on/off control
 0: LPD off (default)
 1: LPD on
(d): WDT on/off control
 0: WDT on (default)
 1: WDT off
(e): Oscillator select:
 000: External clock (default)
 100: RC Oscillator 400k~4M
 110: Crystal /Ceramic Resonator 400k~4M
 111: X'tal 32768Hz

10. In System Programming Notice for OTP

For COB(chip on Board) assembling mode, the In System Programming technology is valid for OTP chip of SinoWealth Co..
The Programming Interface of OTP chip must be left on user's application PCB, and users can assemble all components
including OTP chip in application PCB before programming OTP chip first. Of course it is accessible that bonding OTP chip
only first, then programming code, and assembling the others components at last.
Because the programming timing of Programming Interface is very sensitive, so four jumpers are needed (VDD, VPP, SDA,
SCK) to separate programming pins from application circuit just as following diagram.
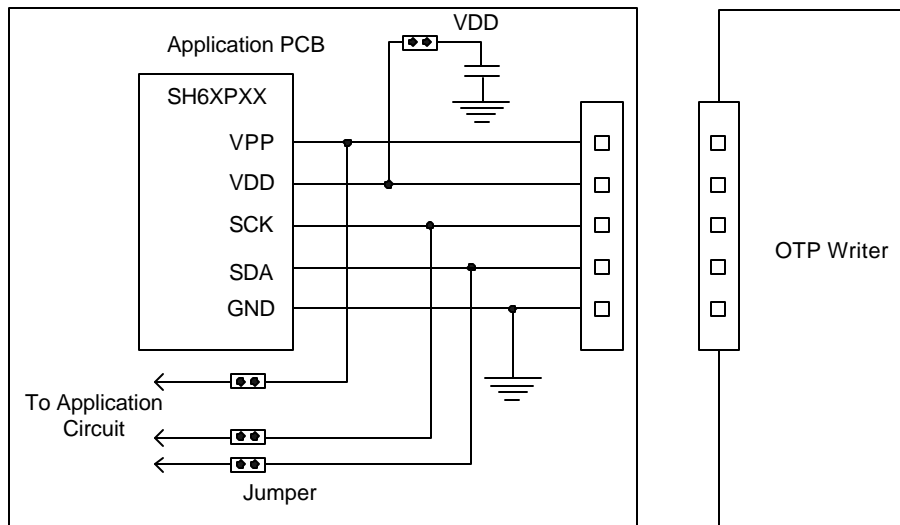
The recommended step is as following for these jumpers:
1) The jumper is Open to separate programming pins from application circuit before programming code.
2) Connect the programming interface with OTP Writer and Begin Programming code.
3) Disconnect OTP writer and short these jumpers when programming is finished.
 For more detail information please refer to the OTP writer user manual.

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Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	$0 \rightarrow AC[3]$; $AC[0] \rightarrow CY$; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I + 1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjustment for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjustment for sub.	CY

Transfer Instructions

Mnemonic	Instruction Code	Function	Flag Change
LDA　X (, B)	00111 0bbb xxx xxxx	AC　　← Mx	
STA　X (, B)	00111 1bbb xxx xxxx	Mx　　← AC	
LDI　X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instructions

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC　　← X　if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC　　← X　if AC ≠ 0	
BC　X	10011 xxxx xxx xxxx	PC　　← X　if CY = 1	
BNC　X	10001 xxxx xxx xxxx	PC　　← X　if CY ≠ 1	
BA0　X	10100 xxxx xxx xxxx	PC　　← X　if AC(0) = 1	
BA1　X	10101 xxxx xxx xxxx	PC　　← X　if AC(1) = 1	
BA2　X	10110 xxxx xxx xxxx	PC　　← X　if AC(2) = 1	
BA3　X	10111 xxxx xxx xxxx	PC　　← X　if AC(3) = 1	
CALL X	11000 xxxx xxx xxxx	ST　　← CY; PC + 1 PC　　← X (Not including p)	
RTNW H, L	11010 000h hhh llll	PC　　←ST; TBR ← hhhh; AC　　← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP　X	1110p xxxx xxx xxxx	PC　　← X (Including p)	
TJMP	11110 1111 111 1111	PC　　← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank. Every $7F as one RAM bank.
ST	Stack	TBR	Table Branch Register

Absolute Maximum Rating*

DC Supply Voltage . . . . **–**0.3V to + 7.0V

Input Voltage . . . . −0.3V to V$_{DD}$ + 0.3V

Operating Ambient Temperature . . . −40 to + 85

Storage Temperature . . . .-55 to + 125

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V$_{DD}$ = 5.0V GND = 0V, T$_A$ = 25 , F$_{OSC}$ = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V$_{DD}$	4.5	5.0	6.0	V	
Operating Current	I$_{OP}$		0.6	1.0	mA	All output pins unloaded (Execute NOP instruction)
Stand by Current (HALT)	I$_{SB1}$			0.5	mA	All output pins unloaded
Stand by Current (STOP)	I$_{SB2}$			1	μA	All output pins unloaded, LPD off (If LPD on, I$_{SB2X}$ = I$_{SB2}$ + 2μA) WDT off (If WDT on, I$_{SB2X}$ = I$_{SB2}$ + 15μA)
Input Low Voltage	V$_{IL1}$	GND		0.2 X V$_{DD}$	V	I/O ports, pins tri-state
Input Low Voltage	V$_{IL2}$	GND		0.15 X V$_{DD}$	V	$\overline{RESET}$, T0
Input Low Voltage	V$_{IL3}$	GND		0.15 X V$_{DD}$	V	OSCI (Driven by external clock)
Input High Voltage	V$_{IH1}$	0.8 X V$_{DD}$		V$_{DD}$	V	I/O ports, pins tri-state
Input High Voltage	V$_{IH2}$	0.85 X V$_{DD}$		V$_{DD}$	V	$\overline{RESET}$, T0
Input High Voltage	V$_{IH3}$	0.85 X V$_{DD}$		V$_{DD}$	V	OSCI (Driven by external Clock)
Input Leakage Current	I$_{IL1}$	-1		1	μA	I/O ports, GND < V$_{I/O}$ < V$_{DD}$
Input Leakage Current	I$_{IL2}$	-5			μA	V$_{\overline{RESET}}$ = GND + 0.25V
Input Leakage Current	I$_{IL3}$		1	5	μA	V$_{\overline{RESET}}$ = V$_{DD}$
Input Leakage Current	I$_{IL4}$	-3	1	3	μA	T0, GND < Vt0 < V$_{DD}$
Input Leakage Current	I$_{IL5}$	-3	1	3	μA	For OSCI
Pull-up/ Pull-low Resistor	R$_P$		150		KΩ	PULL-UP/ PULL-LOW resistor
Output High Voltage	V$_{OH}$	V$_{DD}$ − 0.7			V	I/O ports, I$_{OH}$ = -10mA OSCO$_{RC}$, I$_{OH}$ = -0.7mA
Output Low Voltage	V$_{OL}$			GND + 0.6	V	I/O ports, I$_{OL}$ = 20mA OSCO$_{RC}$, I$_{OL}$ = 1.6mA

AC Electrical Characteristics (V$_{DD}$ = 5.0V GND = 0V, T$_A$ = 25 , unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start Time	T$_{OSC1}$			1	s	X'tal osc = 32.768KHz
RESET pulse width (low)	T$_{RESET}$	10			μs	V$_{DD}$ = 5.0V
WDT Period	Twdt	7	18		ms	V$_{DD}$ = 5.0V
Frequency Stability (RC)	Δ F/F			20	%	RC Oscillator: [F(5.0)-F(4.5)]/F(5.0)

DC Electrical Characteristics (V$_{DD}$ = 3.0V, GND = 0V, T$_A$ = 25 , F$_{OSC}$ = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V$_{DD}$	2.4	3.0	4.5	V	
Operating Current	I$_{OP}$		0.3	0.6	mA	All output pins unloaded (Execute NOP instruction)
Stand by Current (HALT)	I$_{SB1}$			0.2	mA	All output pins unloaded
Stand by Current (STOP)	I$_{SB2}$			1	μA	All output pins unloaded, LPD off (If LPD on, I$_{SB2X}$ = I$_{SB2}$ + 2μA) WDT off (If WDT on, I$_{SB2X}$ = I$_{SB2}$ + 5μA)
Input Low Voltage	V$_{IL1}$	GND		0.2 X V$_{DD}$	V	I/O ports, pins tri-state
Input Low Voltage	V$_{IL2}$	GND		0.15 X V$_{DD}$	V	$\overline{RESET}$, T0
Input Low Voltage	V$_{IL3}$	GND		0.15 X V$_{DD}$	V	OSCI (Driven by external clock)
Input High Voltage	V$_{IH1}$	0.8 X V$_{DD}$		V$_{DD}$	V	I/O ports, pins tri-state
Input High Voltage	V$_{IH2}$	0.85 X V$_{DD}$		V$_{DD}$	V	$\overline{RESET}$, T0
Input High Voltage	V$_{IH3}$	0.85 X V$_{DD}$		V$_{DD}$	V	OSCI (Driven by external Clock)
Input Leakage Current	I$_{IL1}$	-1		1	μA	I/O ports, GND < Vi/o < V$_{DD}$
Input Leakage Current	I$_{IL2}$	-5			μA	V$_{\overline{RESET}}$ = GND + 0.25V
Input Leakage Current	I$_{IL3}$		1	5	μA	V$_{\overline{RESET}}$ = V$_{DD}$
Input Leakage Current	I$_{IL4}$	-3	1	3	μA	T0, GND < Vt0 < V$_{DD}$
Input Leakage Current	I$_{IL5}$	-3	1	3	μA	For OSCI
Output High Voltage	V$_{OH}$	V$_{DD}$ – 0.7			V	I/O ports, I$_{OH}$ = -7mA, V$_{DD}$ = 3V OSCO$_{RC}$, I$_{OH}$ = -0.7mA, V$_{DD}$ = 3V
Output Low Voltage	V$_{OL}$			GND + 0.4	V	I/O ports, I$_{OL}$ = 8mA, V$_{DD}$ = 3V OSCO$_{RC}$, I$_{OL}$ = 1.0mA, V$_{DD}$ = 3V

User Notice:
Max. Current into V$_{DD}$ = 100mA;
Max. Current out of V$_{SS}$ = 150mA
Max. Output current sunk by any I/O port = 50mA;
Max. Output current sourced by any I/O port = 40mA

**AC Electrical Characteristics (VDD = 3.0V, GND = 0V, TA = 25 , unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start Time	T$_{OSC1}$			1	s	Crystal Osc = 32.768KHz, V$_{DD}$ = 3.0V
RESET pulse width (low)	T$_{RESET}$	12			μs	V$_{DD}$ = 3.0V
WDT Period	T$_{WDT}$	7	18		ms	V$_{DD}$ = 3.0V
Frequency Stability (RC)	Δ F/F			20	%	RC oscillator (1MHz): [F(3.0)-F(2.7)]/F(3.0)

Low Power Detect Electrical Characteristics
(a) V$_{DD}$ = 2.4~6V, GND = 0V, T$_A$ = 25°C, F$_{OSC}$ = 4MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LPD Voltage(Low)	V$_{LPD1}$	2.3	2.5	2.7	V	LPD enable
LPD Voltage(High)	V$_{LPD2}$	3.8	4.0	4.2	V	LPD enable
Low power detect ignore time	t$_{LPD}$	100	300	500	us	LPD enable and V$_{DD}$<V$_{LPD}$

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Tcy	Instruction Cycle Time	1		122	µs	
Tiw	T0 Input Width	(Tcy + 40)/N			ns	N = Prescaler divide ratio
TiwH	High Pulse Width	1/2 tiw			ns	
TiwL	LOW Pulse Width	1/2 tiw			ns	

Timing Waveform

T0 Input Waveform
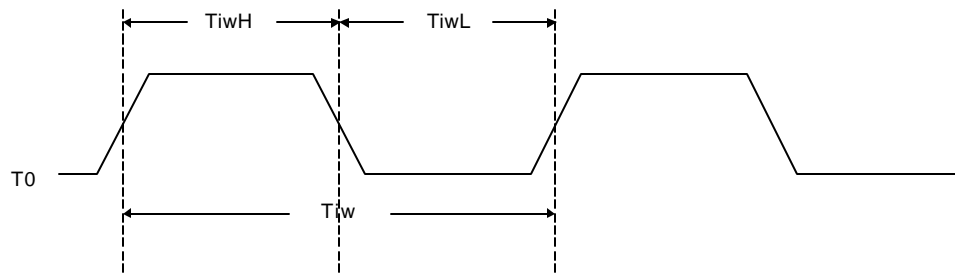
Built-in RC Oscillator (Only use for Watch Dog)
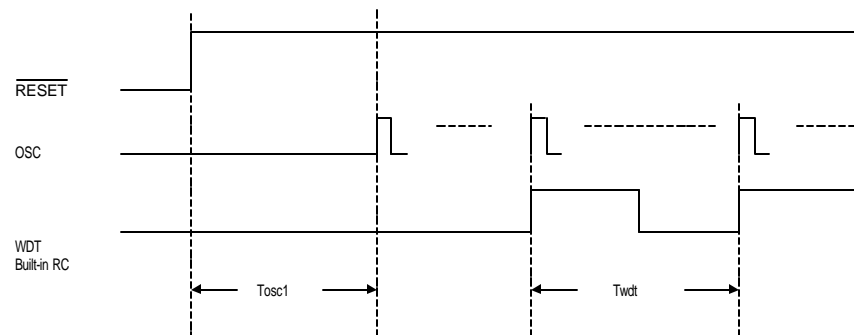
Typical RC oscillator Resistor vs. Frequency: (VDD = 5V, for reference only)
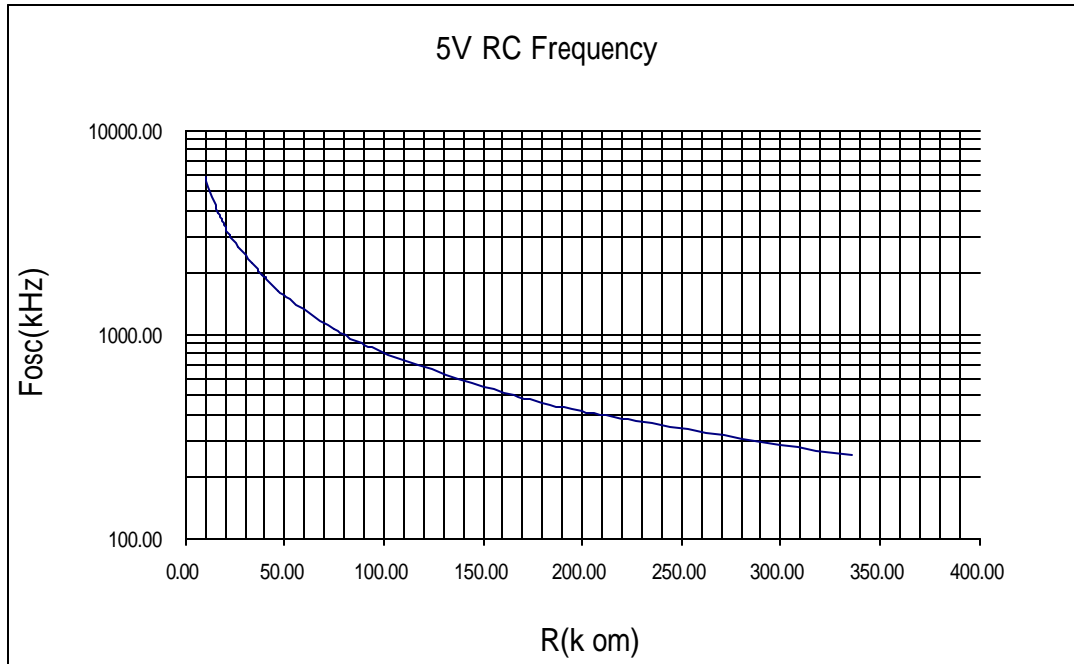
5V RC Frequency

Typical RC Oscillator Resistor vs. Frequency: (VDD = 3V, for reference only)
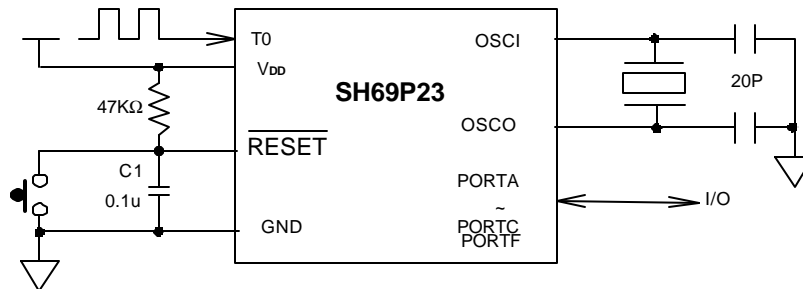

3V RC Frequency
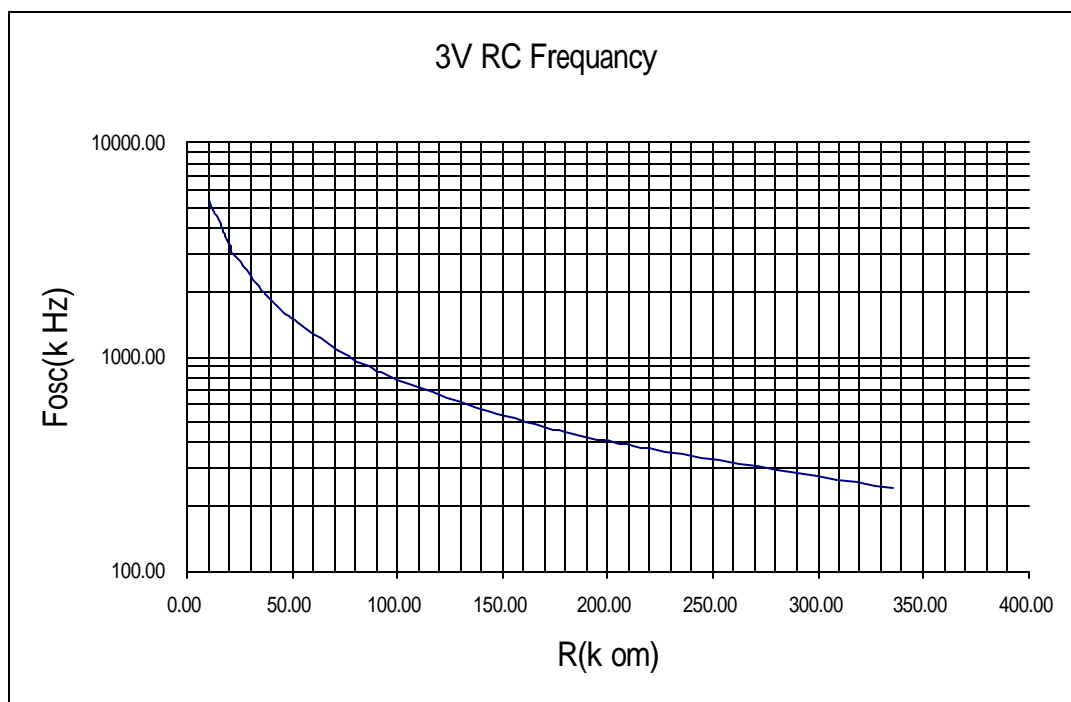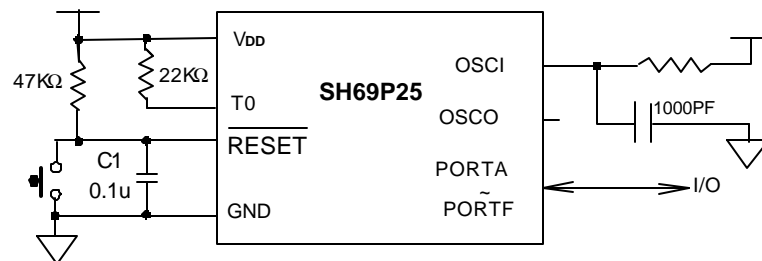
Application Circuit (for reference only)

AP1

(1) Operating voltage: 5.0V

(2) Oscillator: Ceramic resonator 455KHz

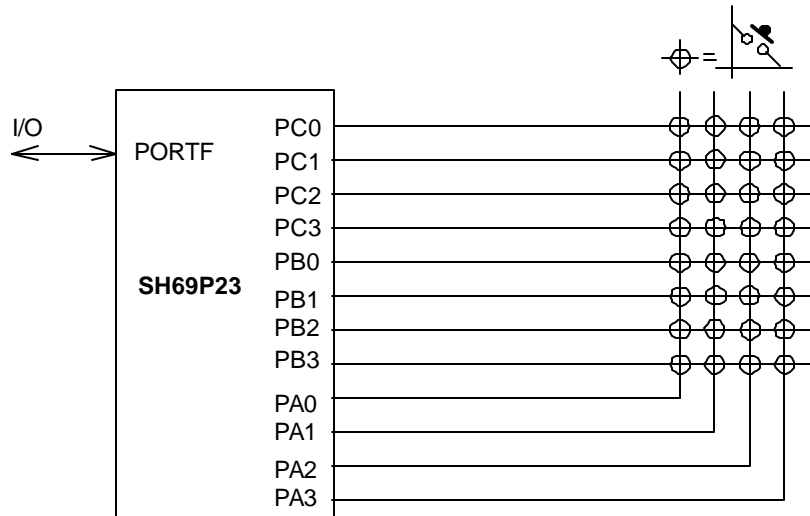(3) T0 input timer clock / counter

(4) PORTA - F: I/O

AP2

(1) Operating voltage: 5.0V.
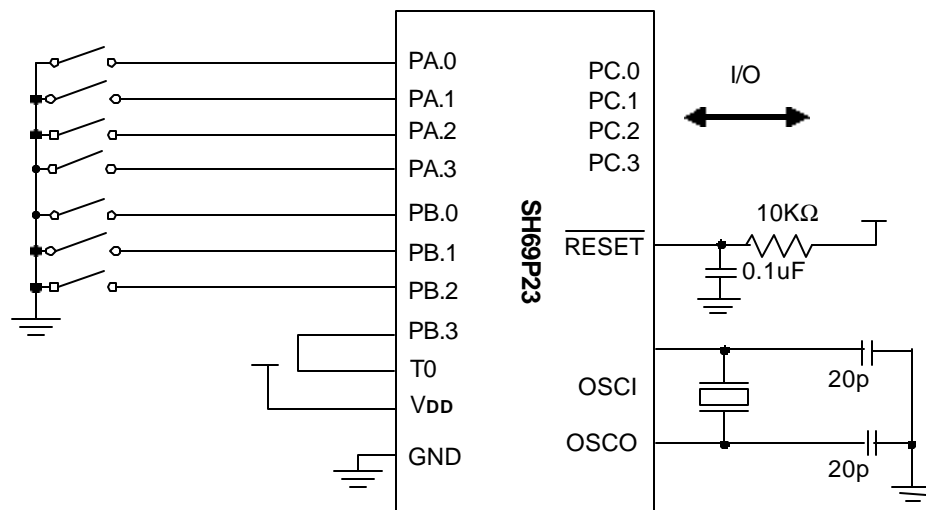
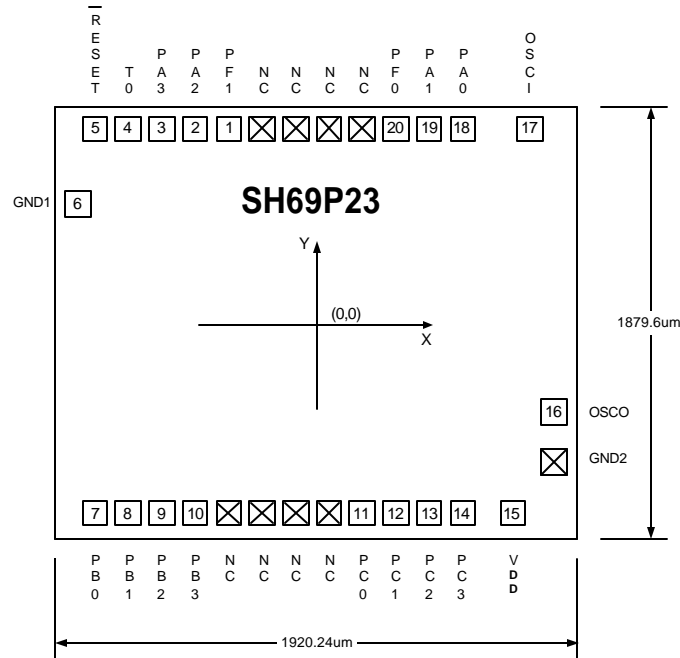(2) Oscillator: RC 420KHz.

(3) PORTA – C,F: I/O

AP3

(1) PORTA - C: as scan KEY BOARD (32 keys)

(2) PORTF: I/O,

(3) All input pin internal Pull up On

AP4:

a. Operating voltage: 3.0V.

b. Oscillator: Crystal 32.768KHz.

c. PORTA - C: I/O. (PULL UP ON)

Bonding Diagram

NOTE:

1. GND1 BONDING TO GROUND PIN

2. GND2 BONDING TO SUBSTRATE

3. SUBSTRATE BONDING TO GROUND PIN

Pad Location   unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PF 1	-283	749.5	11	PC 0	244	-749.5
2	PA 2	-413	749.5	12	PC 1	374	-749.5
3	PA 3	-543	749.5	13	PC 2	504	-749.5
4	T0	-673	749.5	14	PC 3	634	-749.5
5	$\overline{RESET}$	-803	749.5	15	VDD	769	-749.5
6	GND1	-818	585		GND2	822	-619.5
7	PB 0	-796	-749.5	16	OSCO	725	-420
8	PB 1	-666	-749.5	17	OSCI	767	749.5
9	PB 2	-536	-749.5	18	PA 0	587	749.5
10	PB 3	-406	-749.5	19	PA 1	467	749.5
				20	PF 0	347	749.5

Ordering Information

Part No.	Packages
SH69P23H	CHIP FORM
SH69P23	20L DIP
SH69P23M	20L SOP

Package Information

P-DIP 20L Outline Dimensions   unit: inches/mm
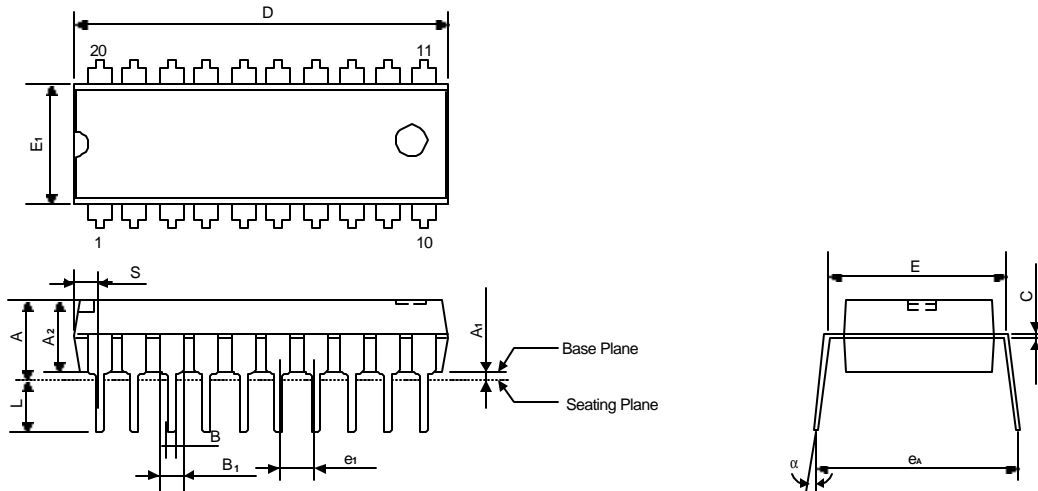
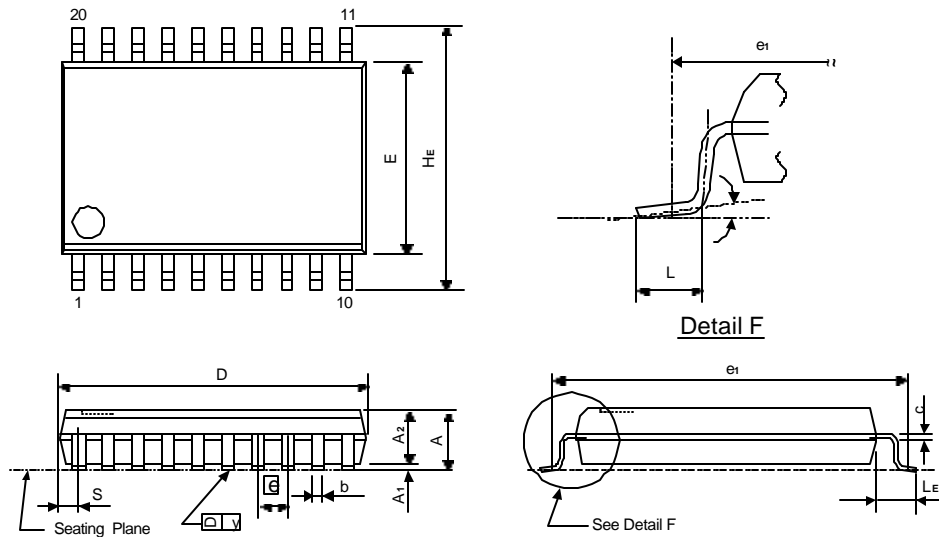| Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A$_1$	0.010 Min.	0.25 Min.
A$_2$	0.130 ± 0.010	3.30 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B$_1$	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.026 Typ. (1.046 Max.)	26.06 Typ. (26.57 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E$_1$	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e$_1$	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
e$_A$	0.345 ± 0.035	8.76 ± 0.89
S	0.078 Max.	1.98 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E$_1$ does not include resin fins.
3. Dimension S includes end flash.

SOP 20L (W.B.) Outline Dimensions   unit: inches/mm

Detail F

Seating Plane

See Detail F

Symbol	Dimensions in inches	Dimensions in mm
A	0.106 Max.	2.69 Max.
A1	0.004 Min.	0.10 Min.
A2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.500 ± 0.02	12.80 ± 0.51
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e1	0.376 NOM.	9.50 NOM.
HE	0.406 ± 0.012	10.31 ± 0.31
L	0.032 ± 0.008	0.81 ± 0.20
LE	0.055 ± 0.008	1.40 ± 0.20
S	0.042 Max.	1.07 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Product Spec. Change Notice

	SH69P23 Specification Revision History	
Version	**Content**	**Date**
1.01	Change "Max current into VDD pin" from 50mA to 100mA Change "Max. output current sunk by any I/O port " from25mA to 50mA Change "Max. Output current sourced by any I/O port" from 20mA to 40mA Delete the defination of "Max. Output current sunk by all ports (A, B, C, D, E, F) = 50mA", and "Max. Output current sourced by all ports (A, B, C, D, E, F) = 40mA" Add "In System Programming Notice for OTP" Add the "Bonding Diagram"	Nov. 2003
1.0	Reduce operating current. Add RC Frequency-Resistance diagram.	May.2003
0.1	Original	Mar.2003